1. Introduction

This document contains updates to the specifications for the Marvell® ARMADA 16x Applications Processor Family. This document is a compilation of device and documentation errata, specification clarifications, and specification changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, and tools.

Marvell Corporation has endeavored to include all documented errata in the consolidation process. However, Marvell makes no representations or warranties concerning the completeness of the ARMADA 16x Applications Processor Family Specification Update, Rev. 2.0 Release I.

Information types defined in Nomenclature are consolidated into the ARMADA 16x Applications Processor Family Specification Update, Rev. 2.0 Release I. and are no longer published in other documents.

This document might also contain information that was not previously published. Change bars indicate changed/edited or new content.

This document contains the following sections:

- Section 2. "Affected and Related Documents"
- Section 3. "Nomenclature"
- Section 4. "Functional Errata Summary"
- Section 5. "Detailed Descriptions for Functional Errata"
- Section 6. "Documentation Change Summary"
- Section 7. "Detailed Descriptions for Documentation Changes"
- Section 8. "Specification Changes Summary"
- Section 9. "Detailed Descriptions for Specification Changes"

1.1 Document Revision History Table

Table 1: Document Revision History Table

<table>
<thead>
<tr>
<th>Doc Rev#</th>
<th>Date</th>
<th>Devices Covered</th>
<th>Description of Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.0/Release K</td>
<td>10/19/2010</td>
<td>Marvell® ARMADA 16x Applications Processor Family</td>
<td>Added Functional Errata: DPF-678</td>
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<td>Doc Rev#</td>
<td>Date</td>
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<tr>
<td>2.0 /</td>
<td>8/18/2010</td>
<td>Marvell® ARMADA 16x Applications Processor</td>
<td>Added Functional Errata: DPF-928, DPF-929, DPF-933</td>
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<tr>
<td>Release I</td>
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<td>Family</td>
<td>Updated Functional Errata: DPF-782</td>
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<td>Added Documentation Change: DPF-940</td>
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<td>Added Specification Changes: DPF-656, DPF-936</td>
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<td>Added Functional Errata: DPF-843, DPF-898, DPF-904, DPF-910</td>
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<td>Release H</td>
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<td>Family</td>
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<td>Updated Documentation Change: DPF-829, DPF-830, DPF-842</td>
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<td>Removed Documentation Change: DPF-680, DPF-637, DPF-789</td>
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<td>Release G</td>
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<td>4-30-2010</td>
<td>Marvell® ARMADA 16x Applications Processor</td>
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<td>4-16-2010</td>
<td>Marvell® ARMADA 16x Applications Processor</td>
<td>Updated Functional Errata: DPF-632, DPF-743, DPF-698, DPF-699, DPF-758</td>
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<td>3-22-2010</td>
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<td></td>
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<td>DPF-639, DPF-640, DPF-641, DPF-651, DPF-653, DPF-668, DPF-669, DPF-672, DPF-698,</td>
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<td>DPF-699, DPF-701, DPF-703, DPF-717, DPF-724, DPF-730, DPF-749, DPF-753, DPF-760,</td>
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<td>DPF-763, DPF-764, DPF-782</td>
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<td>Updated Documentation Changes: DPF-631, DPF-680, DPF-789, DPF-829</td>
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<td>Added Specification Changes: DPF-585, DPF-864</td>
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<td>Updated Specification Changes: DPF-594, DPF-726, DPF-740, DPF-771</td>
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<td>Removed Specification Changes: DPF-771</td>
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<td>2-19-2010</td>
<td>Marvell® ARMADA 16x Applications Processor</td>
<td>Added Functional Errata: DPF-820, DPF-819, DPF-781, DPF-724</td>
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<td>Added Specification Changes: DPF-726, DPF-740, DPF-771</td>
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<td>2.0 /</td>
<td>2-05-2010</td>
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<td>Added Functional Errata: DPF-470, DPF-701</td>
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<td>Release B</td>
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<td>Family</td>
<td>Updated Documentation Changes: DPF-829, DPF-830</td>
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Table 1: Document Revision History Table (Continued)

<table>
<thead>
<tr>
<th>Doc Rev#</th>
<th>Date</th>
<th>Devices Covered</th>
<th>Description of Changes</th>
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<tr>
<td>2.0 /</td>
<td>1-22-2010</td>
<td>Marvell® ARMADA 16x Applications Processor Family</td>
<td>Added Functional Errata: Updated Functional Errata: DPF-669, DPF-629, DPF-730, DPF-760, DPF-763, DPF-764, DPF-724</td>
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<td>Removed Specification Changes: DPF-411</td>
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<td>Added Documentation Changes: DPF-829, DPF-830, DPF-789</td>
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<td>Removed Documentation Changes: DPF-705</td>
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<td></td>
<td></td>
<td></td>
<td>Updated paragraph formatting and remove reference to FEr# and SCR#. Updated summary tables to reference errata number as Errata #:</td>
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<tr>
<td>2.0 /</td>
<td>1-8-2010</td>
<td>Marvell® ARMADA 16x Applications Processor Family</td>
<td>Removed all errata associated with R0 and S0 stepping</td>
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<tr>
<td>Release -</td>
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<td></td>
<td>Updated the &quot;Specification Changes&quot; and &quot;Documentation Changes&quot; sections</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>Added Functional Errata: DPF-672, DPF-717, DPF-758, DPF-730</td>
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</tbody>
</table>
2. **Affected and Related Documents**

Table 2 lists the documents affected by and related to this errata update. Contact a Marvell representative to obtain the latest revisions of these documents.

<table>
<thead>
<tr>
<th>Title</th>
<th></th>
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<tbody>
<tr>
<td>Marvell® ARMADA PXA16x Applications Processor Family Hardware Manual (MV-S301545-00)</td>
<td></td>
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<tr>
<td>Marvell® ARMADA PXA16x Applications Processor Family Software Manual (MV-S301544-00)</td>
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</tbody>
</table>
3. Nomenclature

Errata are design defects or errors. These errata might cause the Marvell® ARMADA 16x Applications Processor Family's behavior to deviate from published specifications. Hardware and software designed to be used with any given processor stepping must assume that all errata documented for that stepping are present on all devices unless otherwise noted.

Specification changes and clarifications describe a modification to the current published specification or further highlight a specification's impact to a complex design situation. These also include any typos, errors, and omissions from the current published specifications. These will be incorporated in any new release of the document.

Errata # is an internal database that Marvell uses to track and resolve product issues. It is not customer visible. Internal teams are familiar with the numbers listed in this document.

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Note

Errata in the specification update throughout the product's life cycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata moved from the specification update are archived and made available upon request. Specification changes, specification clarifications, and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (data sheets, manuals, and so forth).
4. Functional Errata Summary

The following tables summarize the errata, specification changes, specification clarifications, and documentation changes that apply to the Marvell® ARMADA 16x Applications Processor Family. These tables use the following notations:

Table 3: Change Notations

<table>
<thead>
<tr>
<th>Notation</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>R0, S0, etc</td>
<td>This errata exists in the Marvell® ARMADA 16x Applications Processor Family stepping indicated and includes specification change or clarification that applies to this stepping</td>
</tr>
<tr>
<td>Plan Fix</td>
<td>This errata will be fixed in a future stepping of the product.</td>
</tr>
<tr>
<td>Plan Fix Xx</td>
<td>An attempt to fix this errata was made in stepping Xx</td>
</tr>
<tr>
<td>Fixed in Xx</td>
<td>This errata has been fixed in the listed stepping.</td>
</tr>
<tr>
<td>No Fix</td>
<td>There are no plans to fix this errata.</td>
</tr>
<tr>
<td>Eval</td>
<td>Marvell is still researching this errata.</td>
</tr>
<tr>
<td>No Bug</td>
<td>This errata has been determined to be a false errata. Check the workaround section to determine if a document clarification was necessary.</td>
</tr>
<tr>
<td>Shaded</td>
<td>This is either new or has been modified from the previous version of the document</td>
</tr>
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Table 4: Stepping Definitions

<table>
<thead>
<tr>
<th>Notation</th>
<th>Meaning</th>
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<tbody>
<tr>
<td>R0</td>
<td>First silicon engineering samples</td>
</tr>
<tr>
<td>S0</td>
<td>Pre-production engineering samples</td>
</tr>
<tr>
<td>A0, B0</td>
<td>Production silicon</td>
</tr>
</tbody>
</table>

Table 5: Functional Errata Summary Table

<table>
<thead>
<tr>
<th>Erratum Number</th>
<th>Erratum Description</th>
<th>Page</th>
<th>Affected Stepping</th>
<th>Fixed Stepping</th>
</tr>
</thead>
<tbody>
<tr>
<td>DPF-321</td>
<td>USB: USB Suspend/Resume fails when PHY is suspended (USB_PORTSC[PHCD]=1).</td>
<td>page 12</td>
<td>A0, B0</td>
<td>No Fix</td>
</tr>
<tr>
<td>DPF-517</td>
<td>An exception occurs when reading the Host Control Version Register for SD2 and SD4 (SD2_HOST_CTRL_VER and SD4_HOST_CTRL_VER).</td>
<td>page 12</td>
<td>A0, B0</td>
<td>No Fix</td>
</tr>
<tr>
<td>DPF-603</td>
<td>The WAKEUP1 bit in the MPMU_AWUCRS register is asserted after a power-on reset.</td>
<td>page 12</td>
<td>A0, B0</td>
<td>No Fix</td>
</tr>
<tr>
<td>DPF-640</td>
<td>A Test-Logic-Reset sequence does not automatically return the IDCODE in the Data Register.</td>
<td>page 13</td>
<td>A0</td>
<td>B0</td>
</tr>
<tr>
<td>Erratum Number</td>
<td>Erratum Description</td>
<td>Page</td>
<td>Affected Stepping</td>
<td>Fixed Stepping</td>
</tr>
<tr>
<td>---------------</td>
<td>-------------------------------------------------------------------------------------</td>
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</tr>
<tr>
<td>DPF-642</td>
<td>The TDI and TMS default pull state do not meet IEEE requirements.</td>
<td>page 13</td>
<td>A0, B0</td>
<td>No Fix</td>
</tr>
<tr>
<td>DPF-643</td>
<td>An extra bit is shifted into the Data Register when using Concatenate mode.</td>
<td>page 13</td>
<td>A0, B0</td>
<td>No Fix</td>
</tr>
<tr>
<td>DPF-577</td>
<td>Burst assesses to DDR devices fail</td>
<td>page 13</td>
<td>A0, B0</td>
<td>No Fix</td>
</tr>
<tr>
<td>DPF-641</td>
<td>The Boot ROM does not boot from 4-bit SD/eSD cards</td>
<td>page 14</td>
<td>A0</td>
<td>B0</td>
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<tr>
<td>DPF-639</td>
<td>The Boot ROM has a 4-second delay between each MMC/SD port probe if there is no card/device present.</td>
<td>page 14</td>
<td>A0</td>
<td>B0</td>
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<tr>
<td>DPF-539</td>
<td>MMC3 boot failures occur during non-power on resets</td>
<td>page 15</td>
<td>A0, B0</td>
<td>No Fix</td>
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<tr>
<td>DPF-585</td>
<td>The Boot ROM fails to initialize the DDR when using the NTIM header.</td>
<td>page 15</td>
<td>A0</td>
<td>B0</td>
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<tr>
<td>DPF-651</td>
<td>The Boot ROM fails to transfer control to DKB.</td>
<td>page 15</td>
<td>A0</td>
<td>B0</td>
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<tr>
<td>DPF-605</td>
<td>A total non-recoverable system lockup occurs when reading the Ethernet registers.</td>
<td>page 16</td>
<td>A0</td>
<td>B0</td>
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<tr>
<td>DPF-706</td>
<td>SPI boot failures occur when USBVBUS is supplied with 5V during the power-on sequence.</td>
<td>page 16</td>
<td>A0</td>
<td>Plan Fix - B0</td>
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<tr>
<td>DPF-703</td>
<td>The XD Controller returns double bit errors when reading from an XD card.</td>
<td>page 16</td>
<td>A0</td>
<td>B0</td>
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<tr>
<td>DPF-669</td>
<td>Invalid internal temperature sensor readings are returned when an external temperature sensor is connected to the RT_SEN signal.</td>
<td>page 16</td>
<td>A0</td>
<td>B0</td>
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<tr>
<td>DPF-698</td>
<td>The CCIC captures incorrect data when the VSYNC polarity is configured for active low.</td>
<td>page 17</td>
<td>A0</td>
<td>B0</td>
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<tr>
<td>DPF-699</td>
<td>The CCIC captures incorrect data when the HSYNC polarity is configured for active low.</td>
<td>page 17</td>
<td>A0, B0</td>
<td>No Fix</td>
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<tr>
<td>DPF-231</td>
<td>Immediate wakeup from system Sleep mode occurs when the USB wakeup is enabled.</td>
<td>page 17</td>
<td>A0, B0</td>
<td>No Fix</td>
</tr>
<tr>
<td>DPF-632</td>
<td>Random hangs occur when entering 624 MHz/156 MHz (Core/DDR) Operating mode</td>
<td>page 17</td>
<td>A0</td>
<td>B0</td>
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<tr>
<td>DPF-689</td>
<td>Clearing the CCIC_CTRL_0[EN] bit does not clear the frame number.</td>
<td>page 18</td>
<td>A0, B0</td>
<td>No Fix</td>
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<tr>
<td>DPF-753, DPF-668, DPF-653, DPF-435</td>
<td>Fractional divider for the 32K reference clock does not result in a 32.7681 kHz output frequency.</td>
<td>page 19</td>
<td>A0</td>
<td>B0</td>
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Table 5: Functional Errata Summary Table (Continued)

<table>
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<tr>
<th>Erratum Number</th>
<th>Erratum Description</th>
<th>Page</th>
<th>Affected Stepping</th>
<th>Fixed Stepping</th>
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<tbody>
<tr>
<td>DPF-762</td>
<td>The MPMU overheating temperature sensor interrupt does not generate an interrupt from the Interrupt Controller Unit (ICU)</td>
<td>19</td>
<td>A0, B0</td>
<td>No Fix</td>
</tr>
<tr>
<td>DPF-763</td>
<td>The MPMU Overheating temperature sensor interrupt status bit only occurs one time after a reset</td>
<td>19</td>
<td>A0</td>
<td>B0</td>
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<tr>
<td>DPF-764</td>
<td>Default PLL1 VCO frequency does not meet the PLL requirements for generating a 624 PLL1 reference clock.</td>
<td>19</td>
<td>A0</td>
<td>B0</td>
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<tr>
<td>DPF-782</td>
<td>The default output from PLL1 and PLL2 is going through a Phase Interpolator that is not initialized correctly.</td>
<td>20</td>
<td>A0</td>
<td>B0</td>
</tr>
<tr>
<td>DPF-749</td>
<td>Wrong instruction is executed when running out of cache.</td>
<td>21</td>
<td>A0</td>
<td>B0</td>
</tr>
<tr>
<td>DPF-743</td>
<td>Boot failures occur at cold temperatures at or below 0C if the Boot ROM attempts to initialize USB.</td>
<td>21</td>
<td>A0</td>
<td>B0</td>
</tr>
<tr>
<td>DPF-760</td>
<td>The PCIe controller does not get completely powered down.</td>
<td>22</td>
<td>A0</td>
<td>B0</td>
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<td>DPF-672</td>
<td>Boot failures occur when using SD/MMC devices with logical partitions.</td>
<td>22</td>
<td>A0</td>
<td>B0</td>
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<tr>
<td>DPF-717</td>
<td>A hang may occur when there is a non-cacheable lock-unlock Read-Write pair (SWAP Instruction) to DDR address space at the same time a Write burst from L2 Cache occurs.</td>
<td>22</td>
<td>A0</td>
<td>B0</td>
</tr>
<tr>
<td>DPF-758</td>
<td>CCIC End of Frame interrupt may not always occur when the sensor vertical size does not match expected value.</td>
<td>23</td>
<td>A0</td>
<td>B0</td>
</tr>
<tr>
<td>DPF-730</td>
<td>CCIC images not captured correctly at some line widths.</td>
<td>23</td>
<td>A0</td>
<td>B0</td>
</tr>
<tr>
<td>DPF-629</td>
<td>PCIe Link re-training with End Point requires an additional reset to reestablish the link</td>
<td>23</td>
<td>A0, B0</td>
<td>No Fix</td>
</tr>
<tr>
<td>DPF-470</td>
<td>System hangs occur while performing Dynamic Frequency Changes between Mode 2 (624/312 - PLL1) and any other Mode that uses PLL2.</td>
<td>24</td>
<td>A0</td>
<td>B0</td>
</tr>
<tr>
<td>DPF-701</td>
<td>Data corruption may occur when AXI bus peripherals are active during Dynamic Frequency Changes between operating modes.</td>
<td>24</td>
<td>A0</td>
<td>B0</td>
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</table>
### Table 5: Functional Errata Summary Table (Continued)

<table>
<thead>
<tr>
<th>Erratum Number</th>
<th>Erratum Description</th>
<th>Page</th>
<th>Affected Stepping</th>
<th>Fixed Stepping</th>
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</thead>
<tbody>
<tr>
<td>DPF-820</td>
<td>The number of MMC_CLK cycles after the last command has been sent prior to the next command (Ncc) does not meet JEDEC requirements.</td>
<td>page 24</td>
<td>A0, B0</td>
<td>No Fix</td>
</tr>
<tr>
<td>DPF-819</td>
<td>MMC Controller violates the JEDEC initialization sequence specification.</td>
<td>page 25</td>
<td>A0, B0</td>
<td>No Fix</td>
</tr>
<tr>
<td>DPF-781</td>
<td>The MI bit in the KPC_PC register will not be set when the matrix keypad is used to wake up from System Sleep.</td>
<td>page 25</td>
<td>A0, B0</td>
<td>No Fix</td>
</tr>
<tr>
<td>DPF-724</td>
<td>The EPD Controller does not function according to the specification when the ARMADA 16x processor is configured to use Mode 3.</td>
<td>page 25</td>
<td>A0</td>
<td>B0</td>
</tr>
<tr>
<td>DPF-732, DPF-779</td>
<td>USB and DMA failures occur after exiting System Sleep in any mode using a 312 MHz ACLK2 frequency.</td>
<td>page 26</td>
<td>A0</td>
<td>B0</td>
</tr>
<tr>
<td>DPF-858</td>
<td>FIFO data corruption occurs when the CCIC is configured to BT.656 during video playback</td>
<td>page 26</td>
<td>A0, B0</td>
<td>No Fix</td>
</tr>
<tr>
<td>DPF-775</td>
<td>The contents of the Main PMU Reset Status Register (MPMU_ARSR) are not reliable after a power-on reset.</td>
<td>page 26</td>
<td>A0, B0</td>
<td>No Fix</td>
</tr>
<tr>
<td>DPF-646</td>
<td>Data missing from USB Host when using a Device with multiple ISO (Isochronous) endpoints.</td>
<td>page 27</td>
<td>A0, B0</td>
<td>No Fix</td>
</tr>
<tr>
<td>DPF-895</td>
<td>TWSI transfers may hang when using FIFO mode.</td>
<td>page 27</td>
<td>A0, B0</td>
<td>No Fix</td>
</tr>
<tr>
<td>DPF-843</td>
<td>SDIO CARD_INT interrupt may be missed when the DAT1 signal is asserted by the external device.</td>
<td>page 27</td>
<td>A0, B0</td>
<td>No Fix</td>
</tr>
<tr>
<td>DPF-898</td>
<td>Resetting the SD Controller Data Port Logic stops the external clock.</td>
<td>page 28</td>
<td>A0, B0</td>
<td>No Fix</td>
</tr>
<tr>
<td>DPF-904</td>
<td>Wrong APMU interrupt status returned when using the read-to-clear method to clear the Interrupt Status Register (APMU_ISR).</td>
<td>page 28</td>
<td>A0, B0</td>
<td>No Fix</td>
</tr>
<tr>
<td>DPF-910</td>
<td>CompactFlash timing violations occur when using a 104 MHz functional clock for the CompactFlash Controller.</td>
<td>page 28</td>
<td>A0, B0</td>
<td>No Fix</td>
</tr>
<tr>
<td>DPF-928, DPF-929</td>
<td>Incorrect fuse values cause boot, frequency change, and frequency-related failures.</td>
<td>page 29</td>
<td>A0, B0</td>
<td>No Fix</td>
</tr>
</tbody>
</table>
### Table 5: Functional Errata Summary Table (Continued)

<table>
<thead>
<tr>
<th>Erratum Number</th>
<th>Erratum Description</th>
<th>Page</th>
<th>Affected Stepping</th>
<th>Fixed Stepping</th>
</tr>
</thead>
<tbody>
<tr>
<td>DPF-933</td>
<td>USB Host mode does not pass USB certification.</td>
<td>page 29</td>
<td>A0, B0</td>
<td>No Fix</td>
</tr>
<tr>
<td>DPF-678</td>
<td>Imaging data corruption occurs on specific modes of PXA16x CCIC output (UYV-422 planar or YUV-420 planar modes) and sensor output (YUV-422 packed mode) with horizontal resolution greater than 2046 pixels.</td>
<td>page 29</td>
<td>A0, B0</td>
<td>No Fix</td>
</tr>
<tr>
<td>DPF-596</td>
<td>Data loss or corruption when DMA is transferring data to or from DDR Controller when processor or DDR clock frequency is changed.</td>
<td>page 29</td>
<td>A0, B0</td>
<td>No Fix</td>
</tr>
<tr>
<td>DPF-633</td>
<td>After performing a read from a device connected to either NAND flash Chip Select 0 or 1 when (a) the BCH ECC logic detects an error and (b) the NAND Flash Command Buffer 0 auto read status bit is set, the NAND Flash Status Register will reflect &quot;page done&quot; and &quot;command complete&quot;</td>
<td>page 30</td>
<td>A0, B0</td>
<td>No Fix</td>
</tr>
<tr>
<td>DPF-678</td>
<td>DMA transfers from the CMOS Camera Interface Controller (CCIC) fail for frames wider than 2047 pixels when either the YUV 422 planar or YUV 420 planar output format is selected.</td>
<td>page 31</td>
<td>A0, B0</td>
<td>No Fix</td>
</tr>
<tr>
<td>DPF-824</td>
<td>The Temperature Sensor Controller Configuration Register Data Ready flag always shows that data from the Room Temperature Sensor is ready (TSC_CONFIG[DATA_RDY] = 1).</td>
<td>page 31</td>
<td>A0, B0</td>
<td>No Fix</td>
</tr>
<tr>
<td>DPF-932</td>
<td>A pending 64-bit write operation can be corrupted when the CPU-to-memory controller interface logic tries to merge a subsequent 32-bit or smaller write.</td>
<td>page 31</td>
<td>A0, B0</td>
<td>No Fix</td>
</tr>
<tr>
<td>DPF-966</td>
<td>DMA transfers from the CMOS Camera Interface Controller (CCIC) fail for certain frame sizes when either the YUV 422 planar or YUV 420 planar output format is selected.</td>
<td>page 32</td>
<td>A0, B0</td>
<td>No Fix</td>
</tr>
<tr>
<td>DPF-918</td>
<td>Code that enables the L2 cache after the L1 cache is already enabled can hang immediately depending on instruction sequencing and memory timing.</td>
<td>page 33</td>
<td>A0, B0</td>
<td>No Fix</td>
</tr>
<tr>
<td>Erratum Number</td>
<td>Erratum Description</td>
<td>Page</td>
<td>Affected Stepping</td>
<td>Fixed Stepping</td>
</tr>
<tr>
<td>----------------</td>
<td>-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------</td>
<td>------</td>
<td>------------------</td>
<td>----------------</td>
</tr>
<tr>
<td>DPF-968</td>
<td>When the DDR Controller receives a request to access memory that is in Pre-charge Powerdown or Active Powerdown mode, the request is granted prematurely and the access is corrupted.</td>
<td>page 33</td>
<td>A0, B0</td>
<td>No Fix</td>
</tr>
<tr>
<td>DPF-972</td>
<td>Setting the HI_SPEED_EN bit in the SD_HOST_CTRL register results in violations of the SD Association card timing specifications for high-speed Writes.</td>
<td>page 33</td>
<td>A0, B0</td>
<td>No Fix</td>
</tr>
<tr>
<td>DPF-973</td>
<td>Data corruption is seen when CompactFlash transfers are mixed with NAND Flash or Static Memory Controller activity on the Data Flash Interface (DFI)</td>
<td>page 34</td>
<td>A0, B0</td>
<td>No Fix</td>
</tr>
<tr>
<td>DPF-979</td>
<td>LCD pixel corruption that generally appears in the form of shifted pixels occurs for specific combinations of format, burst size, and update width when using a smart panel with DMA.</td>
<td>page 34</td>
<td>A0, B0</td>
<td>No Fix</td>
</tr>
<tr>
<td>DPF-353</td>
<td>The MX status bits in the Timer Status Register (TMR_SRx) do not reflect a match condition several clock cycles after entering the corresponding interrupt service routine.</td>
<td>page 35</td>
<td>A0, B0</td>
<td>None</td>
</tr>
<tr>
<td>DPF-978</td>
<td>The SD host controller reports an ADMA2 error when the physical address crosses a 4-Kbyte boundary.</td>
<td>page 36</td>
<td>A0, B0,</td>
<td>None</td>
</tr>
<tr>
<td>DPF-983</td>
<td>The processor fails to exit system sleep and locks up when the wait or interrupt mode (WFI) is entered too close to a wake-up event.</td>
<td>page 36</td>
<td>A0, B0</td>
<td>None</td>
</tr>
<tr>
<td>DPF-991</td>
<td>SD host controller transfers that are not a multiple of 4 bytes long do not complete.</td>
<td>page 37</td>
<td>A0, B0</td>
<td>None</td>
</tr>
<tr>
<td>DPF-1066</td>
<td>The JTAG SAMPLE instruction does not behave per IEEE 1149.1 specification.</td>
<td>page 37</td>
<td>A0, B0</td>
<td>None</td>
</tr>
<tr>
<td>DPF-1019</td>
<td>Cannot book with Hamming ECC from ONFI-compliant 8 NAND devices that have less than 4 KB of ONFI parameter pages.</td>
<td>page 37</td>
<td>A0, B0</td>
<td>None</td>
</tr>
</tbody>
</table>
5. Detailed Descriptions for Functional Errata

Refer to Section Table 5: "Functional Errata Summary Table" on page 6 to determine which errata are new to this report.

5.1 Functional Errata

<table>
<thead>
<tr>
<th>Relevant for:</th>
<th>A0, B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fixed in:</td>
<td>No Fix</td>
</tr>
<tr>
<td>Errata #:</td>
<td>DPF-321</td>
</tr>
<tr>
<td>Description:</td>
<td>USB: USB Suspend/Resume fails when PHY is suspended (USB_PORTSC[PHCD]=1).</td>
</tr>
<tr>
<td>Problem:</td>
<td>When the PHY is put into a low-power mode and the host sends a USB Resume interrupt, the device receives another Suspend interrupt instead of a Resume interrupt. Suspend interrupts continue until the host performs a reset as an error recovery.</td>
</tr>
<tr>
<td>Implication:</td>
<td>Software enters an error state until a reset occurs.</td>
</tr>
<tr>
<td>Workaround:</td>
<td>Software must be used to differentiate between a Suspend event and a RESUME command. When USB_INTR[SLE] is set to 1, the interrupt handler should read USB_PORTSC[LS] immediately upon entry to ensure the correct value is read. When the device controller enters a Suspend state from an Active state (USB_STS[SLI] = 1), the following values for USBPORTSC[LS] can be used to determine if the interrupt was from a Suspend event or RESUME command.</td>
</tr>
</tbody>
</table>

- **Suspend Event**: USB_PORTSC[LS] = 0b10
- **Resume Command**: USB_PORTSC[LS] = 0b01

5.2 Functional Errata

<table>
<thead>
<tr>
<th>Relevant for:</th>
<th>A0, B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fixed in:</td>
<td>No Fix</td>
</tr>
<tr>
<td>Errata #:</td>
<td>DPF-517</td>
</tr>
<tr>
<td>Description:</td>
<td>An exception occurs when reading the Host Control Version Register for SD2 and SD4 (SD2_HOST_CTRL_VER and SD4_HOST_CTRL_VER).</td>
</tr>
<tr>
<td>Problem:</td>
<td>Incorrect data being returned when issuing a 16-bit read to 0xD428_10FE and 0xD427_F0FE.</td>
</tr>
<tr>
<td>Implication:</td>
<td>Software can not read the SD Host Specification Number for SD2 and SD4.</td>
</tr>
<tr>
<td>Workaround:</td>
<td>Issue a 32-bit Read from 0xD428_10FE and 0xD427_F0FE to read the correct specification numbers for SD2 and SD4.</td>
</tr>
</tbody>
</table>

5.3 Functional Errata

<table>
<thead>
<tr>
<th>Relevant for:</th>
<th>A0, B0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fixed in:</td>
<td>No Fix</td>
</tr>
<tr>
<td>Errata #:</td>
<td>DPF-603</td>
</tr>
<tr>
<td>Description:</td>
<td>The WAKEUP1 bit in the MPU_AWUCRS register is asserted after a power-on reset.</td>
</tr>
<tr>
<td>Problem:</td>
<td>The WAKEUP1 bit in the Wakeup and Clock Resume Lines Status Register (MPU_AWUCRS) is asserted after a power on reset.</td>
</tr>
<tr>
<td>Implication:</td>
<td>The MPU will immediately wakeup from system Sleep mode.</td>
</tr>
<tr>
<td>Workaround:</td>
<td>Prior to entering system sleep, software must mask Wakeup1 by setting the WAKEUP1 bit in the Wakeup and Clock Resume Lines Mask Register (MPU_AWUCRM).</td>
</tr>
</tbody>
</table>
5.4 Functional Errata
Relevant for: A0
Fixed in: B0
Errata #: DPF-640
Description: A Test-Logic-Reset sequence does not automatically return the IDCODE in the Data Register.
Problem: The IDCODE Opcode is not sent to the Instruction Register when TMS is held high for at least 5 rising edges of TCK during a Test-Logic-Reset sequence and the IDCODE is not returned in the Data Register.
Implication: The Data Register does not return the IDCODE automatically after a Test-Logic-Reset sequence. Software that relies on the IDCODE to be available in the Data Register after a TLR will not read the correct IDCODE value.
Workaround: There are no workarounds to get the IDCODE in the Data Register after a TLR. To access these instructions, software must program the Instruction Register with the proper values (0x0FF for IDCODE, and 0x1FF for Bypass).

5.5 Functional Errata
Relevant for: A0, B0
Fixed in: No Fix
Errata #: DPF-642
Description: The TDI and TMS default pull state do not meet IEEE requirements.
Problem: The default pull state for TDI and TMS are with pulldown resistors enabled. IEEE requires that these signals be pulled high.
Implication: A Test-Logic-Reset sequence will not be entered automatically when 5 TCK rising edges occur during power on reset. Software must be used to enter TLR.
Workaround: Add external pull up resistors to TDI and TMS.

5.6 Functional Errata
Relevant for: A0, B0
Fixed in: No Fix
Errata #: DPF-643
Description: An extra bit is shifted into the Data Register when using Concatenate mode.
Problem: An extra bit is shifted out on TDO when reading from the Data Register.
Implication: The value expected on TDO will not be valid data if the extra bit is not accounted for.
Workaround: When Concatenate mode is required, software must parse of the LSB before processing the data. The XDB custom instruction below shows an IDCODE command for both the CPU IDCODE and Core IDCODE. The 0 in the LSB is the extra TDO bit which software must parse out before processing the Data Register.

```
custom "ir[14]=$(0ff.11101;dr[65]=0"
IR=00000000100010
DR=000100000100000100000100010011000000010000010
```

5.7 Functional Errata
Relevant for: A0, B0
Fixed in: No Fix
Errata #: DPF-577
Description: Burst assesses to DDR devices fail
Problem: By default, critical word first is enabled in the Marvell® Sheeva™ core and disabled in the DDR
controller.

**Implication:** Software is prevented from performing any burst accesses on the DDR device.

**Workaround:** Before enabling cache or performing burst accesses critical word first must be either enabled or disabled in both units.

To enable:
1. Set CPU_CONF[lf_cwf_en] to 0b1.
2. Program SDRAM_CNTRL_13 with 0x0000_0008

To disable:
1. Clear CPU_CONF[lf_cwf_en] to 0b0.
2. Program SDRAM_CNTRL_13 with 0x0000_0000

### 5.8 Functional Errata

**Relevant for:** A0

**Fixed in:** B0

**Errata #:** DPF-641

**Description:** The Boot ROM does not boot from 4-bit SD/eSD cards

**Problem:** The Boot ROM configures the MMC/SD port depending on what the card returns after a CMD1 is issued. If the SD/eSD card returns support for 4 bit, the controller fails to boot the processor.

**Implication:** The platform does not boot with 4-bit SD/eSD devices, however at run time OS level the SD/eSD port can be used in 4bit DMA mode.

**Workaround:** Using 1-bit SD/eSD devices will allow the processor to successfully boot. However, due to the initialization protocol, when a card returns that it is 4-bit capable, the controller is configured in 4-bit mode. Most cards will operate in 1-bit mode; however, there is no software workaround to force the device to return that it is 1-bit only; or to ensure the Boot ROM configures the SD Controller into 1-bit mode. Unless a 1-bit mode only device is used, there is no way to boot from SD/eSD.

### 5.9 Functional Errata

**Relevant for:** A0

**Fixed in:** B0

**Errata #:** DPF-639

**Description:** The Boot ROM has a 4-second delay between each MMC/SD port probe if there is no card/device present.

**Problem:** When an MMC or SD device is not present and the Boot ROM executes the probe sequence to read the NTIM header, there is a 4-second delay for each of the three MMC/SD probes. The Boot ROM does not read the status flag that is set when no card is present; instead, it times out after 4 seconds.

**Implication:** The Boot ROM executes the following probe sequence:

1. XIP Flash on nCS0
2. X16 NAND Flash
3. X8 NAND Flash
4. OneNAND & Flex OneNAND
5. SD/MMC devices on MMC3 (primary configuration) - CMD & CLK using MFP_8 & MFP_9
6. SD/MMC devices on MMC3 (secondary configuration) - CMD & CLK using MFP_35 & MFP_36
7. SD/MMC devices on MMC1
8. SPI Flash

Probe orders 5, 6 & 7 each have the 4 second delay. For example, if the system was to boot from boot device #7 as listed above - there will be an 8 second delay until the device is read by the Boot ROM.

**Workaround:** There is no workaround to eliminate the delays for MMC probing.
5.10 Functional Errata
Relevant for: A0, B0
Fixed in: No Fix
Errata #: DPF-653
Description: MMC3 boot failures occur during non-power on resets.
Problem: When the processor transitions through a soft reset state, such as Hibernate mode exit, the Boot ROM will begin the auto-probe sequence and toggle pins shared between the NAND and MMC Controllers. During the NAND probe, the DF_IO7 and DF_IO6 data signals will toggle the MMC3_CLK and MMC3_CMD signals, which can put the card/device in an unknown state.
Implication: The system will fail to boot from MMC3 (primary configuration - CMD & CLK using MFP_8 & MFP_9) after a soft reset such as Hibernate exit.
Workaround: Use the secondary MMC3 configuration with MMC3_CMD on MFP_35 and MMC3_CLK on MFP_36 when using a reset that does not power down and reset the MMC device. For designs using the primary MMC3 configuration, the MMC3 device must be put into Idle state prior to entering Hibernate mode.

5.11 Functional Errata
Relevant for: A0
Fixed in: B0
Errata #: DPF-585
Description: The Boot ROM fails to initialize the DDR when using the NTIM header.
Problem: The Boot ROM returns a CheckMemoryReliability failure after reading NTIM and will continue to loop forever.
Implication: The Boot ROM will fail to complete the boot process and the processor will hang.
Workaround: Use the secondary MMC3 configuration with MMC3_CMD on MFP_35 and MMC3_CLK on MFP_36 when using a reset that does not power down and reset the MMC device. For designs using the primary MMC3 configuration, the MMC3 device must be put into Idle state prior to entering Hibernate mode.

5.12 Functional Errata
Relevant for: A0
Fixed in: B0
Errata #: DPF-651
Description: The Boot ROM fails to transfer control to DKB.
Problem: When the Boot ROM downloads the DKB the NTIM header is loaded to the wrong address, which blocks the download of the remaining images.
Implication: Image download failures occur when using WTPTP.
Workaround: Include two boot loaders in the NTIM, one with ID "DKBI" and on with ID "OBMI" and download both. The second image must be dropped with WTPDownload. An updated WTPTP version is also required.
5.13 Functional Errata
Relevant for: A0
Fixed in: B0
Errata #: DPF-605
Description: A total non-recoverable system lockup occurs when reading the Ethernet registers.
Problem: When software tries to read any of the Ethernet registers while the Ethernet DMA process is in progress, the Ethernet Mac fails to respond to the Read request, which results in a system hang.
Implication: The Ethernet Controller functionality cannot be guaranteed if software must read the registers while the Ethernet DMA process is in progress.
Workaround: Do not allow access to the Ethernet Controller registers while the DMA is active.

5.14 Functional Errata
Relevant for: A0
Fixed in: Plan Fix - B0
Errata #: DPF-706
Description: SPI boot failures occur when USBVBUS is supplied with 5V during the power-on sequence.
Problem: The detection of USBVBUS causes a USB interrupt while the boot ROM is transferring time critical data from the SPI device using the core. The data being transmitted from the SPI device is being lost when an overrun occurs while the boot ROM is servicing the USB interrupt. The boot ROM uses a time critical loop by using the core to transfer the data out of the FIFO. When the overrun occurs the SPI device continues to transfer data to the into the FIFO after it is full and not serviced till the interrupt is processed causing data loss during the transferred.
Implication: Data corruption may occur during SPI boot when USBVBUS is supplied during the power-on sequence, which will cause boot failures.
Workaround: Configure the NTIM header to disable the USB OTG port during the boot process to avoid the USB interrupt. To ensure software does not loose data while transferring from the SPI device DMA should be used to transfer the data from the SPI device. If an overrun occurs while the SPI device is being read, software must be used to stall the data while the FIFO is being emptied.

5.15 Functional Errata
Relevant for: A0
Fixed in: B0
Errata #: DPF-703
Description: The XD Controller returns double bit errors when reading from an XD card.
Problem: The XD controller implements XOR ECC for parity bits (even parity) instead of the required Exclusive NOR (odd parity) ECC.
Implication: Double bit errors will occur when reading from an XD card that was programmed with XNOR ECC. The data being read may be valid, but double bit errors will occur.
Workaround: Disable ECC when reading XD cards programmed with XNOR ECC. Correct software ECC (from xD specification) must be used to ensure the data is correct.

5.16 Functional Errata
Relevant for: A0
Fixed in: B0
Errata #: DPF-669
Description: Invalid internal temperature sensor readings are returned when an external temperature sensor is con-
When configuring the temperature sensor to read the internal temperature the connection to the RT_SEN signal remains connected and both sensors will return data to the temperature sensor. Inaccurate readings will be returned when reading the internal temperature.

**Problem:** Leave the RT_SEN signal floating

5.17 Functional Errata
Relevant for: A0
Fixed in: B0
Errata #: DPF-698
Description: The CCIC captures incorrect data when the VSYNC polarity is configured for active low.
Problem: When CCIC_CTRL_0[VPOL] is set to 0b1, the VCLK does not start properly, causing incorrect data to be captured.
Implication: Incorrect data is captured when using an active-low VSYNC signal (VPOL = 0b1).
Workaround: Use a sensor that requires an active-high VSYNC and clear VPOL to 0b0. For sensors using an active-low VSYNC, clear VPOL to 0b0 and add an inverter to the signal.

5.18 Functional Errata
Relevant for: A0, B0
Fixed in: No Fix
Errata #: DPF-699
Description: The CCIC captures incorrect data when the HSYNC polarity is configured for active low.
Problem: When CCIC_CTRL_0[HPOL] is set to 0b1, the VCLK does not start properly, causing incorrect data to be captured.
Implication: Incorrect data is captured when using an active-low HSYNC signal (HPOL = 0b1).
Workaround: Use a sensor that requires an active-high HSYNC and clear HPOL to 0b0. For sensors using an active-low HSYNC, clear HPOL to 0b0 and add an inverter to the signal.

5.19 Functional Errata
Relevant for: A0, B0
Fixed in: No Fix
Errata #: DPF-231
Description: Immediate wakeup from system Sleep mode occurs when the USB wakeup is enabled.
Problem: When WAKEUP5 in the MPMU Wakeup and Clock Resume Lines Mask Register (MPMU_AWUCRM) is set 0b1 to enable the USB wakeup source, the wakeup occurs immediately after entering system Sleep mode.
Implication: The MPMU can not operate in system Sleep mode when using USB as a wakeup source.
Workaround: Disable the USB wakeup by clearing the WAKEUP5 bit in the MPMU_AWUCRM register.

5.20 Functional Errata
Relevant for: A0
Fixed in: B0
Errata #: DPF-632
Description: Random hangs occur when entering 624 MHz/156 MHz (Core/DDR) Operating mode
Problem: In 624 MHz/156 MHz Operating mode using PLL2, the ACLK and DCLK clock generation hand-shaking
signals can become out of sync.

**Implication:** System hang may occur when entering 624/156 mode

**Workaround:** APMU_SYNC_MODE_BYPASS[D_A_CLK_SYNC_BYPASS] must be set to 1 prior to entering 624/156 mode.

### 0.0.1 Sync Mode Bypass Register (APMU_SYNC_MODE_BYPASS)

#### Instance Name Offset

<table>
<thead>
<tr>
<th></th>
<th>APMU_SYNC_MODE_BYPASS</th>
<th>0x00C8</th>
</tr>
</thead>
</table>

#### Bit Field

- **31:3 Reserved**
- **2** D_A_CLK_SYNC_BYPASS
- **1:0 Reserved**

#### Default


#### Table 6: Sync Mode Bypass Register (APMU_SYNC_MODE_BYPASS)

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:3</td>
<td>Reserved</td>
<td>RSV</td>
<td>--</td>
<td>Reserved. Always write 0. Ignore read value.</td>
</tr>
<tr>
<td>2</td>
<td>D_A_CLK_SYNC_BYPASS</td>
<td>R/W</td>
<td>0x0</td>
<td>Dclk/Aclk Sync Bypass</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 = DCLK/ACLK Sync Bypass &lt;p&gt;Bypass the SYNC mode</td>
</tr>
<tr>
<td>1:0</td>
<td>Reserved</td>
<td>RSV</td>
<td>--</td>
<td>Reserved. Always write 0. Ignore read value.</td>
</tr>
</tbody>
</table>

### 5.21 Functional Errata

**Relevant for:** A0, B0  
**Fixed in:** No Fix  
**Errata #:** DPF-689  
**Description:** Clearing the CCIC_CTRL_0[EN] bit does not clear the frame number.

**Problem:** When software clears the EN bit to update the configuration registers, the CCIC is disabled but the frame number is not reset. The data from the second frame is sent to y[1], u[1] and v[1] memory and the wrong Start of Frame (SOF1) and End of Frame (EOF1) interrupts are asserted.

**Implication:** Software expects to encounter y[0], u[0] and v[0] memory, SOF0 and EOF0 after disabling the CCIC will read invalid data.

**Workaround:** The CCIC Interrupt service routine (ISR) can be extended to track the most recently used buffer (0, 1, or 2) by enabling the SOF0, SOF1, and SOF2 interrupts and setting a tracking variable to record the last active frame buffer. On Disable / Re-enable, the next buffer to be used by the CCIC is the next buffer following the last active frame buffer. In a single buffer capture, software can elect to initialize all Y[x] DMA pointer registers to the same value to ensure that a dropped CI SOF interrupt would not cause the next used counter to be wrong and result in the CCIC writing camera data to an invalid memory region.
5.22 Functional Errata
Relevant for: A0, B0
Fixed in: B0
Errata #: DPF-753, DPF-668, DPF-653, DPF-435
Description: Fractional divider for the 32K reference clock does not result in a 32.7681 kHz output frequency.
Problem: The Fractional divider (12207/16) results in a 34.07881kHz reference clock instead of a 32.7681 kHz when using a 26 MHz PXTAL input clock.
Implication: Timing for peripherals relying on a 32.768 kHz reference clock will need to be adjusted for the 34.07881 kHz reference clock. The default value for the RTC trim register (RTC_TR) will not provide an accurate 1 Hz reference clock. The PWM output will not match the expected output when using the PWM with a 32.768 kHz reference clock (APBC_PWMx_CLK_RST[FNCLKSEL] = 0x1). When using a Hardware Timer with the 32k reference clock (TMR_CCR[CS_x] = 1) or 1 kHz (TMR_CCR[CS_x] = 0x2) the timer will be faster than expected.
Workaround: For the RTC controller a trim register (RTC_TR) use a value of 0x033A_851D to generate a 1 Hz reference clock. If an accurate PWM output is required software must program the registers according to the 34.07881 kHz reference clock, or use a 13 MHz reference clock (APBC_PWMx_CLK_RST[FNCLKSEL] = 0x0). Use a 3.25 MHz reference clock (TMR_CCR[CS_x] = 0x0) when using the hardware timers.

5.23 Functional Errata
Relevant for: A0, B0
Fixed in: No Fix
Errata #: DPF-762
Description: The MPMU overheating temperature sensor interrupt does not generate an interrupt from the Interrupt Controller Unit (ICU)
Problem: The MPMU Overheating interrupt is not sent directly to the ICU to generate an IRQ or FIQ interrupt.
Implication: Software expecting to receive an interrupt when an overheating temperature is reached will never get the interrupt.
Workaround: Software must poll the MPMU_OHCR status bits to determine when an interrupt occurs.

5.24 Functional Errata
Relevant for: A0
Fixed in: B0
Errata #: DPF-763
Description: The MPMU Overheating temperature sensor interrupt status bit only occurs one time after a reset
Problem: The MPMU Throttle/ Overheating Interrupt status bit (MPMU_OHCR[TIS]) only occurs one time. After clearing the status bit and re-arming the temperature sensor the status bit does not get set again.
Implication: Software expecting to make some system adjustments to reduce power after the first interrupt will never get a second interrupt if the overheating condition occurs a second time.
Workaround: If resetting the part after the first TIS interrupt occurs is not an option software must read the MPMU_OHCR[TSS] field to determine the temperature range and take the appropriate actions.

5.25 Functional Errata
Relevant for: A0
Fixed in: B0
Errata #: DPF-764
Description: Default PLL1 VCO frequency does not meet the PLL requirements for generating a 624 PLL1 reference
Problem: To meet the PLL VCO requirements the internal VCO frequency must be above 800 MHz. The default reset VCO frequency is 624 MHz (MPMU_FCCR[PLL1REFD]= 0x2, MPMU_FCCR[PLL1FBD] = 0x60, PLL1_REG1[VCODIV_SEL_SE] = 0x0) instead of the required 1.248 GHz. The 1.248 GHz VCO clock is divided by two inside the PLL to provide the correct 624 MHz output.

Implication: The duty cycle and jitter of PLL1 while running at default 624MHz cannot be guaranteed, which may have unintended consequences.

Workaround: During the initial boot process software must perform a Master Frequency Change to change PLL1’s VCO to operate within it designated range. The output frequency from PLL1 remains at 624 MHz after the MFC. The sequence of instructions required for a MFC is shown below.

1. Program the PLL1_REG1 register to configure the VCO and VCO divisor for proper operation at 1.248 GHz.
   a) MPMU_PLL1_REG1 = 0x91040664
2. Program the PLL1_REG2 register to configure the capacitor selection.
   a) MPMU_PLL1_REG2 = 0x84000030
3. Program the MPMU_FCCR register to enable an MFC after entering system sleep mode, and configure the PLL1REFD and PLL1FBD fields for a 1.248 GHz VCO frequency.
   a) MPMU_FCCR = 0x2000C290
4. Set up for and enter System Sleep mode.
   a) ICU_INT_CONF36 (0x90) = 0x5F (Unmask Interrupt 36 to automatically wakeup after MFC completes)
   b) APMU_IDLE_CFG (0x18) = 0x00300302
   c) MPMU_POCR (0x0C) = 0x70220
5. When the processor exits system sleep mode the PLL1 VCO frequency will be 1.248GHz and the output will be 624 MHz. After exiting system sleep software should clear interrupt 36.
   a) MPMU_APCR[INTCLR] = 1
   b) MPMU_APCR[INTCLR] = 0

5.26 Functional Errata
Relevant for: A0
Fixed in: B0
Errata #: DPF-782
Description: The default output from PLL1 and PLL2 is going through a Phase Interpolator that is not initialized correctly.

Problem: The default output of PLL1 and PLL2 is going through the SSC PI (SEL_VCO_DIFF = SEL_VCO_CLK_SE = 0) and should be direct from the VCO (SEL_VCO_DIFF = SEL_VCO_CLK_SE = 1) without using the PI. If the phase Interpolator logic is not properly initialized, its output frequency is unknown and its frequency may be as much as +/-5% off the VCO output.

Implication: When the PI is not reset properly the output of the PLL may be offset which causes the PLL to be off by ~5%. Peripherals such as the SSP and UART controllers that rely on an accurate clock source may have failures. The PI may also introduce additional cycle to cycle jitter resulting in degraded performance. A difference of up to 30 mV on Vmin for each operating mode also measured, causing larger part-to-part variance in vmin.

Workaround: During a frequency change where PLL2 is disabled software must program registers to have the PLL2 output be direct without going through the PI output. For PLL1 a master frequency change must be used to update the PLL registers to their correct values.

PLL1 Register Settings
1. Program the PLL1_REG1 register to configure the VCO and VCO divisor for proper operation at 1.248 GHz.
   a) MPMU_PLL1_REG1 = 0x91040664
2. Program the PLL1_REG2 register to configure the capacitor selection.
   a) \text{MPMU\_PLL1\_REG2} = 0x84000030

3. Program the MPMU\_FCCR register to enable an MFC after entering system sleep mode, and configure the
   PLL1REFD and PLL1FBD fields for a 1.248 GHz VCO frequency.
   a) \text{MPMU\_FCCR} = 0x2000C290

4. Set up for and enter System Sleep mode. An interrupt source (Hardware Timer) must be enabled to wake up from
   system sleep mode.

5. When the processor exits system sleep mode the PLL1 VCO frequency will be 1.248GHz and the output will be
   624 MHz.

**PLL2 Register Settings**

1. Disable PLL2 (PLL2CR[EN] = 0)

2. Program PLL2REFD and PLL2FBD in the PLL2 Control Register (PLL2CR). PLL2REFD and PLL2FBD values
   depend on the required output for PLL2.
   a) \text{PLL2CR} = 0x00007300 for 797 MHz PLL2 output

3. Program PLL2 Register 1 to set the correct settings for KVCO, VCO\_VRNG, VCO\_DIV\_SEL\_SE,
   VCO\_DIV\_SEL\_DIFF, VDDL, VDDM and ICP for the desired PLL2 output. Values depend on the required output
   for PLL2.
   a) \text{MPMU\_PLL2\_REG1} = 0x90020464 for 797 MHz PLL2 output

4. Program PLL2 Register 2 to set the correct settings for CAP\_SEL, RESET\_EXT, DIFFCLK\_EN,
   SEL\_VCO\_CLK\_SE, and SEL\_VCO\_CLK\_DIFF.
   a) 0x84000070 for 797 MHz PLL2 output.

5. Enable PLL2 (PLL2CR[EN] = 1)

6. Initiate Frequency Change.

### 5.27 Functional Errata

**Relevant for:** A0  
**Fixed in:** B0  
**Errata #:** DPF-749  
**Description:** Wrong instruction is executed when running out of cache.  
**Problem:** When using self modifying code accesses at the page boundary (address 1023), and the next address
is the first address of the next page (1024) the memory attribute is not loaded into the TLB. The access
request at 1023 gets the wrong outer cacheable bit and doesn't get sent to the L2 Cache and instead
gets sent directly to the bus.

**Implication:** When using self modifying code an instruction abort will occur when accessing page boundaries.  
**Workaround:** Clear the L2 Cache entry on the last entry of the page.

### 5.28 Functional Errata

**Relevant for:** A0  
**Fixed in:** B0  
**Errata #:** DPF-743  
**Description:** Boot failures occur at cold temperatures at or below 0C if the Boot ROM attempts to initialize USB.  
**Problem:** If the Boot ROM initializes USB, it programs a UTMI\_PLL[ICP] value (6) that may cause failures at tem-
peratures below 0C. Programming a lower UTMI\_PLL[ICP] value will avoid this problem. The recom-
manded value is 2. Note: this is only a problem at cold temperatures. Boot ROM reliably enables the
USB port at normal temperatures, which allows factory provisioning over USB.

**Implication:** If USB initialization is required, it should be done by the Boot Loader or OS software. Boot Loader and
OS software can use the correct UTMI_PLL[ICP] value and reliably enable USB at all temperatures.

**Workaround:** In the NTIM header add a USB package in the Reserved area to cause Boot ROM to skip USB initialization. After the part boots the boot loader software must program the UTMI_PLL[ICP] field to 2 to guarantee USB functionality at all temperatures. An example of an NTIM header for a SPI boot configuration that disables the USB port is shown below. The "Size of Reserved area in bytes" must reflect these extra 16 bytes. The packet count word that follows the Reserved Data id (0x4f505448) must also reflect this extra packet.

```
; packet that ensures the USB OTG port is NOT configured
0x00555342
0x00000010
0x44696666
0x00000001
```

### 5.29 Functional Errata

- **Relevant for:** A0
- **Fixed in:** B0
- **Errata #:** DPF-760
- **Description:** The PCIE controller does not get completely powered down.
- **Problem:** When the PCIE controller is held in reset, APMU_PCIE_CLK_RES_CTRL (0x100) = 0x00000000, the controller is not powered down completely.
- **Implication:** An extra 5mA of current on the AVDD_PCIE supply will be measured even when PCIE is not being used.
- **Workaround:** When using PCIE there is no workaround to eliminate the extra 5 mA of current when the controller is idle. In designs where PCIE is not being used all PCIE signals should be connected to VSS.

### 5.30 Functional Errata

- **Relevant for:** A0
- **Fixed in:** B0
- **Errata #:** DPF-672
- **Description:** Boot failures occur when using SD/MMC devices with logical partitions.
- **Problem:** When using SD/MMC devices that do not support hardware partitions and rely on logical (MSDOS) partitions, the NTIM header is located at offset 0x0 where the partition table should be located. When the OS is unable to read the correct partition table, the remaining boot process fails and the processor hangs.
- **Implication:** SD/MMC devices that require logical partitions will not boot properly.
- **Workaround:** Use an SD/MMC device that does not require a logical partition at offset 0x0 or an MMC device that supports physical partitioning.

### 5.31 Functional Errata

- **Relevant for:** A0
- **Fixed in:** B0
- **Errata #:** DPF-717
- **Description:** A hang may occur when there is a non-cacheable lock-unlock Read-Write pair (SWAP Instruction) to DDR address space at the same time a Write burst from L2 Cache occurs.
- **Problem:** The Read-Write pair is supposed to be atomic with no other traffic allowed on the bus between the read and write. When the SWAP instruction occurs, the bus arbiter between the PJ1 core and the DDR Controller does not get locked correctly. This may cause the bus to hang when the grant occurs to the other...
System hangs may occur when using the SWAP instruction to DDR address space.

**Workaround:**
Either disable the L2 Cache or use Writethrough mode for L2 Cache when using the SWAP instruction to DDR address space.

### 5.32 Functional Errata

**Relevant for:** A0

**Fixed in:** B0

**Errata #:** DPF-758

**Description:** CCIC End of Frame interrupt may not always occur when the sensor vertical size does not match expected value.

**Problem:** The EOF interrupt does not get triggered when the actual sensor vertical size is smaller than the programmed value (CCIC_IMG_SIZE[VSIZE]).

**Implication:** No EOF is generated to signal the end of frame.

**Workaround:** Do not program the vertical size (CCIC_IMG_SIZE[VSIZE]) to be less than what the sensor is providing.

### 5.33 Functional Errata

**Relevant for:** A0

**Fixed in:** B0

**Errata #:** DPF-730

**Description:** CCIC images not captured correctly at some line widths.

**Problem:** Data corruption occurs in memory when using line widths (CCIC_IMG_SIZE[HSIZE]) from 64 to 2048 with certain line width modulus. Depending on the image format and the modulus of the line width, the image data will be corrupted.

**Implication:** A limited number of line widths are supported.

**Workaround:** The image width field must be set to a multiple of 16 for all image capture types except RGB 888, which must be a multiple of 8.

### 5.34 Functional Errata

**Relevant for:** A0, B0

**Fixed in:** No Fix

**Errata #:** DPF-629

**Description:** PCIE Link re-training with End Point requires an additional reset to reestablish the link

**Problem:** After disabling the link with the end point the PCIE controller is disabled and does not enabled automatically.

**Implication:** The PCIE controller will reestablish connect with the link until a reset occurs.

**Workaround:** To reset the PCIE controller software must set the TX_DETECT_RX bit in the PCIE PHY Mac Control Enforce register.

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5.35 Functional Errata
Relevant for: A0
Fixed in: B0
Errata #: DPF-470
Description: System hangs occur while performing Dynamic Frequency Changes between Mode 2 (624/312 - PLL1) and any other Mode that uses PLL2.
Problem: Clocks are gated off and a handshaking signal in the clock gen is missed when the PLL sources are changed.
Implication: System hangs will occur while changing between Mode 2 and all modes using PLL2.
Workaround: Software must transfer to an intermediate mode 0 (156/156) before changing to the new operating mode.

5.36 Functional Errata
Relevant for: A0
Fixed in: B0
Errata #: DPF-701
Description: Data corruption may occur when AXI bus peripherals are active during Dynamic Frequency Changes between operating modes.
Problem: During a DFC the AXI clocks are stopped for seven clock cycles. Missing data may occur during AXI fabric transactions while the clocks are stopped, which will cause data corruption.
Implication: When AXI peripherals (DMA, NAND Controller, etc) are active during a DFC the missing data will cause data corruption failures.
Workaround: Software must ensure AXI peripherals are inactive during a DFC.

5.37 Functional Errata
Relevant for: A0, B0
Fixed in: No Fix
Errata #: DPF-820
Description: The number of MMC_CLK cycles after the last command has been sent prior to the next command (Ncc) does not meet JEDEC requirements.
Problem: A minimum of 8 clock cycles (Ncc) after the last command has been sent is required before the host can continue sending the next command. The MMC Controller waits only 2 MMC_CLK cycles before starting to send the next command.
Implication: Cards requiring a minimum of 8 clock cycles will fail to initialize.
Workaround: Set the SD_FIFO_PARAM[DIS_PAD_SD_CLK_GATE] (0x0E0) bit to 1.
### 5.38 Functional Errata

**Relevant for:** A0, B0  
**Fixed in:** No Fix  
**Errata #:** DPF-819  
**Description:** MMC Controller violates the JEDEC initialization sequence specification.  
**Problem:** The JEDEC MMC specification requires at least 74 clocks on the MMC_CLK signal prior to the first command. The MMC Controller does not support this portion of the specification.  
**Implication:** Some MMC cards may not initialize properly when inserted.  
**Workaround:** Set the MMC_CLK and MMC_CMD MFPs to their GPIO equivalent and use software to manually generate the required clock pattern. Then set the MFPs back to the MMC alternate functions before taking the MMC Controller out of reset.

### 5.39 Functional Errata

**Relevant for:** A0, B0  
**Fixed in:** No Fix  
**Errata #:** DPF-781  
**Description:** The MI bit in the KPC_PC register will not be set when the matrix keypad is used to wake up from System Sleep.  
**Problem:** When the processor is in the System Sleep mode, it can be configured to wake from a matrix key press. However, once the key is pressed, the Matrix Keypad Interrupt (MI) bit in the Keypad Control Register (KPC_PC) is not set as specified. Although the MI bit is not set, the keypad interrupt to the processor is generated correctly according to the specification.  
**Implication:** When polling the MI bit to determine when the matrix keypad is pressed, the software may get caught in an infinite loop. Also, when using the MI bit to determine if an interrupt was caused by the matrix keypad, the software will determine (erroneously) that the matrix keypad did not cause the interrupt.  
**Workaround:** For a software workaround, read the Keypad Matrix Key Register (KPC_MK) to determine a key press action. When reading this register, a bit being set indicates that a matrix key has been pressed. Software can use this data from the interrupt routine to determine if an interrupt was caused by the matrix keypad.

### 5.40 Functional Errata

**Relevant for:** A0  
**Fixed in:** B0  
**Errata #:** DPF-724  
**Description:** The EPD Controller does not function according to the specification when the ARMADA 16x processor is configured to use Mode 3.  
**Problem:** One feature of the EPD Controller is bus snooping so it can keep track of which pixels have changed since the last refresh. When using Mode 3, the internal timing path for the snoop logic is changed and causes the EPD Controller to function outside the specification, and occasionally stop functioning altogether.  
**Implication:** The EPD Controller cannot be used at the higher frequencies when the ARMADA 16x processor is configured for Mode 3.  
**Workaround:** There are two workarounds for this issue:  
1. The preferred workaround is to use a non-zero value in the Frame Buffer Base Register (FB_BASE) located at offset 0x0050 in the EPD Control registers.  
2. A second workaround involves raising the Vmin value for the processor. This issue is eliminated if the Vmin is raised to about 1.117V.
5.41 Functional Errata
Relevant for: A0
Fixed in: B0
Errata #: DPF-732, DPF-779
Description: USB and DMA failures occur after exiting System Sleep in any mode using a 312 MHz ACLK2 frequency.
Problem: Handshaking occurs between ACLK and ACLK2 using the CLK_EN signal during low power transitions. When entering or System Sleep the CLK_EN signal does not get reset properly when ACLK2 = 312 MHz, which causes data corruption during the handshaking.
Implication: USB and DMA failures will occur when exiting or System Sleep in any mode using a 312 MHz ACLK2 (APMU_CCR[BUS2_CLK_DIV] = 0) frequency.
Workaround: Prior to entering or System Sleep modes software must initiate a Dynamic Frequency change to switch ACLK2 to 156 MHz (APMU_CCR[BUS2_CLK_DIV] = 1) instead of 312 MHz (APMU_CCR[BUS2_CLK_DIV] = 0). After exiting idle software must initiate a Dynamic Frequency change to switch the ACLK2 frequency back to 312 MHz.

5.42 Functional Errata
Relevant for: A0, B0
Fixed in: No Fix
Errata #: DPF-858
Description: FIFO data corruption occurs when the CCIC is configured to BT.656 during video playback
Problem: When CCIC is configured to BT.656 mode during video playback, CCIC expects:
• That Start of Active Video (SAV) ends with an End of Active Video (EAV)
• That a blank-start during a data stream ends with a blank-end
Implication: FIFO data corruption will cause failures when configured to BT.656 given these conditions:
• If a device is used that ends an SAV with a blank-end
• If a device is used that ends a blank-start with an EAV
Workaround: Use a device that ends an SAV with an EAV or one that ends a blank-start with a blank-end.

5.43 Functional Errata
Relevant for: A0, B0
Fixed in: No Fix
Errata #: DPF-775
Description: The contents of the Main PMU Reset Status Register (MPMU_ARSR) are not reliable after a power-on reset.
Problem: After power-on reset, the MPMU_ARSR expected value should be 0x0000_0000. Due to a timing dependency between the fuses and the MPMU_ARSR register updates, the Power On Reset (POR), External Master Reset (EMR) and Watchdog Timer Reset (WDTR) may be set falsely after a power-on reset. There are no processor dependencies on the contents of this register. These status bits are used only by software to determine the source of the reset.
Implication: Software cannot use the POR field in the MPMU_ARSR register as a reliable way of determining that the reset was caused by a power-on reset.
Workaround: After a power-on reset, the contents of the MPMU_ARSR are either 0x0000_0000 or 0x0000_0007. Software must use 0x0000_0000 or 0x0000_0007 as an indication of a POR when reading the MPMU_ARSR register.
5.44 Functional Errata
Relevant for: A0, B0
Fixed in: No Fix
Errata #: DPF-646
Description: Data missing from USB Host when using a Device with multiple ISO (Isochronous) endpoints.
Problem: If conducting multiple concurrent bidirectional ISO USB transfers when running the OTG Controller in Host mode and connected to a USB device with multiple ISOC endpoints, the ISO USB traffic may stop for a number of micro-frames at the beginning of the transfer started.
Implication: In the beginning of multiple concurrent ISO transfer, data is missed when either of these cases occurs:
1. Multiple ISOC endpoint concurrent transfer with unidirectional traffic and high bandwidth (above 391 MBits/s total bandwidth).
2. Multiple ISOC endpoint concurrent transfer with bidirectional traffic with low bandwidth (total bandwidth below 20 Mbits/s, each endpoint has an average Maximum Packet Size (MPS) of above 146 bytes).
Workaround: The speed of the transfers must be limited when connecting to a device with multiple ISO endpoints and bidirectional concurrent ISO traffic.

5.45 Functional Errata
Relevant for: A0, B0
Fixed in: No Fix
Errata #: DPF-895
Description: TWSI transfers may hang when using FIFO mode.
Problem: While operating in FIFO mode (TWSI_CR[FIFOEN] = 1), the TWSI Controller updates the TWSI_CR register during transfers. The transfer hangs if software writes to the TWSI_CR while the controller is clearing TWSI_CR[TB] bit.
Implication: TWSI hangs may occur while using FIFO mode when software writes to the TWSI_CR register.
Workaround: Software must avoid writing to the TWSI_CR register while the TWSI unit is performing a data transfer. Software must wait for the Transaction Begins field (TXBEGIN) in the TWSI_CR register to be cleared by the TWSI unit after the transaction has stopped, and the Transaction Done field (TXDONE) in the TWSI_SR register to be set, before programming the TWSI_CR register.

5.46 Functional Errata
Relevant for: A0, B0
Fixed in: No Fix
Errata #: DPF-843
Description: SDIO CARD_INT interrupt may be missed when the DAT1 signal is asserted by the external device.
Problem: The SD Controller may miss the CARD_INT interrupt when software sets the Card Interrupt Enable bit (CARD_INT_EN) in the SD_NORMAL_INT_STATUS_EN register. When the SDIO device asserts DAT1 low the SD Controller does not generate the card interrupt.
Implication: Interrupt requests from the external SDIO device may not be detected or serviced.
Workaround: There are two possible workarounds for this issue.
1. For devices that do not require a free-running clock: Software must issue a soft reset to the data port logic by setting the SW_RST_DAT bit in the Timeout Control/Software Reset (SD_TIMEOUT_CTRL_SW_RESET) Register after the SDIO transaction completes without error.
2. For devices that require a free-running clock: Software must issue a soft reset to the data port logic by setting the SW_RST_DAT bit in the Timeout Control/Software Reset (SD_TIMEOUT_CTRL_SW_RESET) Register after the SDIO transaction completes without error. The steps in Errata DPF-898 must then be applied to start the clocks.
5.47 Functional Errata
Relevant for: A0, B0
Fixed in: No Fix
Errata #: DPF-898
Description: Resetting the SD Controller Data Port Logic stops the external clock.
Problem: When software sets the SD_RST_DAT bit in the Timeout Control/Software Reset Register (SD_TIMEOUT_CTRL_SW_RESET) to reset data port logic, the clock to the external device (MMCx_CLK) will stop.
Implication: Failures may occur when using an external device that needs a continuous clock.
Workaround: If an external device requires continuous clocks (example: most SDIO devices), after programming SW_RST_DAT software must re-enable the clocks by first detaching the CMD signal from the SD bus, issuing a dummy CMD0, and attaching the CMD signal to the SD bus. CMD0 is recommended because it offers the shortest transaction.

Note
To prevent the external device from receiving a command that, depending on its state, may not be valid, Marvell recommends that software reconfigure the SD_CMD MFPR as a GPIO output high signal before sending the command. Software should then restore the SD_CMD MFPR to the SD_CMD alternate function when the transaction completes.

5.48 Functional Errata
Relevant for: A0, B0
Fixed in: No Fix
Errata #: DPF-904
Description: Wrong APMU interrupt status returned when using the read-to-clear method to clear the Interrupt Status Register (APMU_ISR).
Problem: When reading the APMU_ISR register the Status Register is cleared before software can read the actual contents of the register when using the read-to-clear (APMU_IRWC[FC_INTR_IRST] = 1) method to clear the APMU_ISR interrupt status bits.
Implication: Software using the read-to-clear method for clearing the Status Register hangs while waiting for the status bits to return to an active-interrupt state (0b1).
Workaround: Use the Write-0-to-Clear method (APMU_IRWC[FC_INTR_IRST] = 0b0) for clearing the APMU_ISR status bits.

5.49 Functional Errata
Relevant for: A0, B0
Fixed in: No Fix
Errata #: DPF-910
Description: CompactFlash timing violations occur when using a 104 MHz functional clock for the CompactFlash Controller.
Problem: When using a 104 MHz functional clock source (APMU_CF_CLK_RES_CTRL[CF_CLK_SEL] = 0x3) the CE Hold and Address Hold timing requirements are violated.
Implication: Data corruption/hang may occur when the using a 104 MHz CompactFlash Controller clock.
Workaround: Use a maximum CF Controller functional clock of 78 MHz (APMU_CF_CLK_RES_CTRL[CF_CLK_SEL] = 0x2).
5.50 Functional Errata

Relevant for: A0, B0

Fixed in: No Fix

Errata #: DPF-928, DPF-929

Description: Incorrect fuse values cause boot, frequency change, and frequency-related failures.

Problem: When VDD_CORE ramp rate is slower than 10 mV/µs, the fuse values may not be sensed with the correct values. The appropriate fuse values may not read by the boot ROM causing boot failures. Fuses that are used to configure PLLs and frequency settings may also be read wrong, causing frequency change or frequency-related failures.

Implication: Failures caused by incorrect fuse reading may occur with designs that do not support a power supply with a fast enough ramp rate on VDD_CORE.

Workaround: There are two possible workarounds to ensure proper functionality of fuses after a power-on sequence occurs when using a ramp rate slower than 10 mV/µs on VDD_CORE.

1. Delay the start of the PXTAL_IN input until after VDD_CORE has ramped to a minimum of 0.9V.
   - Marvell recommends using an oscillator that is enabled after VDD_CORE has ramped.
   - As long as VDD_M ramps after VDD_CORE, VDD_M can be used to enable the oscillator.
   - If the VDD_CORE supply outputs a power-good signal as a notification that the supply has fully ramped, this signal can be used to enable the oscillator.

2. Connect JTAG_SEL to a signal that is high (VDD_IO3) while RESET_IN_N is asserted and low when RESET_IN_N is de-asserted.
   - Marvell recommends connecting JTAG_SEL to the RESET_IN_N input source through an inverter.
   - EXT_WAKEUP must be low at reset with a weak pulldown.
   - JTAG_SEL must be connected to ground to use the Watch Dog Timer (WDT) during normal operation.

5.51 Functional Errata

Relevant for: A0, B0

Fixed in: No Fix

Errata #: DPF-933

Description: USB Host mode does not pass USB certification.

Problem: While using Host mode, violations occur on minimum TX-to-TX inter-packet delay required for USB certification. The Host Controller provides 80 bit times while USB certification requires 88 bit times. Actual functionality of Host mode is not impacted.

Implication: Certification tests on Host mode will not pass.

Workaround: None

5.52 Functional Errata

Relevant for: A0, B0

Fixed in: No Fix

Errata #: DPF-678

Description: Imaging data corruption occurs on specific modes of PXA16x CCIC output (UYV-422 planar or YUV-420 planar modes) and sensor output (YUV-422 packed mode) with horizontal resolution greater than 2046 pixels.

Problem: CCIC data transfer fails when capturing under the following three conditions:

- The sensor outputs YUV-422 packed mode
- The horizontal resolution is greater than 2046 pixels
- PXA16x CCIC outputting in YUV-422 planar or YUV-420 planar modes
Implication: Capturing images in the configuration described above will result in image data corruption.

Workaround: There is no known workaround for this issue. However, there are two possible solutions:

1. Use a sensor with a horizontal resolution configured to less than 2046 pixels.
2. Configure the CCIC interface to output data in YUV-422 packed mode.

5.53 Functional Errata
Relevant for: A0, B0
Fixed in: No Fix
Errata #: DPF-596
Description: If DMA is transferring data to or from the DDR Controller when the processor or DDR clock frequency is changed, data loss or corruption may occur that manifests itself as audio clicking and popping, incomplete LCD screen refresh, or write errors to files on NAND flash or USB mass storage devices.
Problem: The processor clock and the DDR clock must be phase-aligned, so synchronization between both clock must occur whenever the frequency of either is changed. This requires that the DDR SDRAM must be put into Self-Refresh mode until the processor and DDR clocks stabilize at the new frequency. In Self-Refresh mode, reads and writes to the DDR SDRAM are blocked by the DDR Controller. DMA read and write transactions to the DDR Controller may be abruptly stalled when the DDR SDRAM is in self-refresh mode, and this may result in corrupted data or FIFO overflow or under-run conditions. Observable signs of this include audio clicking or popping, incompletely rendered LCD screens, corrupted file writes to NAND flash or USB mass storage devices, etc.
Implication: Data corruption or a FIFO overflow/under-run condition may occur when the DMA attempts to access the DDR SDRAM while it is in self-refresh mode if either the processor or DDR clock frequency is changed.
Workaround: DMA traffic between the DDR SDRAM and other peripheral devices must be idled before any operation that changes the processor or DDR clock frequency. These transactions can be restarted when the frequency change operation is complete, the processor and DDR Controller clocks are stable, and the DDR SDRAM is taken out of Self-Refresh mode.

5.54 Functional Errata
Relevant for: A0, B0
Fixed in: No Fix
Errata #: DPF-633
Description: After performing a read from a device connected to either NAND flash Chip Select 0 or 1 when (a) the BCH ECC logic detects an error and (b) the NAND flash command Buffer 0 auto read status bit is set (NFC_NDCB0[AUTO_RS] = 1), the NAND flash Status Register will reflect "page done" and "command complete" for both chip selects (NFC_NDSR[CS0_PAGED] = NFC_NDSR[CS0_CMDD] = 1 and NFC_NDSR[CS1_PAGED] = NFC_NDSR[CS1_CMDD] = 1).
Problem: The auto read status feature allows the NAND Flash Controller to perform automatic status checking of program/erase operations. This feature is not necessary or supported for read operations and should not be enabled for such. When enabled, the NAND Flash Controller improperly sets the page done and command complete status bits for both chip selects after completing a read operation in which the BCH ECC logic detects an error.
Implication: In applications that use two NAND flash devices simultaneously, the improper setting of the "page done" and "command complete" status bits may make it difficult to determine in which NAND flash device an error is detected, possibly imposing additional software overhead and reducing read performance.
Workaround: The auto read status mechanism is intended for use only during Program and Erase operations. Leave it disabled by keeping NFC_NDCB0[AUTO_RS] = 0 during read operations.
5.55  Functional Errata
Relevant for:  A0, B0
Fixed in:  None
Errata #:  DPF-678
Description:  DMA transfers from the CMOS Camera Interface Controller (CCIC) fail for frames wider than 2047 pixels when either the YUV 422 planar or YUV 420 planar output format is selected.
Problem:  When the CCIC is configured to output data in YUV 422 planar or YUV 420 planar format (CCIC_CTRL_0[DOUTFMT] = 0 and CCIC_CTRL_0[YUVOUTFMT] = 0 or 5), DMA transfers fail if the sensor output is wider than 2047 pixels (CCIC_IMG_SIZE[HSIZE] > 0x07ff).
Implication:  When the CCIC is configured for the YUV 422 planar or YUV 420 planar output data formats, the received image will be corrupted if its width is greater than 2047 pixels.
Workaround:  Consider (a) using a CMOS image sensor that outputs images with a width of 2047 pixels or less or, (b) using the YUV 422 packed output data format (CCIC_CTRL_0[YUVOUTFMT] = 4).

5.56  Functional Errata
Relevant for:  A0, B0
Fixed in:  None
Errata #:  DPF-824
Description:  The Temperature Sensor Controller Configuration Register Data Ready flag always shows that data from the Room Temperature Sensor is ready (TSC_CONFIG[DATA_RDY] = 1).
Problem:  When the chip is first powered on, the room temperature sensor is disabled (TSC_CONFIG[TS_EN] = 0) and the data ready flag shows that no data is available (TSC_CONFIG[DATA_RDY] = 0). When the room temperature sensor is enabled, an analog-to-digital conversion is performed to retrieve the first temperature reading. When this data is available, the data ready flag is set (TSC_CONFIG[DATA_RDY] = 1), and another conversion is performed. While this and subsequent conversions take place, the data ready flag remains set (TSC_CONFIG[DATA_RDY] = 1), implying that data from a new sensor reading is available, even if a conversion is still in progress.
The data ready flag can only be cleared by a chip-level reset or by removing power from and then re-applying power to the chip only. No other hardware or software mechanism will clear the flag.
Implication:  The data ready flag remains stuck at 1 after the first reading from the room temperature sensor is output by the analog-to-digital converter, so there is no way to know when updated temperature data is available.
Workaround:  Although the data ready flag is never updated after the first temperature reading is complete, the analog-to-digital converter continues running at the frequency selected by the TSC_CONFIG[CLK_SEL] bit and outputs new data every 52 or 60 converter clock cycles if TSC_CONFIG[MODE_SEL] = 0 or 1, respectively. A timer-driven interrupt service routine running at this rate or less can be used to read the room temperature sensor output a regular intervals.

5.57  Functional Errata
Relevant for:  A0, B0
Fixed in:  None
Errata #:  DPF-932
Description:  A pending 64-bit write operation can be corrupted when the CPU-to-Memory Controller interface logic tries to merge a subsequent 32-bit or smaller write.
Problem:  When the CPU-to-Memory Controller interface is presented with a merging opportunity where the in-
coming write is 32 bits or less and the merge FIFO holds a pending write of 64 bits, the upper 32 bits of the pending write can be dropped. These bits are dropped, corrupting the write, because the size bit that denotes the pending 64-bit write in the FIFO entry is improperly changed to specify a 32-bit write.

**Implication:** The CPU-to-Memory Controller interface write FIFO is intended to improve performance, but in certain cases where a 64-bit write is followed by a 32-bit or smaller write, the FIFO merging logic corrupts the pending 64-bit write.

**Workaround:** Set the AFIFO_MERGE_DIS bit in the CPU_CONF register at 0xD428_2C08 to disable the CPU-to-Memory Controller write FIFO merging logic. Write merge opportunities occur infrequently, and the performance impact will be minimal.

### 5.58 Functional Errata

**Relevant for:** A0, B0  
**Fixed in:** None  
**Errata #:** DPF-966  
**Description:** DMA transfers from the CMOS Camera Interface Controller (CCIC) fail for certain frame sizes when either the YUV 422 planar or YUV 420 planar output format is selected.

**Problem:** When the CCIC is configured to output data in YUV 422 planar or YUV 420 planar format (CCIC_CTRL_0[DOUTFMT] = 0 and CCIC_CTRL_0[YUVOUTFMT] = 0 or 5), DMA transfers fail for the following frame sizes:

<table>
<thead>
<tr>
<th>YUV422 Planar</th>
<th>YUV420 Planar</th>
</tr>
</thead>
<tbody>
<tr>
<td>X (pixels)</td>
<td>Y (pixels)</td>
</tr>
<tr>
<td>240</td>
<td>160</td>
</tr>
<tr>
<td>200</td>
<td>320</td>
</tr>
<tr>
<td>240</td>
<td>320</td>
</tr>
<tr>
<td>400</td>
<td>304</td>
</tr>
<tr>
<td>304</td>
<td>400</td>
</tr>
<tr>
<td>240</td>
<td>480</td>
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<tr>
<td>720</td>
<td>480</td>
</tr>
<tr>
<td>720</td>
<td>576</td>
</tr>
<tr>
<td>600</td>
<td>800</td>
</tr>
<tr>
<td>1,366</td>
<td>768</td>
</tr>
<tr>
<td>900</td>
<td>1,440</td>
</tr>
<tr>
<td>1,200</td>
<td>1,600</td>
</tr>
<tr>
<td>1,680</td>
<td>1,050</td>
</tr>
<tr>
<td>1,200</td>
<td>1,920</td>
</tr>
<tr>
<td>1,324</td>
<td>2,012</td>
</tr>
<tr>
<td>1,704</td>
<td>2,272</td>
</tr>
<tr>
<td>1,648</td>
<td>2,464</td>
</tr>
<tr>
<td>2,032</td>
<td>2,560</td>
</tr>
<tr>
<td>2,000</td>
<td>3,008</td>
</tr>
</tbody>
</table>

**Implication:** When the CCIC is configured for the YUV 422 planar or YUV 420 planar output data formats, the received image will be corrupted for the frame sizes listed above.
Workaround: Consider (a) using a CMOS image sensor with a frame size not listed above, (b) using the YUV 422 packed output data format (CCIC_CTRL_0[YUVOUTFMT] = 4), or (c) allowing the CCIC to begin a new DMA transfer immediately following the previous one (CCIC_CTRL_1[DMAREQCTRL] = 1).

5.59 Functional Errata
Relevant for: A0, B0
Fixed in: None
Errata #: DPF-918
Description: Code that enables the L2 cache after the L1 cache is already enabled can hang immediately, depending on instruction sequencing and memory timing.
Problem: Instruction alignment, sequencing, and timing are critical when enabling the CPU caches. There are certain cases in which enabling the L2 cache when the L1 caches are already enabled interferes with proper data transfer and results in the CPU core hanging. Code executing from memories connected to the Static Memory Controller is especially but not exclusively prone to this condition.
Implication: Cache enabling code must be executed in a specific order to avoid stalling the CPU core.
Workaround: The L1 caches must not be enabled before the L2 cache. Either enable both caches with the same write to CP15 Control Register 0 or first enable the L2 cache, then enable the L1 caches to avoid a possible CPU hang.

5.60 Functional Errata
Relevant for: A0, B0
Fixed in: None
Errata #: DPF-968
Description: When the DDR Controller receives a request to access memory that is in Pre-charge Powerdown or Active Powerdown mode, the request is prematurely granted and the access is corrupted.
Problem: To reduce power dissipation, the DDR Controller takes advantage of the power management modes defined in the JEDEC DDR specifications and places the DDR memories into the Pre-charge Powerdown or Active Powerdown modes when applicable.

The DDR Controller uses a 4-entry queue to hold access requests. When a request to access memory that is in one of the JEDEC-defined Powerdown modes is the first entry in this queue, there is a case in which the user-programmed SDRAM timing can result in the DDR Controller processing this request before it has actually signaled the memory to exit Powerdown mode, causing the access to fail.
Implication: Access failures that occur when the DDR Controller does not release the DDR memories in a timely fashion may cause program crashes or data corruption.
Workaround: The tXP field in SDRAM Timing Register 3 must be set to a value of 3 or greater. Do not leave this field at or set to its default value of 2, even for memories running at lower frequencies (such as LPDDR-200) for which tXP = 2 would be a valid setting.

5.61 Functional Errata
Relevant for: A0, B0
Fixed in: None
Errata #: DPF-972
Description: Setting the HI_SPEED_EN bit in the SD_HOST_CTRL register results in violations of the SD Association card timing specifications for high-speed Writes.
Problem: The SD Host Controller Specification defines the high-speed enable bit (SD_HOST_CTRL Bit 2) such that it is to be set for cards that support and are operated at clock frequencies above 25 MHz and up to 50 MHz (52 MHz for MultiMediaCards) so that the controller CMD and DAT[3:0] lines are driven on the rising edge of CLK instead of the falling edge.
On PXA168 family devices, however, setting this bit drives CMD and DAT[3:0] such that SD card hold time specifications are violated, preventing card operation at clock frequencies above 25 MHz.

**Implication:** Card operation at clock frequencies above 25 MHz is not supported when HI_SPEED_EN=1.

**Workaround:** Do not set HI_SPEED_EN. Even when HI_SPEED_EN = 0, the timing of CMD and DAT[3:0] is such that card operation at clock frequencies up to 50 MHz (52 MHz for MultiMediaCards) is supported without violating hold timing specifications.

---

### 5.62 Functional Errata

**Relevant for:** A0, B0  
**Fixed in:** None  
**Errata #:** DPF-973  
**Description:** Data corruption is seen when CompactFlash transfers are mixed with NAND flash or Static Memory Controller activity on the data flash interface (DFI).

**Problem:** The DFI is a multiplexed bus interface with an arbitration mechanism that allows the CompactFlash Controller (CFC) NAND Flash Controller (NFC), and Static Memory Controller (SMC) to perform data transfers across a single shared set of pins. When NFC or SMC transfers are mixed with CFC transfers, the data read from or written to the CompactFlash card can be corrupted because the DFI arbitration mechanism does not work properly with the CFC.

**Implication:** Data read from or written to a CompactFlash card can be corrupted if transfers from the SNC or NFC are allowed to occur simultaneously.

**Workaround:** Implement a semaphore locking mechanism such that when the CFC is to read or write data, it acquires an exclusive lock on use of the DFI, effectively blocking the NFC or SMC until its transfers are complete. In turn, NFC or SMC activity must block CFC transfers until complete. While this workaround effectively prevents use of the DFI arbitration mechanism if CompactFlash is used in conjunction with the NFC or the SMC, it does not apply to mixed NFC and SMC traffic. In this situation, the arbitration mechanism works as expected.

---

### 5.63 Functional Errata

**Relevant for:** A0, B0  
**Fixed in:** None  
**Errata #:** DPF-979  
**Description:** LCD pixel corruption that generally appears in the form of shifted pixels occurs for specific combinations of format, burst size, and update width when using a smart panel with DMA.

**Problem:** LCD Controller Reads are always aligned to 8-byte boundaries, and alignment is based on the read request address (X position). If the number of bytes to be read is larger than the burst size (64 bytes), the read request must be split so that it does not cross a burst boundary.

Where bits [2:0] of the Read request address are 3'b100 or 3'b110, the offset required to perform a properly aligned burst is incorrectly calculated, the Read begins from the wrong address, and any part of the Read request that crosses a burst boundary ends up misaligned and returns the wrong data.

**Implication:** When the following conditions are true:

\[
\text{Total bytes per line} + (X \text{ Position} \times \text{Bytes per Pixel}) \mod 8 > 64....
\]

...misaligned LCD Read requests occur, resulting in image corruption via pixel shifting. This problem occurs only when DMA is used and the line to be updated is (a) 30 or 31 pixels wide with a color depth of 2 bytes per pixel, or (b) 20 or 21 pixels wide with a color depth of 3 bytes per pixel.

**Workaround:** The two primary options for dealing with this are to (a) split the image update into left and right halves...
such that the line width is less than 30/31 pixels or 20/21 pixels in 2 or 3 bytes per pixel color depths, respectively, or (b) increase the width of the image update by 1 or 2 pixels such that the total bytes per line updated is > 64.

Furthermore, when using a smart panel, updates can be made in Master mode (via DMA) or Slave mode (via CPU Writes). Using DMA for small updates with a smart panel is not particularly efficient, so simply performing the updates via CPU Writes avoids this condition and is unlikely to impact performance in any meaningful way.

### 5.64 Functional Errata

**Relevant for:** A0, B0  
**Fixed in:** None  
**Errata #:** DPF-353  
**Description:** The Mx status bits in the Timer Status Registers (TMR_SRx) do not reflect a match condition several clock cycles after entering the corresponding interrupt service routine.

**Problem:** For timer comparator matches, the logic that sets the Mx status bits is delayed by multiple clock cycles relative to the interrupt request logic. It is entirely possible to enter a timer interrupt service routine before the comparator match condition is propagated to the corresponding Mx bit in TMR_SRx.

**Implication:** In a timer interrupt service routine, the Mx status bit corresponding to the comparator with the match condition is not set as expected. Software that clears the interrupt request by writing to the corresponding TCLRx bit in the Timer Interrupt Clear Register (TMR_ICRx) will not actually clear the interrupt request if it does not wait for the pending Mx bit to set.

**Workaround:** Wait for the corresponding Mx bit in TMR_SRx to set before writing to TMR_ICRx to clear a timer match event interrupt request.

### 5.65 Functional Errata

**Relevant for:** A0, B0  
**Fixed in:** None  
**Errata #:** DPF-978  
**Description:** The SD host controller reports an ADMA2 error when the physical data address crosses a 4-Kbyte boundary.

**Problem:** The ARM AMBA AXI specification mandates that no burst may cross a 4-Kbyte boundary. AXI masters and slaves and the fabrics connecting masters to slave must comply with this limitation or risk erroneous behavior.

The SD host controllers on the PXA16x do not properly comply with this limitation. If...

(ADMA2 physical starting address modulo 4096) + ADMA2 transfer length > 4096

...then the transfer specified by such a descriptor will fail and the SD host controller will set the ADMA_LEN_ERR bit in the SD_ADMA_ERROR_STATUS register.

**Implication:** The PXA16x SD host controllers cannot complete ADMA2 transfers that cross a 4-Kbyte boundary.

**Workaround:** Several means of avoiding this kind of transfer failure are possible: (1) Align transfers to 4-Kbyte boundaries by splitting them into two or more transfers that do not cross 4-Kbyte boundaries. (2) Use SDMA, which properly handles transfers that cross 4-Kbyte boundaries, instead of ADMA2. (3) Like SDMA, programmed I/O (PIO) transfers are not subject to this limitation.
5.66 Functional Errata
Relevant for: A0, B0
Fixed in: None
Errata #: DPF-983
Description: The processor fails to exit system sleep and locks up when the wait for interrupt mode (WFI) is entered too close to a wake-up event.
Problem: If PMU recognition of the CPU entering WFI occurs one oscillator clock (one 26 MHz period or approximately 38.46 ns) after PMU recognition of a wake-up event, the PMU will get stuck in the PLL off state and fail to wake from system sleep. Only a power-on reset can recover the system from this state.
Implication: The PXA16x will never recover from system sleep mode if a wake-up event is recognized by the PMU one oscillator clock cycle before the PMU recognizes a CPU request to enter wait for interrupt mode.
Workaround: There are only two practical cases in which a wake-up event can occur before the CPU enters WFI:

1. An OS timer is programmed with such a short delay that it initiates a wake-up event before the CPU can actually request entrance into wait for interrupt mode.
2. Two or more wake-up sources are used in a system such that wake-up events and WFI requests overlap (e.g. timer and DMA).

In the first case, make the OS timer delay of sufficient length so that the wake-up event can be enabled and the CPU can enter WFI well before the timer wake-up event occurs. Be sure that a new timer wake-up event cannot occur while recovering from the previous timer wake-up and before re-entering WFI.

The second case is more complicated because it covers situations such as maintaining audio playback during what is otherwise a system-wide (e.g. not just the processor) low-power mode. This may involve DMA wake-ups used to maintain an audio buffer in conjunction with routine timer wake-ups.

Short of avoiding WFI altogether during low-power audio playback and running at the lowest possible frequency and voltage (mode 0 = 156 MHz and 0.9V), no specific guidelines can be provided to completely eliminate the very remote possibility of nearly simultaneous PMU recognition of a wake-up event and WFI request. The recommendation for the first case still applies such that the software that processes entrance to and exit from WFI should attempt to selectively enable and disable wake-ups so that the time at which wake-up events can possibly occur is well past PMU recognition of WFI entrance.

5.67 Functional Errata
Relevant for: A0, B0
Fixed in: None
Errata #: DPF-991
Description: SD host controller transfers that are not a multiple 4 bytes long do not complete.
Problem: For any transfer, whether PIO, SDMA, or ADMA2, for which the length is not a multiple of 4 bytes, the PXA16x SD host controller will not set the XFER_COMPLETE flag in the SD_NORMAL_INT_STATUS register. This violates the SD Association Host Controller Specification version 2.0 and later which imposes no such limitation.
Implication: The PXA16x SD host controller does not comply with the SD Association Host Controller Specification which does not require that PIO, SDMA, or ADMA2 transfers be a multiple of any fundamental size like 4 bytes.
Workaround: Guarantee that transfers are always a multiple of 4 bytes. The Marvell Linux SD host controller driver is compiled with the “quirks” options to account this limitation.
5.68 Functional Errata
Relevant for: A0, B0
Fixed in: None
Errata #: DPF-1066
Description: The JTAG SAMPLE instruction does not behave per IEEE 1149.1 specification.
Problem: SAMPLE is a mandatory JTAG instruction that returns the logic state of digital input/output pins connect-
ed to the boundary scan register (BSR). The opcode for SAMPLE (0x0AC on the PXA16x) is also used
for the PRELOAD instruction, which allows test data for output pins to be pre-loaded into the BSR with-
out affecting normal operation of the device under test.

The SAMPLE instruction on the PXA16x is non-functional. After 0x0AC is clocked into the ARMADA 16x
on the TDI pin during the instruction register shift phase, the test access port (TAP) controller logic does
not enable the output of the BSR, which results in all 0s being driven on TDO pin during the data register
shift phase. Consequently, there is no way to read (sample) pins connected to the BSR during normal
operation.

PRELOAD is affected by the same problem. While test data can be loaded into the BSR (pre-load) to
drive output pins in response to the EXTEST instruction, nothing is ever shifted out. This means that if
it is part of a boundary scan chain that includes other devices, no data can ever be passed through the
PXA16x during the data register shift phase following the PRELOAD (SAMPLE) instruction.

Implication: The PXA16x is not 100% compliant with the IEEE 1149.1 specification because it does not properly im-
plement the mandatory SAMPLE/PRELOAD instruction.

Workaround: None

5.69 Functional Errata
Relevant for: A0, B0
Fixed in: None
Errata #: DPF-1019
Description: Cannot boot with Hamming ECC from ONFI-compliant x8 NAND devices that have less than 4 KB of
ONFI parameter pages.
Problem: Versions 1.0 and 2.0 of the ONFI specification define a parameter page data structure with 256 bytes of
information, at least three copies of which are required. Because of the order in which the PXA16x
probes and identifies NAND flash boot memories, an ONFI-compliant x8 device with less than 4 KB of
parameter pages (i.e. fewer than 16 copies) returns invalid data (usually 0xFF for all parameter page
bytes) when probed, is not properly identified, and is ignored by the boot ROM.

Implication: Hamming ECC cannot be used when booting from ONFI-compliant x8 NAND flash devices that return
less than 4 KB of parameter page data.

Workaround: Ideally, ONFI-compliant NAND flash devices that are programmed with 4 KB of parameter pages should
be used, but determining if this is the case may not be possible from manufacturer data sheets. Instead,
program ONFI-compliant x8 devices using BCH ECC, even when the manufacturer documentation
states that 1-bit of ECC per 528 bytes (8 bits wide) or 264 words (16 bits wide) of data, and therefore
Hamming ECC, is sufficient.
### 6. Documentation Change Summary

**Table 8: Summary of Documentation Changes**

<table>
<thead>
<tr>
<th>Number</th>
<th>Description</th>
<th>Document</th>
<th>Relevant Revision</th>
<th>Revision Fixed</th>
</tr>
</thead>
<tbody>
<tr>
<td>DPF-940</td>
<td>Multi-Function Pin Drive Strength section in Appendix A has incorrect settings for Fast IO pins drive strength.</td>
<td>Marvell® ARMADA PXA16x Applications Processor Family Software Manual (MV-S301544-00)</td>
<td>4.0A, 4.0B</td>
<td>Next Revision</td>
</tr>
<tr>
<td>7.3</td>
<td>Figure 60 in the Marvell® ARMADA 16x Applications Processor Family Software Manual is incorrect, making the NAND Flash device connected to ND_CS[1]n inaccessible.</td>
<td>Marvell® ARMADA 16x Applications Processor Family Software Manual</td>
<td>40A, 4.0B</td>
<td>None</td>
</tr>
<tr>
<td>7.4</td>
<td>Table 7 in the Marvell® ARMADA 16x Applications Processor Family Hardware Manual does not include an operating specification for the PCIe supplies.</td>
<td>Marvell® ARMADA 16x Applications Processor Family Hardware Manual</td>
<td>40A, 4.0B</td>
<td>None</td>
</tr>
<tr>
<td>7.5</td>
<td>The description of the SMC_CSADRMAPx register STADD field in Table 393 of the Marvell® ARMADA 16x Applications Processor Family Software Manual does not clearly identify which processor address bus bits correspond with the MSBs of the chip select starting address.</td>
<td>Marvell® ARMADA 16x Applications Processor Family Software Manual</td>
<td>4.0A, 4.0B</td>
<td>None</td>
</tr>
</tbody>
</table>
7. Detailed Descriptions for Documentation Changes

7.1 Documentation Change
Relevant for: Marvell® ARMADA PXA16x Applications Processor Family Software Manual (MV-S301544-00)
Revision: 4.0A, 4.0B
Fixed In: Next Revision
Errata #: DPF-940
Description: Multi-Function Pin Drive Strength section in Appendix A has incorrect settings for Fast IO pins drive strength.
Changes: Refer to A.1.1 “Multi-Function Pin Drive Strength” for updated Fast IO drive strength settings.

A.1.1 Multi-Function Pin Drive Strength

Two different configurations are available for setting the drive strength for each multi-function pin. For normal IO pins, MFPR_<xx11:10> are used for each pin. For Fast IO pins, the combination of MFPR_58[11:10] and MFPR_56[11:10] are used to determine the P and N drive strengths for the entire block of fast IO pins (MFPR_<56:85>). Refer to Table 9 for example drive strength settings for the fast IO pins using PMOS and NMOS drivers. Refer to Table 10 for MFPR bit assignments used to program the PMOS and NMOS drivers.

Table 9: Fast IO Multi-Function Pin Drive Strengths

<table>
<thead>
<tr>
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</thead>
<tbody>
<tr>
<td>00</td>
<td>00</td>
<td>1X</td>
</tr>
<tr>
<td>01</td>
<td>01</td>
<td>2X</td>
</tr>
<tr>
<td>10</td>
<td>10</td>
<td>3X</td>
</tr>
<tr>
<td>11</td>
<td>11</td>
<td>4X</td>
</tr>
</tbody>
</table>

Table 10: ZPR and PNR MFPR Assignments

<table>
<thead>
<tr>
<th>ZPR/ZNR</th>
<th>MFPR Bit Assignments</th>
</tr>
</thead>
</table>

Note
Refer to “Electrical Specifications” in the Marvell® ARMADA PXA16x Applications Processor Family Hardware Manual (MV-S301545-00) for current values for each drive strength setting.
7.2 Documentation Change
Relevant for: A0, B0
Errata #: None
Description: The PXA162 variant of the ARMADA 16x has a 64-Kbyte cache. On all ARMADA 16x family members, the L2 cache can be configured as 128 Kbytes of SRAM.
Changes: Table 2 changed to clarify cache and SRAM sizes.

Table 2: ARMADA 16x Applications Processor Family Hardware Features

<table>
<thead>
<tr>
<th>Feature Group</th>
<th>Feature</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Marvell® Sheeva™ Core and Internal Memory</td>
<td>Marvell® Sheeva™ Embedded CPU Technology</td>
<td>ARM® v5TE instruction set compliant</td>
</tr>
<tr>
<td></td>
<td>L1 Instruction and Data Cache</td>
<td>32 KB, 16 x 32 KB D$</td>
</tr>
<tr>
<td></td>
<td>L2 Cache</td>
<td>128 KB</td>
</tr>
<tr>
<td></td>
<td>Internal 8-bit ROM</td>
<td>Support boot from 8-bit NAND, 16-bit NAND, MMC, SD, OneNAND, SLC, MLC NAND, SSP, SPI, and XIP</td>
</tr>
</tbody>
</table>

This table entry is corrected to read as:

L2 Cache / SRAM

128 Kbytes (PXA162 = 64 Kbytes)

L2 cache is usable as 128 Kbytes of SRAM on all ARMADA 16x family members.

7.3 Documentation Change
Relevant for: A0, B0
Errata #: None
Description: Figure 60 in the Marvell® ARMADA 16x Applications Processor Family Software Manual is incorrect, making the NAND flash device connected to ND_CS[1]n inaccessible.
Changes: ND_IO[7:0] must be connected to I/O[7:0] on both devices. ND_IO[15:8] is left disconnected. See the corrected figure below:
Figure 60a: Typical NAND Flash Memory System Example Using ND_CS[0]n and ND_CS[1]n

The diagram below is added to show how two x8 NAND devices are connected to ND_CS[0]n such that they can be accessed in x16 fashion.

Figure 60b: Ganged Data Flash Memory System Example Using ND_CS[0]n
7.4 Documentation Change  
Relevant for: A0, B0  
Errata #: None  
Description: Table 7 in the Marvell® ARMADA 16x Applications Processor Family Hardware Manual does not include an operating specification for the PCIe supplies.  
Changes: Table 7 expanded to include min/typical/max specifications for AVDD_PCIE and AVDDT_PCIE as follows:

<table>
<thead>
<tr>
<th>Voltage Applied</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Value</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>AVDD_PCIE</td>
<td>1.7</td>
<td>1.8</td>
<td>1.9</td>
<td>V</td>
<td>—</td>
</tr>
<tr>
<td>AVDDT_PCIE</td>
<td>1.7</td>
<td>1.8</td>
<td>1.9</td>
<td>V</td>
<td>—</td>
</tr>
<tr>
<td>Tsystmp</td>
<td>—</td>
<td>—</td>
<td>25</td>
<td>mV/uS</td>
<td>—</td>
</tr>
</tbody>
</table>

7.5 Documentation Change  
Relevant for: A0, B0  
Errata #: None  
Description: The description of the SMC_CSADRMAPx register STADD field in Table 393 of the Marvell® ARMADA 16x Applications Processor Family Software Manual does not clearly identify which processor address bus bits correspond with the MSBs of the chip select starting address.  
Changes: Table 393 changed to clarify correspondence between STADD and the full 32-bit internal address bus.
<table>
<thead>
<tr>
<th>21:16</th>
<th>STADD</th>
<th>R/W</th>
<th>0x0</th>
<th>Start Address Bits</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Used to set the start address of the nCSx, default values are:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>nCS0 STADD0 = 0x00 = default for nCS0 start address is 0x8000_0000</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>nCS1 STADD1 = 0x10 = default for nCS1 start address is 0x9000_0000</td>
</tr>
</tbody>
</table>

**Note:** The start address default values are different for each nCSx. This field represents the top 6-bits of the start address, the rest of the start address bits are zeros.

This table entry is corrected to read as:

nCS0 STADD0 0x00 = default for nCS0 start address is 0x8000_0000
nCS1 STADD1 0x10 = default for nCS1 start address is 0x9000_0000

**Note:** The start address default values are different for each nCSx. From MSB to LSB, STADD corresponds with processor address bus bits ADDR[29] to ADDR[24] inclusively, such that:

\[
nCSx\text{ starting address} = 0x8000_0000 \times (\text{STADDx} \ll 24)
\]

For example, if STADD0 = 0x00 and STADD1 = 0x1F then...

\[
nCS0\text{ starting address} = 0x8000_0000 \times (0x00 \ll 24) = 0x8000_0000
\]

and

\[
nCS1\text{ starting address} = 0x9000_0000 \times (0x1F \ll 24) = 0x90FF_0000
\]
## 8. Specification Changes Summary

### Table 12: Summary of Specification Changes

<table>
<thead>
<tr>
<th>Number</th>
<th>Description</th>
<th>Change Revision</th>
</tr>
</thead>
<tbody>
<tr>
<td>DPF-275</td>
<td>Booting from MLC NAND is not supported on the R0 and S0 stepping.</td>
<td>Plan Support - A0</td>
</tr>
<tr>
<td>DPF-???</td>
<td>PXA16x product line moving from SAC105 to SAC305 solder ball material.</td>
<td>A0</td>
</tr>
<tr>
<td>DPF-572</td>
<td>EXT_WAKEUP being added as a wake-up source for Idle modes.</td>
<td>B0</td>
</tr>
<tr>
<td>DPF-747</td>
<td>GPIO being added as a wake-up source for idle modes.</td>
<td>B0</td>
</tr>
<tr>
<td>DPF-790</td>
<td>Additional operating modes added and register settings updated for each mode, and operating mode voltage levels for VDD_CORE have changed.</td>
<td>A0</td>
</tr>
<tr>
<td>DPF-594</td>
<td>Production support for Mode 4 (1.066 GHz)</td>
<td>Support - B0</td>
</tr>
<tr>
<td>DPF-802</td>
<td>Additional register fields in the CCIC Control 0 register have been added.</td>
<td>Support - B0</td>
</tr>
<tr>
<td>DPF-726</td>
<td>Additional boot support being added for Samsung and Hynix NAND devices.</td>
<td>Support - B0</td>
</tr>
<tr>
<td>DPF-740</td>
<td>Because all ARMADA 16X parts are auto probe, the delay in the probe of non-existent flash adds a significant amount of time to the resume-from-hibernate. As a result, when booting from eMMC, Boot ROM resume time is much longer than NAND, which may not meet all customer requirements.</td>
<td>Support - B0</td>
</tr>
<tr>
<td>DPF-845</td>
<td>Marvell® Sheeva™ Core Clock Gating disabled by default after reset.</td>
<td>B0</td>
</tr>
<tr>
<td>DPF-864</td>
<td>Boot ROM enables BCH ECC method for non-ONFI compliant NAND devices during the boot process.</td>
<td>B0</td>
</tr>
<tr>
<td>DPF-913</td>
<td>Additional register added to power down the PCIE Controller.</td>
<td>B0</td>
</tr>
<tr>
<td>DPF-914</td>
<td>APMU_PCR bit 29 must be set to 0b1.</td>
<td>B0</td>
</tr>
<tr>
<td>DPF-906</td>
<td>Application Subsystem Idle and Application Subsystem Sleep modes no longer supported.</td>
<td>A0, B0</td>
</tr>
<tr>
<td>DPF-839</td>
<td>L2 Cache Write Allocate mode is not supported.</td>
<td>A0, B0</td>
</tr>
<tr>
<td>DPF-915</td>
<td>Using Spread Spectrum Clocking (SSC) on PLL1 is not supported.</td>
<td>A0, B0</td>
</tr>
<tr>
<td>DPF-656</td>
<td>Room Temperature Sensor support added.</td>
<td>B0</td>
</tr>
<tr>
<td>DPF-936</td>
<td>Default MPMU register values have changed between A0 and B0.</td>
<td>B0</td>
</tr>
<tr>
<td>DPF-952</td>
<td>USB Host controller support being added to ARMADA 162</td>
<td>B0</td>
</tr>
<tr>
<td>DPF-411</td>
<td>Support for DDR3 has been added.</td>
<td>B0</td>
</tr>
<tr>
<td>DPF-958</td>
<td>The ARMADA 160 144 pin package is no longer supported.</td>
<td>ARMADA 160</td>
</tr>
</tbody>
</table>
Table 12: Summary of Specification Changes (Continued)

<table>
<thead>
<tr>
<th>Number</th>
<th>Description</th>
<th>Change Revision</th>
</tr>
</thead>
<tbody>
<tr>
<td>DPF-972</td>
<td>Setting the HI_SPEED_EN bit in the SD_HOST_CTRL register results in violations of the SD Association card timing specifications for high-speed Writes</td>
<td>A0, B0</td>
</tr>
<tr>
<td>9.23</td>
<td>The PXA162 variant of the ARMADA 16x processor has a 64-Kbyte cache. On all ARMADA 16x family members, the L2 cache can be configured as 128 Kbytes of SRAM.</td>
<td>A0, B0</td>
</tr>
<tr>
<td>9.24</td>
<td>The description of the CMOS Camera Interface Control Register 0 (CCIC_CTRL_0) Output Data Format (DOUTFMT) and Input Data Format (DINFMT) fields in Table 334 of the Marvell® ARMADA 16x Applications Processor Family Software Manual mistakenly states that the 0x2 encodings are reserved</td>
<td>A0, B0</td>
</tr>
</tbody>
</table>
9. Detailed Descriptions for Specification Changes

9.1 Specification Change
Relevant for: Plan Support - A0
Errata #: DPF-275
Description: Booting from MLC NAND is not supported on the R0 and S0 stepping.
Changes: The Boot ROM has been updated to include drivers to support MLC NAND devices.

9.2 Specification Change
Relevant for: A0
Errata #: DPF-???
Description: PXA16x product line moving from SAC105 to SAC305 solder ball material.
Changes: Change of solder ball material from SAC105 to SAC305 effective with builds starting on WW40'09 (for BGA only). SAC105 materials will be shipped as engineering samples until the supply is depleted. SAC305 with its higher silver content in the alloy (Sn-3Ag-0.5Cu) shows more resistance to coarsening of tin grains during thermal fatigue. Chapter 4 Package Information will be updated to reflect this change.

9.3 Specification Change
Relevant for: B0
Errata #: DPF-572
Description: EXT_WAKEUP being added as a wake-up source for Idle modes.
Changes: EXT_WAKEUP is being added to Alternate Function 0 on the EXT_WAKEUP signal. This function will serve as a wake-up source (WAKEUP3) for Idle modes including system sleep.

9.4 Specification Change
Relevant for: B0
Errata #: DPF-747
Description: GPIO being added as a wake-up source for idle modes.
Changes: The GPIO alternate function is being added as a wakeup source. This function will serve as a wake-up source (WAKEUP3) for Idle modes including system sleep.

9.5 Specification Change
Relevant for: A0
Errata #: DPF-790
Description: Additional operating modes added and register settings updated for each mode, and operating mode voltage levels for VDD_CORE have changed.
Changes: The 800/200 and 624/156 (PCLK/DCLK) operating modes have been added.

9.6 Specification Change
Relevant for: Support - B0
Errata #: DPF-594
Description: Production support for Mode 4 (1.066 GHz)
Changes: Current steppings do not support Modes 4 without exceeding the maximum allowable VDD_CORE volt-
age level. Support for Mode 4 is being added with VDD\_CORE less than 1.155V.

### 9.7 Specification Change

**Relevant for:** Support - B0  
**Errata #:** DPF-802  
**Description:** Additional register fields in the CCIC Control 0 register have been added.  
**Changes:** Refer to Table 13 for a description of the new VSYNC Edge Control EOF Control and register fields and bit locations.

#### Control 0 Register (CCIC\_CTRL\_0)

<table>
<thead>
<tr>
<th>Instance Name</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>CCIC_CTRL_0</td>
<td>0x003C</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit</th>
<th>SIFMODE</th>
<th>DSSCALE</th>
<th>VCLKPOL</th>
<th>VPOL</th>
<th>HPOL</th>
<th>Reserved</th>
<th>YUVENDFMT</th>
<th>YUVOUTFMT</th>
<th>RGBOUTEND</th>
<th>RGBINOUTFMT</th>
<th>DOUTFMT</th>
<th>DINFM</th>
<th>Reserved</th>
<th>RGBENDFMT</th>
<th>Reserved</th>
<th>EN</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
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<td>24</td>
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<tr>
<td>23</td>
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<td></td>
</tr>
</tbody>
</table>

**Table 13:** Control 0 Register (CCIC\_CTRL\_0)

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
</table>
| 23   | VEDGE\_CTRL | R/W  | 0x0   | **VSYNC Edge Control**  
This field controls the detection of VSYNC.  
0x0 = Detect at rising edge.  
0x1 = Detect at falling edge |
| 22   | EOF\_CTRL   | R/W  | 0x0   | **EOF Control**  
This field controls the generation of EOF (internal signal)  
0x0 = Based on VSIZE  
0x1 = Based on VSYNC  
Note: Program to 1 when VSIZE is bigger than actual number of line sent by CMOS sensor. |
| 21:18| Reserved    | RSVD | --    | Reserved. Always write 0. Ignore read value. |

### 9.8 Specification Change

**Relevant for:** Support - B0  
**Errata #:** DPF-726  
**Description:** Additional boot support being added for Samsung and Hynix NAND devices.  
**Changes:** Some Samsung and Hynix NAND devices do not follow the ONFI specifications for the 4th Read ID data. Additional support has been added to support the new Read ID data. For Samsung devices returning
0xD7 and 0xD5, and Hynix devices returning 0xD5 for the Device ID the boot ROM will use the correct parameters that are different than the generic ONFI standard.

9.9 Specification Change
Relevant for: Support - B0
Errata #: DPF-740
Description: Because all ARMADA 16X parts are auto probe, the delay in the probe of non-existent flash adds a significant amount of time to the resume-from-hibernate. As a result, when booting from eMMC, Boot ROM resume time is much longer than NAND, which may not meet all customer requirements.
Changes: The Boot ROM now recognizes optional resume-from-hibernate packages that may be located in the NTIM. When enabled, the package instructs the Boot ROM to skip the loading of the OBM from flash to non-volatile memory. Instead, the Boot ROM jumps directly to a DDR address specified through the TIM package as the jump location. This action saves hibernate time by skipping the loading of OBM and any pre-OS images. This option is functional only when the DDR is configured via the Boot ROM.

9.10 Specification Change
Relevant for: B0
Errata #: DPF-845
Description: Marvell® Sheeva™ Core Clock Gating disabled by default after reset.
Changes: The reset value for CPU_CONF[CG_BPASS0] has changed from 0x0 to 0x1 and Marvell® Sheeva™ core clock gating is disabled by default. Software must clear CG_BPASS0 to 0x0 to enable core clock gating to save power.

9.11 Specification Change
Relevant for: B0
Errata #: DPF-864
Description: Boot ROM enables BCH ECC method for non-ONFI compliant NAND devices during the boot process.
Changes: The Boot ROM attempts to read the ONFI Parameters from the NAND device. If byte 102 (Number of bits per cell) returns back a value greater than 1 the boot ROM will enable BCH ECC. If the NAND device is not ONFI compliant the boot ROM will automatically enable BCH. Designs with non-ONFI NAND devices with hamming ECC correction will need to take the following steps to boot properly.
1. Program the NTIM to Block 0 with BCH mode enabled. BCH may be enabled on a page boundary, so only pages contain NTIM must be programmed in this fashion to ensure that the Boot ROM can read out NTIM correctly.
2. Program all remaining pages and blocks using the Hamming method.
3. Add a GPIO package to the NTIM reserved area that will be interpreted by the Boot ROM and force the controller back in to using Hamming ECC method after reading in the NTIM using BCH. The Boot ROM will read in the OEM Boot Module using Hamming method. The details of setting up the TIM reserved area are as follows:
   Reserved Data:
   0x4F505448  <- Reserved Area
   0x00000002
   0x4750494F  <- GPIO
   0x00000014
   0x00000001  <- Update 1 value
   0xD4283028  <- NFC address
   0x00000000  <- Disable BCH
9.12 Specification Change
Relevant for: B0
Errata #: DPF-913
Description: Additional register added to power down the PCIE Controller.
Changes: Additional bits in the APMU_PCR register added to control power to the PCIE Controller. Refer to Table 14 for details on the new register bits.

0.0.2 Power Control Register (APMU_PCR)

<table>
<thead>
<tr>
<th>Instance Name</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>APMU_PCR</td>
<td>0x0000</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:28</td>
<td>Reserved</td>
<td>RSVD</td>
<td>--</td>
<td>Reserved. Always write 0. Ignore read value.</td>
</tr>
<tr>
<td>27</td>
<td>SetAlways</td>
<td>R/W</td>
<td>0x0</td>
<td>Must be set to 0b1</td>
</tr>
<tr>
<td>26:10</td>
<td>Reserved</td>
<td>RSVD</td>
<td>--</td>
<td>Reserved. Always write 0. Ignore read value.</td>
</tr>
<tr>
<td>9</td>
<td>PCIE_TCHIP_AN_OVR_EN</td>
<td>R/W</td>
<td>0x0</td>
<td>PCIe tchip_pd_ana override control</td>
</tr>
<tr>
<td>8</td>
<td>PCIE_TCHIP_AN_OVR</td>
<td>R/W</td>
<td>0x0</td>
<td>PCIe tchip_pd_ana override value (bit 9 needs to be set to take effect)</td>
</tr>
<tr>
<td>7</td>
<td>PCIE_MX_PDN_2_OVR_EN</td>
<td>R/W</td>
<td>0x0</td>
<td>mx_powerdown_i0_a[2] override control</td>
</tr>
<tr>
<td>6</td>
<td>PCIE_MX_PWDN_2_OVR</td>
<td>R/W</td>
<td>0x0</td>
<td>mx_powerdown_i0_a[2] override value (bit 7 needs to be set to take effect)</td>
</tr>
<tr>
<td>5</td>
<td>PCIE_MX_PDN_1_OVR_EN</td>
<td>R/W</td>
<td>0x0</td>
<td>mx_powerdown_i0_a[1] override control</td>
</tr>
</tbody>
</table>

Table 14: Power Control Register (APMU_PCR)
### 9.13 Specification Change

**Relevant for:** B0

**Errata #:** DPF-914

**Description:**
APMU_PCR bit 29 must be set to 0b1.

**Changes:**
On A0, the APMU_PCR bit 29 is a reserved bit that must be cleared to 0b0. On B0, this bit must be set to 0b1.

---

### 9.14 Specification Change

**Relevant for:** A0, B0

**Errata #:** DPF-906

**Description:**
Application Subsystem Idle and Application Subsystem Sleep modes no longer supported.

**Changes:**
The Application Subsystem Idle and Application Subsystem Sleep modes are no longer supported. Ignore references in the documentation or software to these low-power modes.

---

### 9.15 Specification Change

**Relevant for:** A0, B0

**Errata #:** DPF-839

**Description:**
L2 Cache Write Allocate mode is not supported.

**Changes:**
The L2 Cache Write Allocate mode (CPU_CONF[L2_WRITE_ALLOC] = 0x2) is not supported. Ignore any documentation references to L2 Cache Write Allocate mode.

---

### 9.16 Specification Change

**Relevant for:** A0, B0

**Errata #:** DPF-915

**Description:**
Using Spread Spectrum Clocking (SSC) on PLL1 is not supported.

**Changes:**
Using SSC on PLL1 is not supported. Ignore any documentation references to PLL1 SSC.
9.17 Specification Change
Relevant for: B0
Errata #: DPF-656
Description: Room Temperature Sensor support added.
Changes: The Room Temperature Sensor Controller has been added to read the external temperature as well as internal die temperature.

9.18 Specification Change
Relevant for: B0
Errata #: DPF-936
Description: Default MPMU register values have changed between A0 and B0.
Changes: Refer to Table 15 for a list of MPMU registers and the A0 and B0 default values.

<table>
<thead>
<tr>
<th>MPMU Register</th>
<th>A0 Default Value</th>
<th>B0 Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>PLL1 Register 1 (MPMU_PLL1_REG1)</td>
<td>0x1001_0264</td>
<td>0x9104_0664</td>
</tr>
<tr>
<td>PLL1 Register 2 (MPMU_PLL1_REG2)</td>
<td>0x8200_0000</td>
<td>0x8400_0030</td>
</tr>
</tbody>
</table>

9.19 Specification Change
Relevant for: B0
Errata #: DPF-952
Description: USB Host controller support being added to ARMADA 162
Changes: Support for the USB Host controller is being added to the ARMADA 162 package.

9.20 Specification Change
Relevant for: B0
Errata #: DPF-411
Description: Support for DDR3 has been added.
Changes: Ball V14 has changed from Vss to nDDRRESET to support the DDR3 reset signal requirement.

9.21 Specification Change
Relevant for: ARMADA 160
Errata #: DPF-958
Description: The ARMADA 160 144 pin package is no longer supported
Changes: Ignore references to this package.

9.22 Specification Change
Relevant for: A0, B0
Errata #: DPF-972
Description: Setting the HI_SPEED_EN bit in the SD_HOST_CTRL register results in violations of the SD Association card timing specifications for high-speed Writes
Changes: Description of the HI_SPEED_EN bit changed to indicate that it should not be set but that operation at clock frequencies above 25 MHz and up to 50 MHz (52 MHz for MultiMediaCards) is still supported.
This value should read: “Do not set this bit to one. Doing so causes timing for the CMD and DAT[3:0] signals to violate specifications. Proper operation with correct timing is achieved at clock frequencies above 25 MHz and up to 50 MHz (52 MHz for MultiMediaCards) when HI_SPEED_EN = 0.

Changes:

9.23 Specification Change
Relevant for: A0, B0
Errata #: None
Description: The PXA162 variant of the ARMADA 16x has a 64-Kbyte cache. On all ARMADA 16x family members, the L2 cache can be configured as 128 Kbytes of SRAM.
Changes: Table 2 changed to clarify cache and SRAM sizes.
9.24 Specification Change
Relevant for: A0, B0
Errata #: None
Description: The description of the CMOS Camera Interface Control Register 0 (CCIC_CTRL_0) Output Data Format (DOUTFMT) and Input Data Format (DINFMT) fields in Table 334 of the Marvell® ARMADA 16x Applications Processor Family Software Manual mistakenly states that the 0x2 encodings are reserved.
Changes: The feature list for the CMOS Camera Interface Controller states that capture and output in raw Bayer mode is supported. Table 334 is updated as follows to reflect this change:

<table>
<thead>
<tr>
<th>Feature Group</th>
<th>Feature</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Marvell® Sheeva™ Core and Internal Memory</td>
<td>Marvell® Sheeva™ Embedded CPU Technology</td>
<td>ARM® v6TE instruction set compliant</td>
</tr>
<tr>
<td>L1 Instruction and Data Cache</td>
<td>32 KB, IS + 32 KB, DS.</td>
<td></td>
</tr>
<tr>
<td>L2 Cache</td>
<td>128 KB</td>
<td></td>
</tr>
<tr>
<td>Internal Boot ROM</td>
<td>Support boot from 8-bit NAND, 16-bit NAND, MMC, SD, OneNAND, SLC, MLC NAND, SSP SPI, and XII</td>
<td></td>
</tr>
</tbody>
</table>

This table entry is corrected to read as:

L2 Cache / SRAM
128 Kbytes (FXA162 = 64 Kbytes)
L2 cache is usable as 128 Kbytes of SRAM on all ARMADA 16x family members.