

# Brightlane<sup>™</sup> Q6223 Central Switch

12-port Automotive Ethernet switch with integrated 1000BASE-T1 PHYs and MACsec

P/N MV-Q6223

### **Overview**

The Brightlane™ Q6223 (MV-Q223) is a secure, managed Automotive Ethernet switch designed for use in numerous applications, including as a central switch in zonal network architectures. It offers 90 Gbps of non-blocking switching capacity and features a wide array of advanced security features. The device is a member of the fourth generation of Marvell Automotive Ethernet switches.

The 12-port switch includes two integrated IEEEE 802.3-compliant 1000/100BASE-T1 PHYs, 2x RGMII/MII/RMII, 4x multi-speed 2.5 Gbps SerDes (2.5G/1Gbps) and 8x multispeed 10 Gbps SerDes (10G/5G/2.5G/1Gbps). Additionally, two of the 10G SerDes can be configured as a PCIe Gen3 x2 interface.

The port interface options offer flexible configurations for connectivity to external devices, such as 2.5/5/10GBASE-T1 PHYs, or uplinks to host SoCs. This makes the device ideal for in-vehicle networking (IVN) applications, such as advanced driver assist systems (ADAS), zonal control modules, and central gateways. The MV-Q6223 includes a high-performance dual core ARM® R52 CPU that operates in lockstep, with dedicated on-chip memory to support Time Sensitive Networking (TSN) protocols such as Precision Time Protocol (PTP) and security firewall to protect from external malicious attacks.

The switch incorporates advanced security features including 802.1AE MACsec, which provides link security to prevent man-in-the- middle attacks; and a Denial of Service (DoS) engine.

A patented, enhanced TCAM implementation for deep packet inspection (DPI) filters and classifies over 4,000 IPv4/IPv6 flows, and trusted boot functionality secures the vehicle network.

An embedded hardware security module (HSM) enhances device security by supporting secure and encrypted boot and performs key management for features such as MACsec.

512 Entry TCAM (Ingress & Egress)				Arm Dual Core R52 (Lockstep) with 1280KB SRAM							
IPv4/IPv6 Filtering (4K flows)				eHSM with Arm M3							
Queue Controller				4 Mb Packet Memory							
8-Level QoS per port				4K MAC Addresses, 4K VLANs						JTAG	
Switching Engine								PLL	$\leftrightarrow$		
Layer 3 Static Routing				AVB / TSN							
802.1AS & IEEE 1588/PTP								SMI/SPI			
802.1AE MACSec							SMI PHY	↔			
2.5G SerDes 100/ 1000B- T1 1 x MUX	2.5G RGMII/ SerDes XMII	2.5G RGMII/ SerDes XMII	10G SerDes	10G SerDes	10G SerDes	10G SerDes	10G SerDes	10G SerDes	2 x 10G SerDes or 1 x PCIe (2-lanes, 2 physical funcations)	EEPROM Interface	$\leftrightarrow$
1	1	1	1	1	1	1	1	1	<u> </u>		
	(Ingress IPv4/IPv6 Filte Queue C 8-Level Q Layer 3 Stat	(Ingress & Egress) IPv4/IPv6 Filtering (4K flows) Queue Controller 8-Level QoS per port Layer 3 Static Routing 2.56 100/ SerDes 100/ T1 2.56 RGMII/ xMII	(Ingress & Egress) IPv4/IPv6 Filtering (4K flows) Queue Controller 8-Level QoS per port Switchin Layer 3 Static Routing 802.1AS & IE 802.1AE 802.1AE 802.1AE	(Ingress & Egress)  IPv4/IPv6 Filtering (4K flows) Queue Controller 8-Level QoS per port Layer 3 Static Routing Egres 802.1AS & IEEE 158 802.1AE MACSe 2.56 1000/B- T1 SerDes RGMII/ SerDes RGMII/ 106 SerDes	(Ingress & Egress)       IPv4/IPv6 Filtering (4K flows)       Image: Controller and the controlle	(Ingress & Egress)       w         IPv4/IPv6 Filtering (4K flows)          Queue Controller 8-Level QoS per port          SerDes       Static Routing         Layer 3 Static Routing       802.1AS & IEEE 1588/PTP         SerDes       1000/ 1000B- T1         SerDes       RGMII/ XMII         SerDes       RGMII/ SerDes	(Ingress & Egress)       with 1280         IPv4/IPv6 Filtering (4K flows)       IPv4/IPv6 Filtering (4K flows)       IPv4/IPv6 Filtering (4K flows)         Queue Controller 8-Level QoS per port       IPv4/IPv6 Filtering (4K flows)       IPv4/IPv6 Filtering (4K flows)         IPv4/IPv6 Filtering (4K flows)       IPv4/IPv6 Filtering (4K flows)       IPv4/IPv6 Filtering (4K flows)       IPv4/IPv6 Filtering (4K flows)         IPv4/IPv6 Filtering (4K flows)       IPv4/IPv6 Filtering (4K flows)       IPv4/IPv6 Filtering (4K flows)       IPv4/IPv6 Filtering (4K flows)         IPv4/IPv6 Filtering (4K flows)       IPv4/IPv6 Filtering (4K flows)       IPv4/IPv6 Filtering (4K flows)       IPv4/IPv6 Filtering (4K flows)         IPv4/IPv6 Filtering (4K flows)       IPv4/IPv6 Filtering (4K flows)       IPv4/IPv6 Filtering (4K flows)       IPv4/IPv6 Filtering (4K flows)         IPv4/IPv6 Filtering (4K flows)       IPv4/IPv6/IPv6/IPv6/IPv6/IPv6/IPv6/IPv6/IPv6	(Ingress & Egress)       with 1280KB SRA         IPv4/IPv6 Filtering (4K flows)       eHSM with Arm I         Queue Controller 8-Level QoS per port       state A Mb Packet Mem 4K MAC Addresses, 4H         Layer 3 Static Routing       switch SRA         Layer 3 Static Routing       south SerDes         SerDes       1000/ 11         SerDes       RGMII/ SerDes         SerDes       RGMII/ SerDes         SerDes       RGMII/ SerDes         SerDes       RGMII/ SerDes         SerDes       RGMII/ SerDes         SerDes       RGMII/ SerDes	(Ingress & Egress)       with 1280KB SRAM         IPv4/IPv6 Filtering (4K flows)       eHSM with Arm M3         Queue Controller 8-Level QoS per port       # Mb Packet Memory 4K MAC Addresses, 4K VLANs         Layer 3 Static Routing       Switching         Kale       Static Routing         SerDes       1000/ 11000B- T1         SerDes       RGMII/ SerDes         RGMII/ 106       106 SerDes       10	with 1280KB SRAMWith 1280KB SRAMIPv4/IPv6 Filtering (4K flows)eHSM with Arm M3Queue Controller 8-Level QoS per port4 Mb Packet Memory 4K MAC Addresses, 4K VLANsSwitching Serber JulySwitching Ser	(Ingress & Egress)       with 1280KB SRAM       GPIO         IPv4/IPv6 Filtering (4K flows)       IPv4/IPv6 Filtering (4K flows)       IPv4/IPv6 Filtering (4K flows)       GPIO         Queue Controller       4 Mb Packet Memory       4 Mb Packet Memory       QSPI         8-Level QoS per port       4 Mb Packet Memory       JTAG         JTAG       PILL       PILL         Layer 3 Static Routing       SW1/SPI       SM1/SPI         SW2.IAS & IEVENTE         SW2.IAS & IEVENTE

#### **Block Diagram**

## **Key Features**

Features	Benefits
Processor	Integrated dual core Arm R52 CPU operating in lockstep
Security	<ul> <li>802.1AE MACsec</li> <li>Embedded hardware security module (eHSM)</li> <li>Secure boot and encrypted boot support</li> </ul>
Switch port interfaces	<ul> <li>2x 1000BASE-T1/100BASE-T1 PHYs</li> <li>2x RGMII/MII/RMII</li> <li>4x multi-speed SerDes (2.5G/1Gbps)</li> <li>8x multi-speed SerDes (10G/5G/2.5G/1Gbps)</li> <li>1x PCIe Gen 3 x2 supporting single root I/O virtualization (SR-IOV)</li> </ul>
I/O interfaces	<ul> <li>Configurable GPIO</li> <li>JTAG interface for debugging</li> <li>SMI/SPI interface for configuration</li> <li>QSPI with configurable frequencies (19.2MHz-83.3MHz)</li> </ul>
Time Sensitive Networking (TSN) support	<ul> <li>802.1AS-2020</li> <li>802.1Qat / Qav / Qbu / Qbv / Qci / Qcr</li> <li>802.1CB</li> </ul>
Automotive qualified	<ul> <li>AEC Q-100</li> <li>Automotive Grade 2 (-40°C to +105°C)</li> </ul>
Package characteristics	• 17mm x 17mm, 360 pin TFBGA, 0.8mm pitch

## **Target Applications**

- Central gateway
- Zonal control module
- In-vehicle infotainment
- Advanced driver assistance systems (ADAS)
- Body domain controller



To deliver the data infrastructure technology that connects the world, we're building solutions on the most powerful foundation: our partnerships with our customers. Trusted by the world's leading technology companies for 25 years, we move, store, process and secure the world's data with semiconductor solutions designed for our customers' current needs and future ambitions. Through a process of deep collaboration and transparency, we're ultimately changing the way tomorrow's enterprise, cloud, automotive, and carrier architectures transform—for the better.

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