88SM9705

SATA 6.0 Gbps: 1-to-5 Port Multiplier

Preliminary Specifications

Doc No. MV-S109142-00 Rev. A

June 12, 2015

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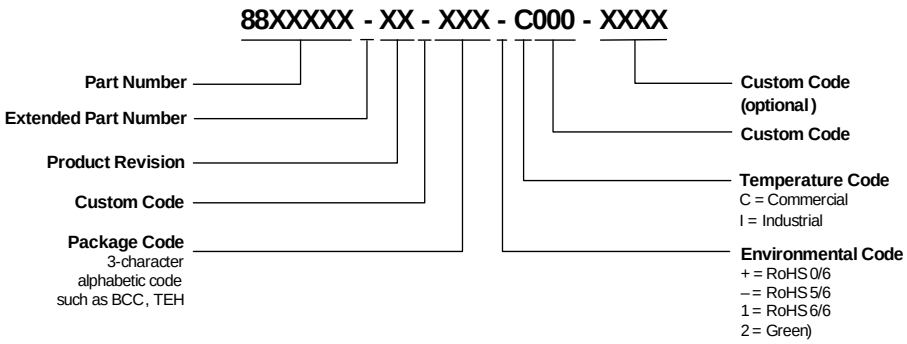
ORDERING INFORMATION

Ordering Part Numbers and Package Markings

The following figure shows the ordering part numbering scheme for the 88SM9705 part. For complete ordering information, contact your Marvell FAE or sales representative.

Figure 0-1 Sample Ordering Part Number



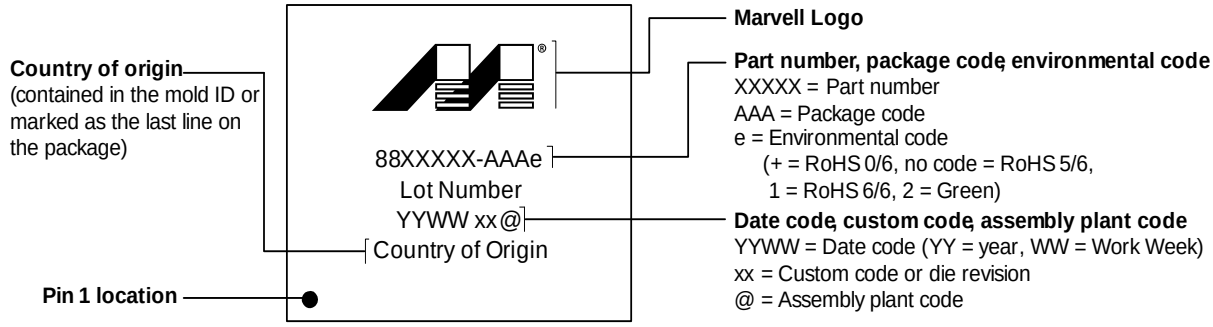
The standard ordering part numbers for the respective solutions are indicated in the following table.

Ordering Part Numbers

Part Number	Description
88SM9705A0-NNR2C000	84-Pin 10 x 10 QFN Package, SATA 6.0 Gbps, One-to-Five Port Multiplier
88SM9705A0-NNR2I000	84-Pin 10 x 10 Industrial Grade QFN Package, SATA 6.0 Gbps, One-to-Five Port Multiplier
88SM9705A0-NNR2A000	84-Pin 10 x 10 Automotive Grade QFN Package, SATA 6.0 Gbps, One-to-Five Port Multiplier

The next figure shows a typical Marvell package marking.

Figure 0-2 88SM9705 Package Marking and Pin 1 Location



Note: The above drawing is not drawn to scale. The location of markings is approximate. Add-on marks are not represented. Flip chips vary widely in their markings and flip chip examples are not shown here. For flip chips, the markings may be omitted per customer requirement.

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CHANGE HISTORY

The following table identifies the document change history for Rev. A.

Document Changes *

Location	Type	Description	Date
Page -iii	Update	Added automotive grade part number 88SM9705A0-NNR2A000 to the Ordering Part Numbers table.	May 6, 2015
Global	Update	Updated section 4.1, Board Schematic Example as follows: • Replaced schematic diagrams with updated versions.	April 7, 2015
Global	Update	Added an introduction sentence to all tables in the document.	September 26, 2013
Global	Update	Added GPIO registers.	October 21, 2014
Page 2-2	Update	Removed the following bullet item in section 2.1, General: “Full scan for high-production test coverage and PHY self-test.”	October 21, 2014
Page 2-3	Update	Added the following bullet item for 2.2, Functional: “Supports SATA Port Multiplier Rev. 1.2.”	February 28,2013
Page 9-5	Update	Added section 9.5, Thermal Data.	September 14 2014
Page 8-13	Parameter	Corrected the default value of PORT_NUM (R002h [3:0]) from 5h to Vh.	February 26, 2013
Page 8-42	Update	Updated description for GPIO[19]_SRC_SEL (R3E4h [9:5]).	March 27, 2015
Page 8-42	Update	Updated description for GPIO[18]_OUTPUT_SRC_SEL (R3E4h [4:0]).	March 27, 2015

* The type of change is categorized as: Parameter, Revision, or Update. A Parameter change is a change to a spec value, a Revision change is one that originates from the chip Revision Notice, and an Update change includes all other document updates.

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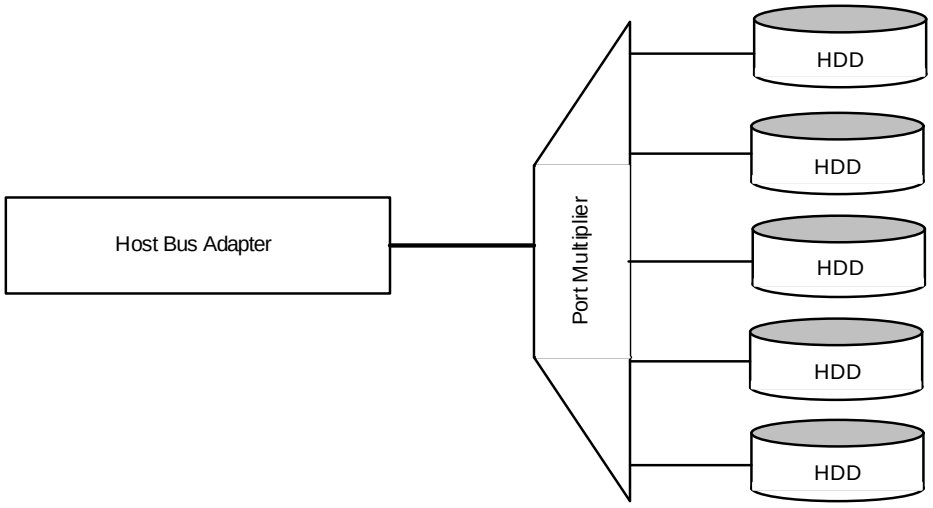
CONTENTS

1 OVERVIEW

The 88SM9705 is a SATA port multiplier that allows an active host connection to communicate with up to five device ports and one SEMB port. The 88SM9705 is used to consolidate the capacity of storage devices by allowing a single host SATA port to be connected to more than one SATA 6 gbps device.

Figure 1-1 illustrates a typical port multiplier configuration.

Figure 1-1 Overview (Five Port)



The 88SM9705 port multiplier employs Marvell SATA 6 Gbps Physical Layer (PHY) technology and recognizes the SATA-defined OOB sequence and speed-negotiation sequence on all of its SATA ports.

The 88SM9705 has programmable amplitude and pre-emphasis settings for a range of drive capabilities to support various backplane and cabling environments.The arbiter receives all the requests from the host port, the device ports, and the control port if these ports must transmit a FIS to the host port. The control port has the highest arbitration priority. The priority of the other ports is determined by a fair priority algorithm.

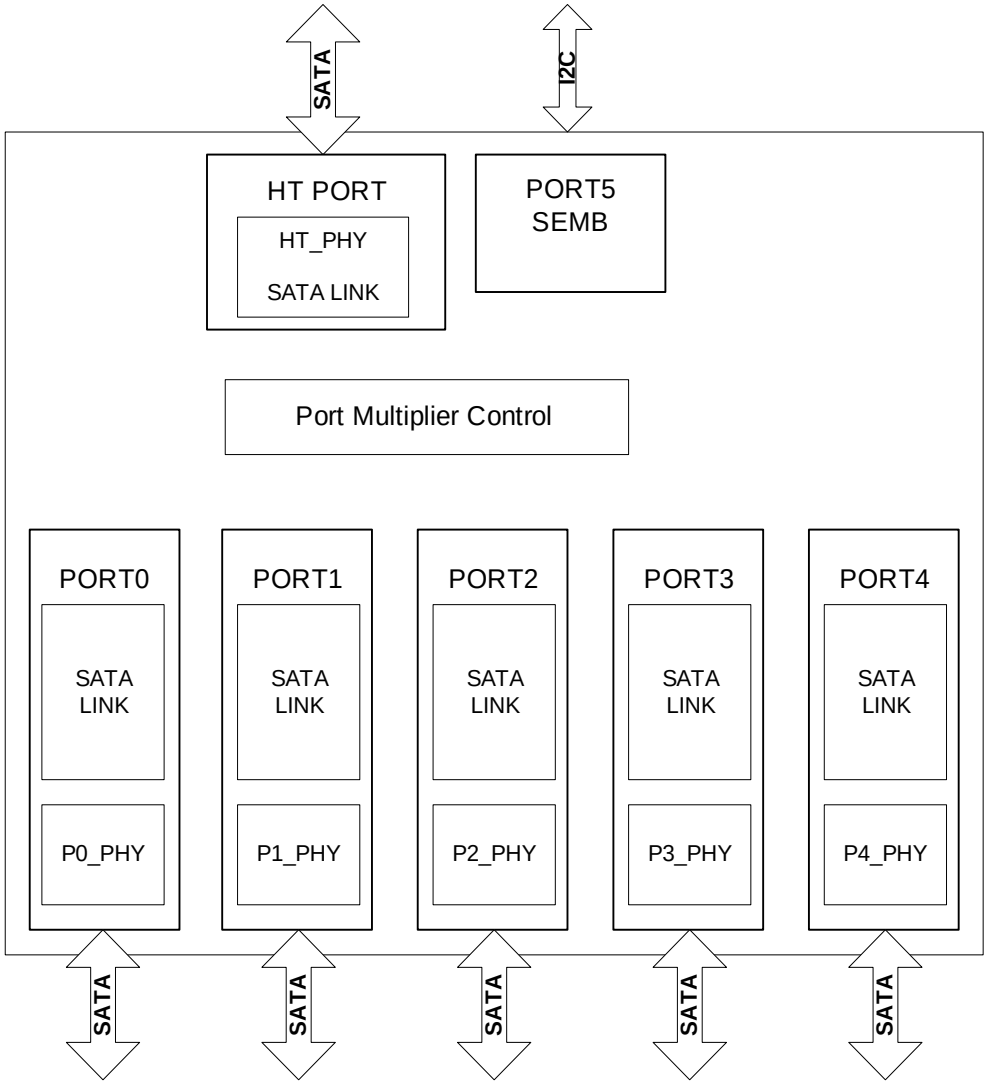
All device ports and the host port can be set up through the host port or UART interface to perform SATA self-tests at the same time.

The PHY Test module is specifically used to test the SATA PHY. All the test patterns are referenced from SATA Test Patterns and the High-Speed Serialized Attachment specification. For more information, see *Serial ATA Revision 3.1 Specification*

(*http://www.sata-io.org*).

Figure 1-2 shows the 88SM9705 blocks.

Figure 1-2 88SM9705 Blocks



2 FEATURES

This chapter contains the following sections:

2.1 General

- 55 nm CMOS technology.
- Supports Serial ATA Revision 3.1 Specification, with communication speeds of 1.5 Gbps, 3 Gbps, and 6 Gbps on host and device ports.
- 1.0V, 1.8V, and 3.3V power.
- 84-pin QFN ePad package.
- PHY test mode.
- One host port.
- Five device
- Supports 25 MHz reference clock.

2.2 Functional

- 115200 bps UART access.
- Spread-spectrum clocking transmission.
- SATA BIST over host and device links.
- Asynchronous notification.
- NOP command to select PM port field (Marvell Specific Mode, optional).SPI interface for internal register programming.
- Supports SATA Port Multiplier Rev. 1.2.

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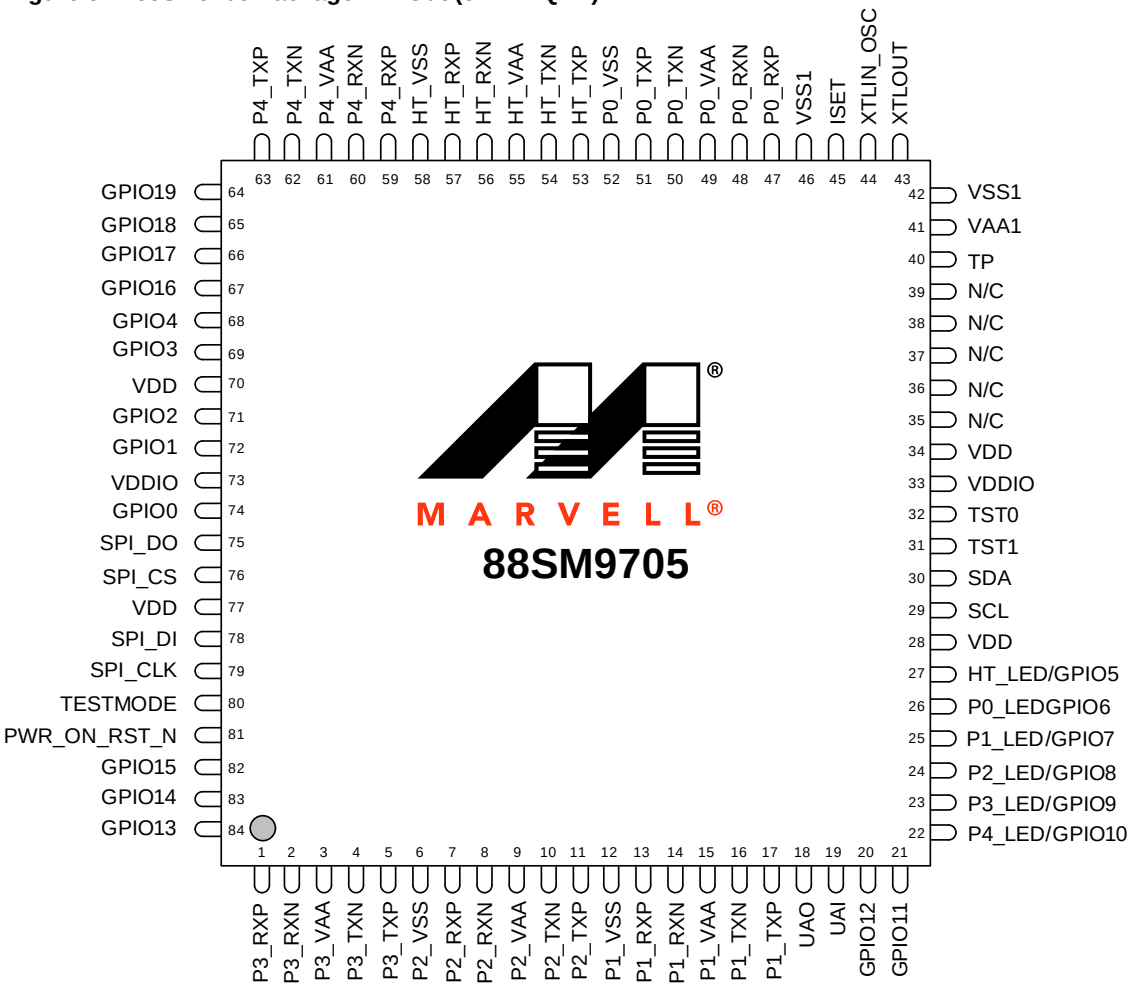
3 PACKAGE

This chapter contains the following sections:

3.1 Package Pin-Out

Figure 3-1 88SM9705 Package Pin-Out (84-Pin QFN)



3.2 Package Dimensions

Figure 3-2 Mechanical Drawings

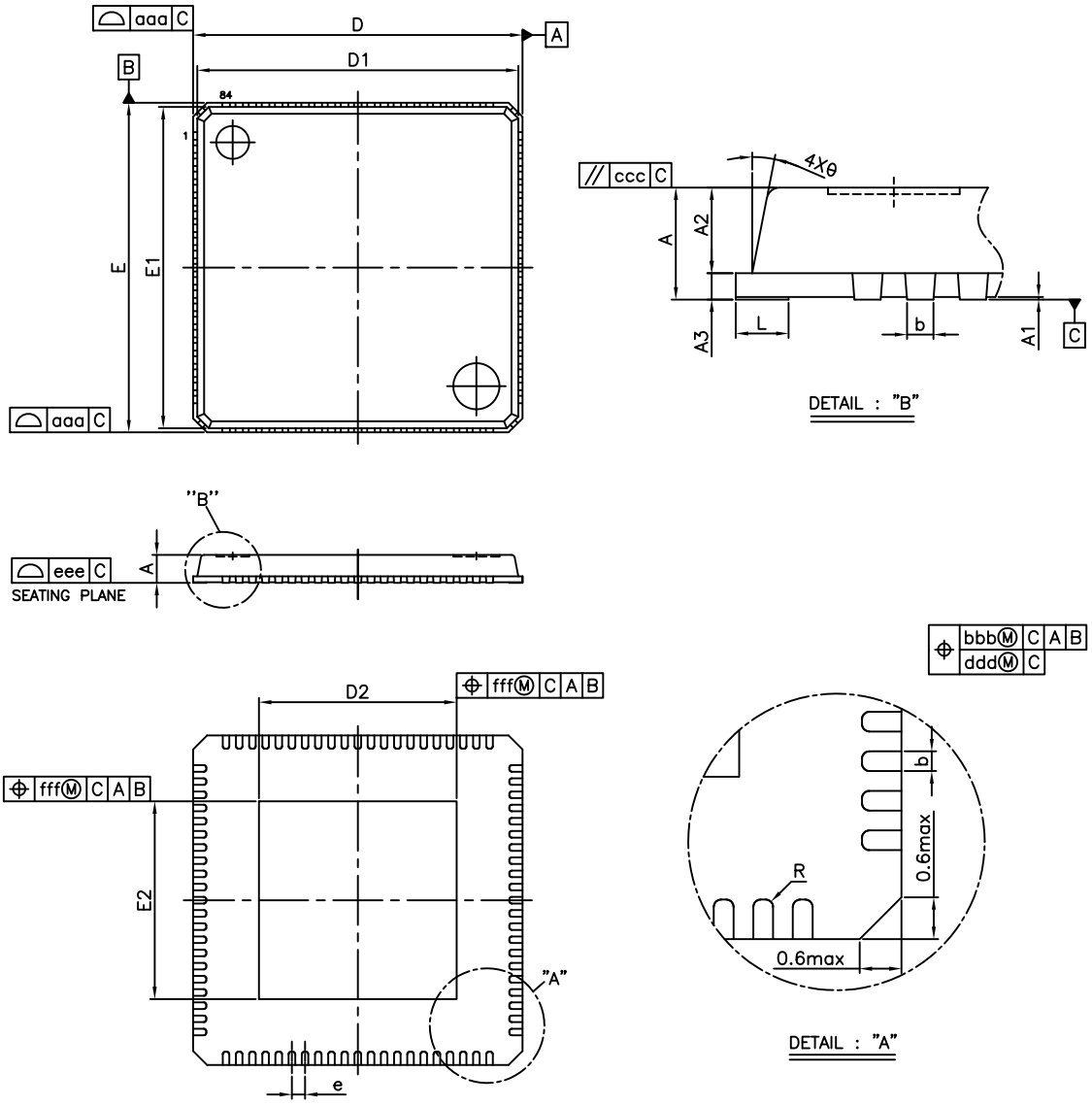


Figure 3-3 Mechanical Dimensions

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	1.00	0.031	0.033	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	0.60	0.65	0.80	0.024	0.026	0.031
A3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	10.00 BSC			0.394 BSC		
D1/E1	9.75 BSC			0.384 BSC		
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
θ	0°	---	14°	0°	---	14°
R	0.075	---	---	0.003	---	---
aaa	---	---	0.15	---	---	0.006
bbb	---	---	0.10	---	---	0.004
ccc	---	---	0.10	---	---	0.004
ddd	---	---	0.05	---	---	0.002
eee	---	---	0.08	---	---	0.003
fff	---	---	0.10	---	---	0.004

	Die Pad Size Options (D2/E2)			Shape Option
	Symbol	Dimension in mm	Dimension in inch	
	D_2	4.60 BSC	.181 BSC	Square
	E_2	4.60 BSC	.181 BSC	

3.3 Pin Descriptions

3.3.1 Pin Type Definitions

This section outlines the 88SM9705 pin descriptions. All signals ending with the letter N indicate an active-low signal. Pin type definitions are shown in the following table.

Table 3-1 Pin Type Definitions

Pin Type	Definition
I/O	Input and output
I	Input only
O	Output only
PD	Internal pull-down resistor (50 kΩ)
PU	Internal pull-up resistor (50 kΩ)
mA	DC sink capability
5	5V tolerance

3.3.2 Pin List

Table 3-2 Serial ATA Interface Signals

Signal Name	Signal Number	Type	Description
P0_TXP	51	O	Serial ATA Transmitter Differential Outputs.
P0_TXN	50	O	
P1_TXP	17	O	
P1_TXN	16	O	
P2_TXP	11	O	
P2_TXN	10	O	
P3_TXP	5	O	
P3_TXN	4	O	
P4_TXP	63	O	
P4_TXN	62	O	
HT_TXP	53	O	
HT_TXN	54	O	

Table 3-2 Serial ATA Interface Signals (continued)

Signal Name	Signal Number	Type	Description
P0_RXN	48	I	Serial ATA Receiver Differential Inputs.
P0_RXP	47	I	
P1_RXN	14	I	
P1_RXP	13	I	
P2_RXN	8	I	
P2_RXP	7	I	
P3_RXN	2	I	
P3_RXP	1	I	
P4_RXN	60	I	
P4_RXP	59	I	
HT_RXN	56	I	
HT_RXP	57	I	

Table 3-3 Chip Power-On Reset Signal

Signal Name	Signal Number	Type	Description
PWR_ON_RST_N	81	I	Chip Power on Reset. Active Low.

Table 3-4 UART Two-Wire Serial Interface

Signal Name	Signal Number	Type	Description
UAO	18	O	UART Data Output.
UAI	19	I	UART Data Input.
SCL	29	I/O	Serial Clock
SDA	30	I/O	Serial Data.

Table 3-5 Configuration and Test Pins

Signal Name	Signal Number	Type	Description
GPIO19	64	I/O	General Purpose I/O 19.
GPIO18	65	I/O	General Purpose I/O 18.
GPIO17	66	I/O	General Purpose I/O 17.
GPIO16	67	I/O	General Purpose I/O 16.

Table 3-5 Configuration and Test Pins (continued)

Signal Name	Signal Number	Type	Description
GPIO15	82	I/O	General Purpose I/O 15.
GPIO14	83	I/O	General Purpose I/O 14.
GPIO13	84	I/O	General Purpose I/O 13.
GPIO12	20	I/O	General Purpose I/O 12.
GPIO11	21	I/O	General Purpose I/O 11.
P4_LED/GPIO10	22	I/O	Device Port 4 Link-up and Activity LED or General Purpose I/O 10.
P3_LED/GPIO9	23	I/O	Device Port 3 Link-up and Activity LED or General Purpose I/O 9.
P2_LED/GPIO8	24	I/O	Device Port 2 Link-up and Activity LED or General Purpose I/O 8.
P1_LED/GPIO7	25	I/O	Device Port 1 Link-up and Activity LED or General Purpose I/O 7.
P0_LED/GPIO6	26	I/O	Device Port 0 Link-up and Activity LED or General Purpose I/O 6.
HT_LED/GPIO5	27	I/O	Host Port Link-up and Activity LED or General Purpose I/O 5.
GPIO4	68	I/O	General Purpose I/O 4.
GPIO3	69	I/O	General Purpose I/O 3
GPIO2	71	I/O	General Purpose I/O 2.
GPIO1	72	I/O	General Purpose I/O 1.
GPIO0	74	I/O	General Purpose I/O 0.
TST0	32	I	Test Pin.
TST1	31	I	Test Pin.

Table 3-6 Reference Signals

Signal Name	Signal Number	Type	Description
ISET	45	I	Reference Current for Crystal Oscillator and PLL. This pin must be connected to an external 6.04 kΩ 1% resistor to the Ground.
XTLOUT	43	O	Crystal Output.
XTLIN_OSC	44	I	Reference Clock Input. It can be from crystal or oscillator.

Table 3-7 Power Pins

Signal Name	Signal Number	Type	Description
HT_VAA	55	I	1.8V Power Source for Host Port SATA PHY.
P0_VAA	49	I	1.8V Power Source for Device Port 0 SATA PHY.
P1_VAA	15	I	1.8V Power Source for Device Port 1 SATA PHY.
P2_VAA	9	I	1.8V Power Source for Device Port 2 SATA PHY.
P3_VAA	3	I	1.8V Power Source for Device Port 3 SATA PHY.
P4_VAA	61	I	1.8V Power Source for Device Port 4 SATA PHY.
VAA1	41	I	1.8V Power Source for Analog logic.
VSS1	42, 46	I	Ground for Analog Logic.
P0_VSS	52	I	Ground for SATA PHY.
P1_VSS	12	I	Ground for SATA PHY.
P2_VSS	6	I	Ground for SATA PHY.
HT_VSS	58	I	Ground for SATA PHY.
VDDIO	33, 73	I	3.3 V Power Source for Digital IO.
VDD	28, 34, 70, 77	I	1.0 V Power Source for Digital.

Table 3-8 SPI Flash Interface Signals

Signal Name	Signal Number	Type	Description
SPI_DO	75	O	Data Output of SPI Flash Interface.
SPI_CLK	79	O	Clock Output of SPI Flash Interface.
SPI_CS	76	O	Mode Select of SPI Flash Interface.
SPI_DI	78	I	Data Input of SPI Flash Interface.

Table 3-9 Test Mode Interface Signals

Signal Name	Signal Number	Type	Description
TESTMODE	80	I	Chip Test Mode.
TP	40	O	Analog Test Point.

Table 3-10 Pins Not Connected

Signal Name	Signal Number	Type	Description
N/C	35, 36, 37, 38, 39	N/A	Not Connected.

4 LAYOUT GUIDELINES

This chapter describes the system recommendations from the Marvell Semiconductor design and application engineers who work with the 88SM9705. It is written for those who are designing schematics and printed circuit boards for an 88SM9705-based system. Whenever possible, the PCB designer must try to follow the suggestions provided in this chapter.

The information in this chapter is preliminary. Consult with Marvell Semiconductor design and application engineers before starting your PCB design.

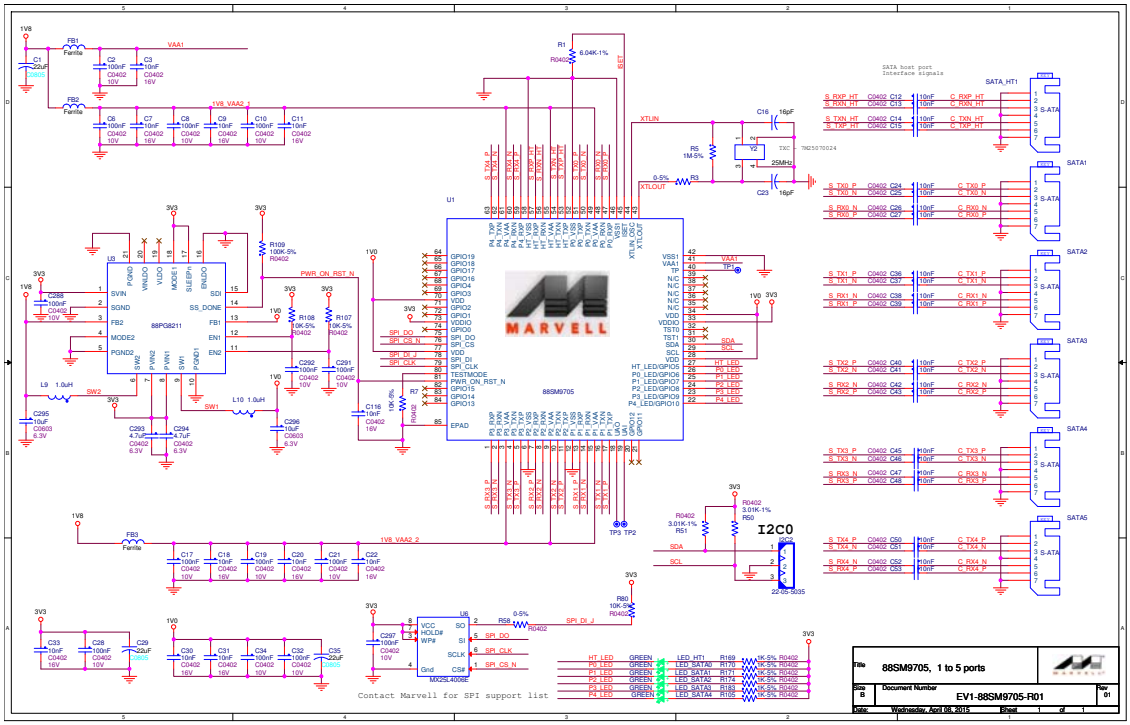
The chapter contains the following sections:

See Chapter 3, Package, for package information.

4.1 Board Schematic Example

The board schematic consists of the major interfaces of the 88SM9705. Figure 4-1 shows an example board schematic.

Figure 4-1 88M9705 Example Board Schematic



Note: This diagram is for reference only. Contact your Marvell field applications engineer for the latest schematics.

4.2 Layer Stack-Up

The recommended minimum requirements are 5-mil traces and 5-mil spacing.The following layer stack up is recommended:

- Layer 1–Topside, Parts, Slow and High Speed Signal Routes, and Power Routes
- Layer 2–Solid Ground Plane
- Layer 3–Power Plane
- Layer 4–Bottom Layer, Slow and High-Speed Signal Routes, and Power Routes

4.2.1 Layer 1–Topside, Parts, Slow and High Speed Signal Routes, and Power Routes

All active parts are to be placed on the topside. Some of the differential pairs for SATA are routed on the top layer, differential 100Ω impedance must be maintained for those high speed signals.

4.2.2 Layer 2–Solid Ground Plane

A solid ground plane must be located directly below the top layer of the PCB. This layer must be a minimum distance below the top layer to reduce the amount of crosstalk and EMI. No cutouts must exist in the ground plane. It is recommended to use 1 ounce copper.

4.2.3 Layer 3–Power Plane

Use solid planes on layer 3 to supply power to the ICs on the PCB. Avoid narrow traces and necks on this plane.

4.2.4 Layer 4–Bottom Layer, Slow and High-Speed Signal Routes, and Power Routes

Some of the differential pairs for SATA are routed on the top layer, differential 100Ω impedance must be maintained for those high speed signals. The high speed signals have the return current on the third layer, which is the power plane. No cut-out must exist under the signal path.

4.3 Power Supply

The 88SM9705 operates using the following power supplies:

- VDD Power (1.0V)
- Analog Power Supply (1.8V)
- VDDIO Power (3.3V)
- Power-on-Reset Timing Requirement
- Bias Current Resistor (RSET)

4.3.1 VDD Power (1.0V)

All digital power pins (VDD pins) must be connected directly to a VDD plane in the power layer with short and wide traces to minimize digital power-trace inductances.

Use vias close to the VDD pins to connect to this plane and avoid using the traces on the top layer. Marvell recommends placing capacitors around the three sides of the PCB near VDD pins with the following dimensions:

- 1 nF (1 capacitor)
- 0.1 µF (2 capacitors)
- 2.2 µF (1 ceramic capacitor)

The 2.2 µF ceramic decoupling capacitor is needed to filter the lower frequency power-supply noise.

To reduce system noise, the use of high-frequency surface-mount monolithic ceramic bypass capacitors must be placed as close as possible to the channel VDD pins. At least one decoupling capacitor must be placed on each side of the IC package.

Short and wide copper traces must be used to minimize parasitic inductances. Low-value capacitors (1,000–10,000 pF) are preferable over higher values because they are more effective at higher frequencies.

4.3.2 Analog Power Supply (1.8V)

The 1.8V power is for analog design of the chip.

4.3.3 VDDIO Power (3.3V)

The digital power (3.3V) is the power supply for the digital pad.

4.3.4 Power-on-Reset Timing Requirement

The minimum timing requirement for power on reset is 50 µs after all power supplies are stable and before the power-on-reset signal is released.

4.3.5 Bias Current Resistor (RSET)

This resistor must connect a 6.04 KΩ (1%) resistor to the ISET pin and the adjacent top ground plane. It must lie as close as possible to the ISET pin.

4.4 PCB Trace Routing

The stack-up parameters for the reference board are shown in Table 4-1.

Table 4-1 PCB Board Stack-up Parameters

Layer	Layer Description	Copper Weight (oz)	Target Impedance (±10%)
1	Signal	0.5	50
2	GND	1	N/A
3	Power	1	N/A
4	Signal	0.5	50

4.5 Recommended Layout

Solid ground planes are recommended. However, special care must be taken when routing VAA and VSS pins.

The following general tips describe what must be considered when determining your stack-up and board routing. These tips are not meant to substitute for consulting with a signal-integrity expert or doing your own simulations.

Note: Specific numbers or rules-of-thumb are not used here because they might not be applicable in every situation.

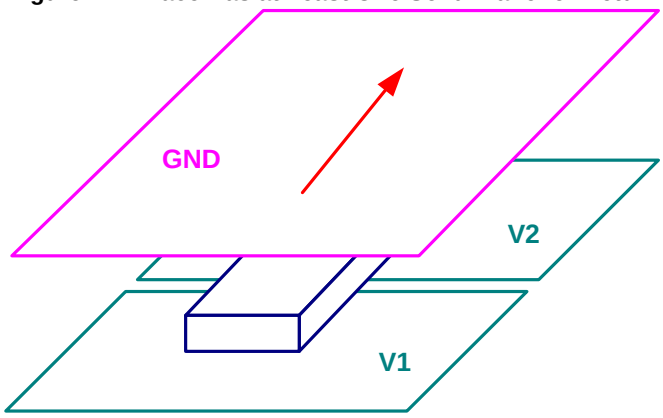
- Do not split ground planes.

  Keep good spacing between possible sensitive analog circuitry on your board and the digital signals to sufficiently isolate noise. A solid ground plane is necessary to provide a good return path for routing layers. Try to provide at least one ground plane adjacent to all routing layers (see Figure 4-2).

- Keep trace layers as close as possible to the adjacent ground or power planes.

  This helps minimize crosstalk and improve noise control on the planes.

Figure 4-2 Trace Has at Least One Solid Plane for Return Path



- When routing adjacent to only a power plane, do not cross splits.

  Route traces only over the power plane that supplies both the driver and the load. Otherwise, provide a decoupling capacitor near the trace at the end that is not supplied by the adjacent power plane.

- Critical signals must avoid running parallel and close to or directly over a gap.

  This would change the impedance of the trace.

- Separate analog powers onto opposing planes.

  This helps minimize the coupling area that an analog plane has with an adjacent digital plane.

- For dual strip-line routing, traces must only cross at 90 degrees.

  Avoid more than two routing layers in a row to minimize tandem crosstalk and to better control impedance.

- Planes must be evenly distributed in order to minimize warping.

- Calculating or modeling impedance must be made prior to routing.

  This helps ensure that a reasonable trace thickness is used and that the desired board thickness is available. Consult with your board fabricator for accurate impedance.

- Allow good separation between fast signals to avoid crosstalk.

  Crosstalk increases as the parallel traces get longer.

- When packages become smaller, route traces over a split power plane

  Smaller packages force vias to become smaller, thereby reducing board thickness and layer counts, which might create the need to route traces over a split power plane. Some alternatives to provide return path for these signals are listed below.

  Caution must be used when applying these techniques. Digital traces must not cross over analog planes, and vice-versa. All of these rules must be followed closely to prevent noise contamination problems that might arise due to routing over the wrong plane.

  By tightly controlling the return path, control noise on the power and ground planes can be controlled.

  - Place a ground layer close enough to the split power plane in order to couple enough to provide buried capacitance, such as SIG-PWR-GND (see Figure 4-3). Return signals that encounter splits in this situation simply jumps to the ground plane, over the split, and back to the other power plane. Buried capacitance provides the benefit of adding low inductance decoupling to your board. Your fabricator may charge for a special license fee and special materials. To determine the amount of capacitance your planes provide, use the following equation:

    $$C = 1.249 \bullet 10^{-13} \bullet E_r \bullet L \bullet W / H$$

    Where E_R is the dielectric coefficient, L • W represents the area of copper, and H is the separation between planes.
  - Provide return-path capacitors that connect to both power planes and jumps the split. Place them close to the traces so that there is one capacitor for every four or five traces. The capacitors would then provide the return path (see Figure 4-4).
  - Allow only static or slow signals on layers where they are adjacent to split planes.

Figure 4-3 shows the ground layer close to the split power plane.

Figure 4-3 Close Power and Ground Planes Provide Coupling for Good Return Path

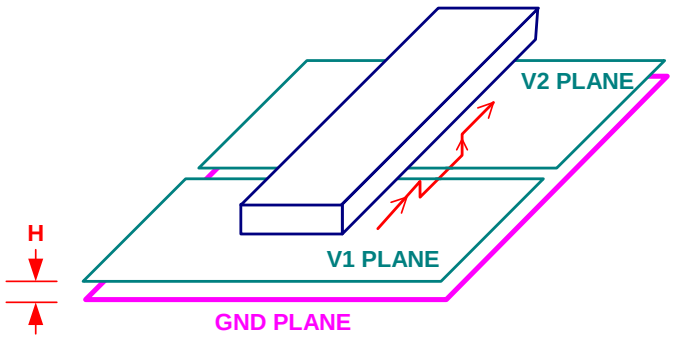
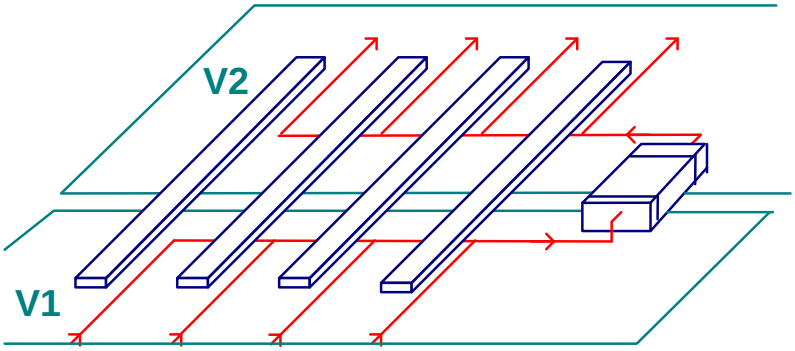


Figure 4-4 shows the thermal ground plane in relation to the return-path capacitor.

Figure 4-4 Suggested Thermal Ground Plane on Opposite Side of Chip



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5 GENERAL PURPOSE I/O PORT INTERFACE

This chapter contains the following sections:

5.1 Overview

The 88SM9705 contains a 20-bit General Purpose Port Input/Output (GPIO) interface. The GPIO interface provides the following features:

- Each of the GPIO pins can be assigned to act as a general purpose input or output pin.
- A dedicated register provides the GPIO input value.
- A dedicated register provides the GPIO output value.
- Each of the GPIO outputs can be programmed for the LED to blink approximately every 100 ms.

5.2 GPIO Normal Mode

Table 5-1 describes the function of the GPIO pins.

Table 5-1 GPIO Pin Default Functions

Pin Name	Default Setting	Default Function	Capable Function	Source	Description
GPIO0	PU	General Purpose I/O	LED blink for RAID	Selectable	Multiple blink frequency
GPIO1	PU	General Purpose I/O	LED blink for RAID	Selectable	Multiple blink frequency
GPIO2	PU	General Purpose I/O	LED blink for RAID	Selectable	Multiple blink frequency
GPIO3	PU	General Purpose I/O	LED blink for RAID	Selectable	Multiple blink frequency
GPIO4	PU	Three-device-port mode: This function is Device 2 port link-up and activity LED Otherwise: General Purpose I/O	0: LED blink for RAID 1: Notification SDB sending pulse output, pulse (1 µs) 2: System alert level output	Selectable	Multiple blink frequency
GPIO5	PU	Host port link-up and activity LED *	LED blink for RAID	Selectable	Multiple blink frequency
GPIO6	PU	Device 0 port link-up and activity LED *	LED blink for RAID	Selectable	Multiple blink frequency
GPIO7	PU	Device 1 port link-up and activity LED *	LED blink for RAID	Selectable	Multiple blink frequency
GPIO8	PU	Device 2 port link-up and activity LED *	LED blink for RAID	Selectable	Multiple blink frequency
GPIO9	PU	Device 3 port link-up and activity LED *	LED blink for RAID	Selectable	Multiple blink frequency
GPIO10	PU		LED blink for RAID	Selectable	Multiple blink frequency
GPIO11	PU	General Purpose I/O	LED blink for RAID	Selectable	Multiple blink frequency
GPIO12	PU	General Purpose I/O	LED blink for RAID	Selectable	Multiple blink frequency
GPIO13	PU	General Purpose I/O	LED blink for RAID	Selectable	Multiple blink frequency
GPIO14	PU	General Purpose I/O	LED blink for RAID	Selectable	Multiple blink frequency
GPIO15	PU	General Purpose I/O	General Purpose I/O	N/A	

Table 5-1 GPIO Pin Default Functions (continued)

Pin Name	Default Setting	Default Function	Capable Function	Source	Description
GPIO16	PU	System alert level output	General Purpose I/O	N/A	Send level when system alert condition is met
GPIO17	PU	General Purpose I/O	General Purpose I/O	N/A	N/A
GPIO18	PU	General Purpose I/O	Power management: POW_OIT	N/A	N/A
GPIO19	PU	General Purpose I/O	Power management: POW_IN	N/A	N/A

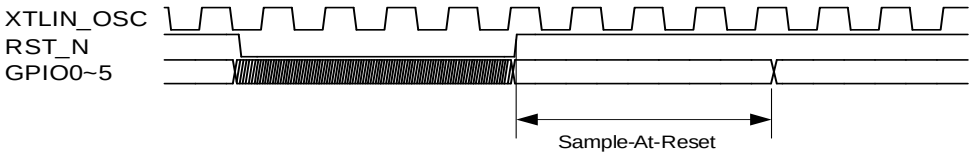
* The link up and activity can be separated and selectable for the blink source.

5.3 GPIO Sample-at-Reset Pins

During chip reset, the method of using the GPIO pins to set the chip operation to the normal functional mode is called sample at reset. This method is activated when the RST_N input rises from low to high and is deactivated four reference cycles later. For example, if the reference cycle is 40 ns, the total time for deactivation is 4 x 40 ns = 160 ns.

Figure 5-1 shows the sample-at-reset timing.

Figure 5-1 Sample-at-Reset Timing



During sample at reset, the signal levels of the GPIO pins must be kept stable so the chip can reliably sample the values. After the sample at reset is deactivated, the GPIO pins can switch to other functions and the chip stops sampling GPIO pins. The sampled values are stored in the internal signals as shown in Table 5-2.

Table 5-2 Sample-at-Reset Signal Descriptions

Pin Name	Function
GPIO0	Legacy Host Enable. **0h:** Legacy Host mode is disabled **1h:** Legacy Host mode is enabled
GPIO1	SEMB Disable. **0h:** SEMB is enabled **1h:** SEMB is disabled.
GPIO2	12C Speed-Up Disable. **0h:** I2C speed-up enabled. **1h:** I2C speed-up disabled.
GPIO3	PHY SSC Disable. **0h:** SATA host and device port SSC enabled. **1h:** SATA PHY SSC disabled
GPIO4	PLL SSC Disable. **0h:** System PLL SSC enabled. **1h:** System PLL SSC disabled.
GPIO5	PM Lock Disable. **0h:** PM Lock enabled. **1h:** PM Lock disabled
GPIO6	NOP Select Disable. **0h:** NOP command selection enabled **1h:** NOP command selection disabled

Table 5-2 Sample-at-Reset Signal Descriptions (continued)

Pin Name	Function
GPIO7	All Ports Disable. **0h:** All ports enabled **1h:** All ports disabled
GPIO8	8K FIFO Disable. **0h:** Device port 8K FIFO enabled **1h:** Device port 8K FIFO disabled

6 UART INTERFACE

This chapter contains the following sections:

6.1 UART Interface Overview

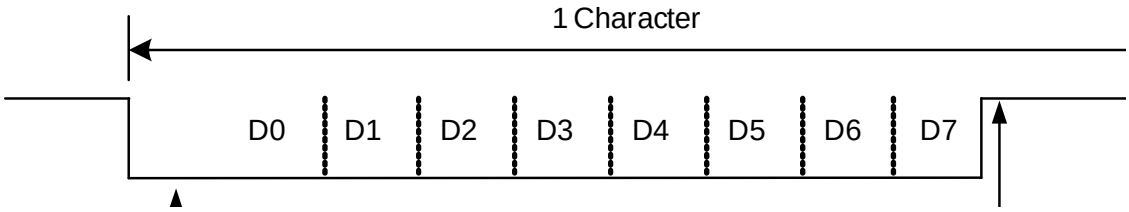
The 88SM9705 has one 115200 bps UART interface.

The UART interface is used to access internal registers, including those for the SATA status and SATA debug registers of each port. The UART interface is not required for normal operation. At the fixed baud rate of 115200 bps, the UART interface block is used mostly for debugging purposes. If the UART pins are not used, then all UAI pins must be left high for normal operation.

6.2 UART Interface Timing

Figure 6-1 illustrates an example of UART signal timing.

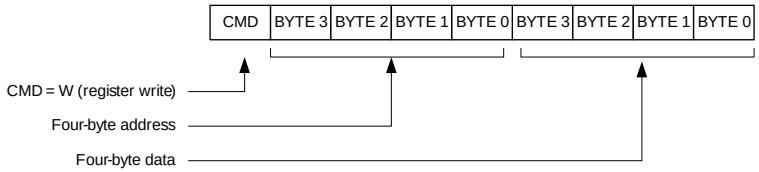
Figure 6-1 UART Signal Timing Example



6.3 Register Access Sequence Through UART

This section describes the register access sequence through the UART. Figure 6.2 shows the write command format.

Figure 6-2 Write Command Format

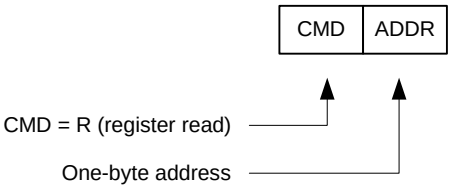


Following are the parameters of the write command format:

- A carriage return (CR) character and a line feed (LF) character are required after a WRITE command for command execution.
- A zero, a carriage return, and a line feed are returned if the command executes correctly.
- A question mark (“?”), a carriage return, and a line feed are returned if an error is encountered.

All alphabetic characters must be in upper case. The backspace character is not recognized. For example: W12AD34DF23 + CR + LF means write the value of AS34DF23h to the location R12h. If the UART returns 0 + CR + LF, then the command executed properly. If the UART returns ? + CR + LF, then the command did not execute properly. Figure 6.3 shows the read command format.

Figure 6-3 Read Command Format



Following are the parameters of the READ command format:

- The carriage return and line feed characters are required after a READ command.
- The register value, carriage return, and line feed characters are returned if the command executes correctly.
- A question mark (“?”), carriage return, and line feed characters are returned if an error is encountered.

All alphabetic characters must be in upper case. The backspace character is not recognized. For example, R12h + CR + LF means read from R12h. If the register value + CR + LF is returned, then the read command executed properly. If ? + CR + LF is returned from the UART, then the command did not execute properly.

6.3.1 UART Read/Write Command Sequences

Each UART sequence includes the parity bit in the last bit. Table 6-1 through Table 6-4, Write Command, Error detail the register Read/Write sequences for Read and Write commands, with and without errors.

Table 6-1 describes the registers read command sequence when no errors are returned.

Table 6-1 Read Command, No Error

Byte	Master	Slave	Value
1	CMD(R)	-	52h
2	ADDR[31:24]	-	ASCII (ADDR[31:28])
3			ASCII (ADDR[27:24])
4	ADDR[23:16]	-	ASCII (ADDR[23:20])
5			ASCII (ADDR[19:16])
6	ADDR[15:8]	-	ASCII (ADDR[15:12])
7			ASCII (ADDR[11:8])
8	ADDR[7:0]	-	ASCII (ADDR[7:4])
9			ASCII (ADDR[3:0])
10	CR	-	0Dh
11	LF	-	0Ah
12	-	DATA[31:24]	ASCII (DATA[31:28])
13			ASCII (DATA[27:24])
14	-	DATA[23:16]	ASCII (DATA[23:20])
15			ASCII (DATA[19:16])
16	-	DATA[15:8]	ASCII (DATA[15:12])
17			ASCII (DATA[11:8])
18	-	DATA[7:0]	ASCII (DATA[7:4])
19			ASCII (DATA[3:0])
20	-	CR	0Dh
21	-	LF	0Ah

Table 6-2 describes the registers read command sequence when errors are returned.

Table 6-2 Read Command, Error

Byte	Master	Slave	Value
1	CMD(R)	-	52h
2	ADDR[31:24]	-	ASCII (ADDR[31:28])
3			ASCII (ADDR[27:24])
4	ADDR[23:16]	-	ASCII (ADDR[23:20])
5			ASCII (ADDR[19:16])
6	ADDR[15:8]	-	ASCII (ADDR[15:12])
7			ASCII (ADDR[11:8])

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Table 6-2 Read Command, Error (continued)

Byte	Master	Slave	Value
8	ADDR[7:0]	-	ASCII (ADDR[7:4])
9			ASCII (ADDR[3:0])
10	CR	-	0Dh
11	LF	-	0Ah
12		?	3Fh
13	-	CR	0Dh
14	-	LF	0Ah

Table 6-3 describes the registers write command sequence when no errors are returned.

Table 6-3 Write Command, No Error

Byte	Master	Slave	Value
1	CMD(W)	-	57h
2	ADDR[31:24]	-	ASCII (ADDR[31:28])
3			ASCII (ADDR[27:24])
4	ADDR[23:16]	-	ASCII (ADDR[23:20])
5			ASCII (ADDR[19:16])
6	ADDR[15:8]	-	ASCII (ADDR[15:12])
7			ASCII (ADDR[11:8])
8	ADDR[7:0]	-	ASCII (ADDR[7:4])
9			ASCII (ADDR[3:0])
10	DATA[31:24]	-	ASCII (DATA[31:28])
11			ASCII (DATA[27:24])
12	DATA[23:16]	-	ASCII (DATA[23:20])
13			ASCII (DATA[19:16])
14	DATA[15:8]	-	ASCII (DATA[15:12])
15			ASCII (DATA[11:8])
16	DATA[7:0]	-	ASCII (DATA[7:4])
17			ASCII (DATA[3:0])
18	CR	-	0Dh
19	LF	-	0Ah
20	-	0	30h
21	-	CR	0Dh
22	-	LF	0Ah

Table 6-4 describes the registers write command sequence when errors are returned.

Table 6-4 Write Command, Error

Byte	Master	Slave	Value
1	CMD(W)	-	57h
2	ADDR[31:24]	-	ASCII (ADDR[31:28])
3			ASCII (ADDR[27:24])
4	ADDR[23:16]	-	ASCII (ADDR[23:20])
5			ASCII (ADDR[19:16])
6	ADDR[15:8]	-	ASCII (ADDR[15:12])
7			ASCII (ADDR[11:8])
8	ADDR[7:0]	-	ASCII (ADDR[7:4])
9			ASCII (ADDR[3:0])
10	DATA3	-	ASCII (BYTE3 [7:4])
11			ASCII (BYTE3[3:0])
12	DATA2	-	ASCII (BYTE2 [7:4])
13			ASCII (BYTE2[3:0])
14	DATA1	-	ASCII (BYTE1 [7:4])
15			ASCII (BYTE1[3:0])
16	DATA0	-	ASCII (BYTE0 [7:4])
17			ASCII (BYTE0[3:0])
18	CR	-	0Dh
19	LF	-	0Ah
20	-	?	3Fh
21	-	CR	0Dh
22	-	LF	0Ah

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7 PORTS

This chapter contains the following sections:

7.1 PM_PORT Field

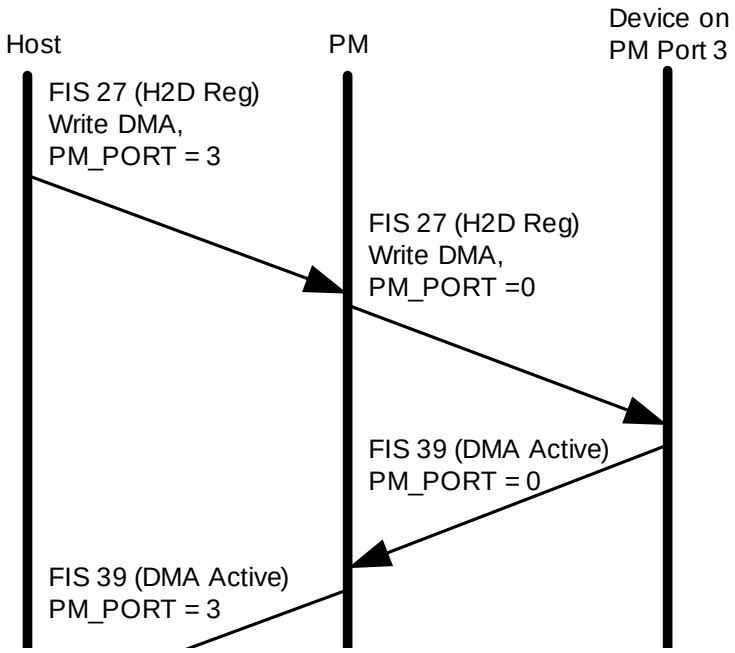
For the 88SM9705 to function, the host must be able to select each SATA device that is connected to the 88SM9705. To accomplish this, the PM_PORT field has been added to all SATA FISes (see Table 7-1). Before the introduction of the port multiplier, these bits had been defined as reserved bits. If the host is port multiplier–enabled, then after the port multiplier's detection and initialization process, the host is able to access each device by changing the value of the PM_PORT field.

Table 7-1 First Dword of All FIS Types

Byte Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Dword 0	(As defined in Serial ATA 3.1 Specification)																				PM_PORT				FIS Type							
Value	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0

Figure 7-1 shows an example of communication between a port multiplier–enabled host and the port multiplier (PM).

Figure 7-1 Traffic Between a Port Multiplier-Aware Host and the Port Multiplier



7.2 Control Ports

Each port multiplier has a control port that provides some device information—such as the connection status (S-Status), SATA Error (S-Error), and the supported port numbers—to the host. The control port also provides the host with some form of control over the devices. For example, the host can tell the port multiplier to disconnect a port or to engage in SATA BIST activity.

To the host, the control port functions exactly the same as a series of registers.

Port multiplier registers are categorized into the following types:

- General Status and Control Registers (GSCR)
- Port Status and Control Registers (PSCR).

Each port multiplier has only one set of GSCR and one set of PSCR for each port.

For more information on the GSCR and PSCR registers, see Chapter 8, Registers.

The host can access the port multiplier's control port as port Fh by using the READ BUFFER (E4h) and WRITE BUFFER (E8h) ATA commands. See section 8.1.1, Register Access from Host and UART for more detail on how these ATA commands can be used with the port multiplier.

7.3 Cascading

The port multiplier should not be cascaded. Do not connect a port multiplier to another port multiplier.

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8 REGISTERS

This chapter contains the following sections:

8.1 Register Summary

This section contains the following subsections:

8.1.1 Register Access from Host and UART

Registers can be accessed from either the host (SATA) or the UART.

8.1.1.1 Accessing from the Host

All registers are accessed from the host (SATA) with an address that uses a combination of the port number and an offset, as described in Table 8-1

Table 8-1 Access Registers from Host (SATA)

Port Number	Address Range	Register Description
F	00h–7Fh	General Purpose Status and Control
F	80h–FFh	Vendor Specific
F	100h–1FFh	Host Port PHY Event
F	200h–2FFh	Host Port
F	300h–3FFh	GPIO
0	00h–FFh	Device 0 Port
0	100h–1FFh	Device 0 Port PHY Event
1	00h–FFh	Device 1 Port
1	100h–1FFh	Device 1 Port PHY Event
2	00h–FFh	Device 2 Port
2	100h–1FFh	Device 2 Port PHY Event
3	00h–FFh	Device 3 Port
3	100h–1FFh	Device 3 Port PHY Event
4	00h–FFh	Device 4 Port
4	100–1FFh	Device 4 Port PHY Event
5	00–FFh	SEMB

Example: Port Multiplier Register Read

To read PM port 2 register 01h, a port multiplier READ command (E4h) is issued to the port multiplier, as shown in Table 8-2:

Table 8-2 PM Read Register

DWORD	[31:24]	[23:16]	[15:8]	[7:0]
DW0	Feature[7:0]	Command	C R R R PM Port	FIS Type
	Reg address[7:0] = 01h	E4h	8 F	27h
DW1	Device	LBA[23:16]	LBA[15:8]	LBA[7:0]
	Port Num = 2	Reserved	Reserved	Reserved
DW2	Feature[15:8]	LBA[47:40]	LBA[39:32]	LBA[31:24]
	Reg address[15:8] = 00h	Reserved	Reserved	Reserved
DW3	Control	ICC	Count[15:8]	Count[7:0]
	Reserved	Reserved	Reserved	Reserved
DW4	Auxiliary[31:24]	Auxiliary[23:16]	Auxiliary[15:8]	Auxiliary[7:0]
	Reserved	Reserved	Reserved	Reserved

Note: FIS is the read Port Multiplier command.

Table 8-3 indicates that the port multiplier returns the read value of the specific register (04050000h).

Table 8-3 PM Read Register Return

DWORD	[31:24]	[23:16]	[15:8]	[7:0]
DW0	Error	Status	R I R R PM Port	FIS Type
	00h	50h	4 F	34h
DW1	Device	LBA[23:16]	LBA[15:8]	LBA[7:0]
	Reserved	Value[31:24] = 04h	Value[23:16] = 05h	Value[15:8] = 00h
DW2	Reserved	LBA[47:40]	LBA[39:32]	LBA[31:24]
	Reserved	Reserved	Reserved	Reserved
DW3	Reserved	Reserved	Count[15:8]	Count[7:0]
	Reserved	Reserved	Reserved	Value[7:0] = 00h
DW4	Reserved	Reserved	Reserved	Reserved
	Reserved	Reserved	Reserved	Reserved

Note: Register D2H FIS from Port Multiplier.

Example: Port Multiplier Register Write

To write to PM port F register 90h with a value of CAFE1F1Fh, a PM WRITE command (E8h) is issued to the PM as shown in Table 8-4.

Table 8-4 PM Write Register

DWORD	[31:24]	[23:16]	[15:8]	[7:0]
DW0	Feature[7:0]	Command	C R R R PM Port	FIS Type
	Reg address[7:0] = 90h	E8h	8 F	27h
DW1	Device	LBA[23:16]	LBA[15:8]	LBA[7:0]
	Port = F	Value[31:24] = CAh	Value[23:16] = FEh	Value[15:8] = 1Fh
DW2	Feature[15:8]	LBA[47:40]	LBA[39:32]	LBA[31:24]
	Reg address[15:8] = 00h	Reserved	Reserved	Reserved
DW3	Control	ICC	Count[15:8]	Count[7:0]
	Reserved	Reserved	Reserved	Value[7:0] = 1Fh
DW4	Auxiliary[31:24]	Auxiliary[23:16]	Auxiliary[15:8]	Auxiliary[7:0]
	Reserved	Reserved	Reserved	Reserved

Note: FIS is the write Port Multiplier command.

8.1.1.2 Accessing from UART

All registers are accessed from UART with a base address of R00020xxxh.

The following items show read and write examples of accessing a General Purpose register with offset 58h:

- Read—R00020058h
- Write—W00020058A5A5A5A5 (write A5A5A5A5 to register 58h).

Table 8-5 shows the address offset ranges and descriptions for register access from UART.

Table 8-5 Register Access from UART

Offset Range	Register Description
R000h–R07Fh	General Status and Control
R080h–R0FFh	Vendor-Specific
R1A0h–R1FFh	GPIO
R200h–R2FFh	Host Port
R300h–R3FFh	Host Port PHY Event
R400h–R4FFh	Device 0 Port
R500h–R5FFh	Device 0 Port PHY Event
R600h–R6FFh	Device 1 Port
R700h–R7FFh	Device 1 Port PHY Event

Table 8-5 Register Access from UART (continued)

Offset Range	Register Description
R800h–R8FFh	Device 2 Port
R900h–R9FFh	Device 2 Port PHY Event
RA00h–RAFFh	Device 3 Port
RB00h–RBFFh	Device 3 Port PHY Event
RC00h–RCFFh	Device 4 Port
RD00h–RDFFh	Device 4 Port PHY Event
RE00h–REFFh	SEMB

8.1.2 General Status and Control Registers

Table 8-6 General Purpose Status and Control Register Summary

Register	Default Value	Register Description	Location
R000h	VVVV1B4Bh	Product Identifier	Page 8-12
R001h	0000A00Eh	Revision Information	Page 8-12
R002h	0000000Vh	Port Information	Page 8-13
R020h	00000000h	Error Information	Page 8-13
R021h	0400FFFFh	Error Information Bit Enable	Page 8-13
R022h	00000000h	PHY Event Counter Control	Page 8-14
R040h	0000001Fh	Port Multiplier Revision 1 X Features Support	Page 8-15
R060h	00000001h	Port Multiplier 1 X Feature Enable	Page 8-15

8.1.3 Vendor-Specific Port Multiplier Control Registers

Table 8-7 Vendor-Specific PM Control Register Summary

Register	Default Value	Register Description	Location
R080h	00000000h	PM Control	Page 8-17
R081h	00000000h	Probe Control	Page 8-18
R082h	00000000h	Probe Signal	Page 8-18
R083h	0000003Eh	PM Lock Control	Page 8-19
R084h	00000000h	PM Lock Status	Page 8-19
R086h	00002C2Bh	SEMB I2C Control	Page 8-20
R087h	00900000h	SEMB Time-out Value	Page 8-20
R089h	00000000h	PLL Control 1	Page 8-21
R08Ah	8000003Fh	PLL Control 2	Page 8-21
R091h	F81E003Ah	FIFO Size Control	Page 8-22
R092h	00000666h	Memory Control	Page 8-23
R093h	00888888h	SATA Port PHY Control	Page 8-23
R0A0h	00000000h	Side Bank Address Register	Page 8-24
R0A1h	00000000h	Side Bank Data Register	Page 8-24

8.1.4 Host Port PHY Event Counter Registers

Table 8-8 Host Port PHY Event Counter Register Summary

Register	Default Value	Register Description	Location
R100h	00000000h	Host Port PHY Event Counter 1	Page 8-25

8.1.5 General Purpose Input/Output (GPIO) Registers

Table 8-9 GPIO Register Summary

Register	Default Value	Register Description	Location
R3A0h	00000000h	GPIO Data Out	Page 8-25
R3A4h	000107C0h	GPIO Data Out Enable	Page 8-25
R3A8h	00000000h	GPIO Blink Enable	Page 8-26
R3ACh	00000000h	GPIO Data In Polarity	Page 8-26
R3B0h	00000000h	GPIO Data In	Page 8-26
R3C4h	2AF624C3h	GPIO [6] through GPIO [11] Port Source Select	Page 8-27
R3C8h	047868C0h	Power-Control Logic Time-Out Control Register	Page 8-32
R3D8h	255AD6B5h	GPIO [0] through GPIO [5] Port Source Select	Page 8-33
R3E0h	2A2AD6B5h	GPIO[12] through GPIO[17] Port Source Select	Page 8-39
R3E4h	000002B5h	GPIO[18] through GPIO[19] Port Source Select	Page 8-42
R3E8h	00000041h	Blink Rate Counter Register for SATA4 and Overall Link	Page 8-42
R3ECh	01041041h	Blink Rate Counter Register for SATA0/1/2/3/H	Page 8-43
R3F0h	01041041h	Blink Rate Counter Register for GPIO_OUT[4] through GPIO_OUT[0]	Page 8-44
R3F4h	01041041h	Blink Rate Counter Register for GPIO_OUT[9] through GPIO_OUT[5]	Page 8-45
R3F8h	01041041h	Blink Rate Counter Register for GPIO_OUT[14] through GPIO_OUT[10]	Page 8-46
R3FCh	01041041h	Blink Rate Counter Register for GPIO_OUT[19] through GPIO_OUT[15]	Page 8-46

8.1.6 SATA PHY and Link Registers

This section includes the following sections:

- Link Registers
- SATA PHY—Low-Power SERDES PHY Registers

8.1.6.1 Link Registers

Table 8-10 Link Register Summary

Register Address	Default Value	Register Description	Location
R00Eh	00002001h	PHY Reserved Input Control	Page 8-47

8.1.6.2 SATA PHY—Low-Power SERDES PHY Registers

Table 8-11 SATA PHY—Low-Power SERDES PHY Register Summary

Register Address	Default Value	Register Description	Location
R8Dh	C958h	Generation 1 Setting 0	Page 8-48
R8Fh	AA62h	Generation 2 Setting 0	Page 8-48
R91h	0BEBh	Generation 3 Setting 0	Page 8-49

8.1.7 Device Port PHY Event Counter Registers

Table 8-12 Device Port PHY Event Counter Register Summary

Register	Default Value	Register Description	Location
R100h	00000000h	Device Port PHY Event Counter 0	Page 8-51
R101h	00000000h	Device Port PHY Event Counter 2	Page 8-51

8.2 Register Map Summary

Table 8-13 General Status and Control Register Map Summary

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R000h	DEV_ID																VENDOR_ID															
R001h	RSVD																PM_REV								RSVD					SPT_PM_12	SPT_PM_S1	SPPRT_PM_10	RSVD
R002h	RSVD																												PORT_NUM			
R020h	RSVD																											P4_SELBIT_PSCR_OR	P3_SELBIT_PSCR_OR	P2_SELBIT_PSCR_OR	P1_SELBIT_PSCR_OR	P0_SELBIT_PSCR_OR
R021h	ERR_INFO_BIT_EN																															
R022h	H_PORTH_GLBL_CNT_RST	RSVD										P4_CNT_RST	P3_CNT_RST	P2_CNT_RST	P1_CNT_RST	P0_CNT_RST	RSVD															PHY_EVENT_CNT_EN
R040h	RSVD																											SPT_PHY_CNT	SPT_NOTIFY	SPT_SSC	SPT_PMREQ	SPT_BIST

Table 8-13 General Status and Control Register Map Summary (continued)

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R060h	RSVD																												NOTIFY_EN	SSC_EN	PMREQP_EN	BIST_EN

Table 8-14 Vendor-Specific Port Multiplier Control Register Map Summary

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R080h	RSVD		SEMB_MEMBIST_TEST_FAIL	SEMB_MEMBIST_TEST_FIN	PORT_4_MEMBIST_TEST_FAIL	PORT_4_MEMBIST_TEST_FIN	PORT_3_MEMBIST_TEST_FAIL	PORT_3_MEMBIST_TEST_FIN	PORT_2_MEMBIST_TEST_FAIL	PORT_2_MEMBIST_TEST_FIN	PORT_1_MEMBIST_TEST_FAIL	PORT_1_MEMBIST_TEST_FIN	PORT_0_MEMBIST_TEST_FAIL	PORT_0_MEMBIST_TEST_FIN	PM_CTL_MEMBIST_TEST_FAIL	PM_CTL_MEMBIST_TEST_FIN	RSVD												NOP_COM_EN	ALL_DEV_EN	HOST_DEV_INV	I2C_SPEED_SEL
R081h	RSVD																				PROBE_MON_SEL				PROBE_MOD_SEL				PROBE_SIG_SEL			
R082h	RSVD																PROBE_SIG															
R083h	LOCK_NOTIFY_EN	RSVD																									SET_DEV_BIT_FIS_REL_LOCK_EN	D2H_FIS_REL_LOCK_EN	SET_DEV_BIT_FIS_LOCK_EN	DMA_SETUP_FIS_LOCK_EN	H2D_FIS_LOCK_EN	PM_LOCK_EN
R084h	RSVD																											PM_LOCK_VALID	PM_LOCK_PORT_ID			
R086h	RSVD			SEMB_INTR	SEMB_WR	SEMB_ADDR			SEMB_RD_WR_DATA								RSVD	SEP_TWOWIRE_SERIAL_ADD							RSVD	SEMB_TWOWIRE_SERIAL_ADD						
R087h	RSVD								SEMB_TO_VAL																							
R089h	RSVD	ANA_GROUP_TESTSEL			ANA_GROUP_GAINX2	ANA_GROUP_BYPASS	ANA_GROUP_BG_SEL		PLL_TEST_MON		PLL_SCC_RESET_EXT	PLL_SCC_FREQ_DIV																	PLL_SSC_GAINX2	PLL_SSC_MODE	PLL_PU_SSC	PLL_SSC_EN
R08Ah	PU_PLL	RSVD	PLL_SSC_RNG														RSVD								RSVD	RSVD	SYSCLK_EN	SATA_DEV_4_CLK_EN	SATA_DEV_3_CLK_EN	SATA_DEV_2_CLK_EN	SATA_DEV_1_CLK_EN	SATA_DEV_0_CLK_EN
R091h	FIFO_SIZE_THRESH_SEL			FIFO_SIZE_THRESH													RSVD								PM_CTL_FIFO_FLOW_CTL_THRSH							
R092h	RSVD																				SEMB_1P_MEM_WTC	SEMB_1P_MEM_RTC			PORT_2P_MEM_WTC	PORT_2P_MEM_RTC			PM_CTL_2P_MEM_WTC	PM_CTL_2P_MEM_RTC		
R093h	RSVD								PORT4_PU	PORT4_SPD_SEL	PORT3_PU	PORT3_SPEED_SEL			PORT2_PU	PORT2_SPEED_SEL					PORT1_PU	PORT1_SPEED_SEL			PORT0_PU	PORT0_SPEED_SEL			HOST_PORT_PU	HOST_PORT_SPEED_SEL		
R0A0h	SPI_MEM_ACCESS	RSVD		UNIT_SEL					MEM_ADD																							
R0A1h	SIDE_BANK_ACCESS																															

Table 8-15 Host Port PHY Event Counter Register Map Summary

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R100h	PHY_EVENT_CNT_1																															

Table 8-17 GPIO Registers

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R3A0h	RSVD												GPIO[19:0]_DATA_OUTPUT																				
R3A4h	OUTPUT_EN_POLARITY	RSVD											GPIO_OUTPUT_EN																				
R3A8h	RSVD												GPIO[19:11]_BLINKING_EN										GPIO[10:5]_BLINKING_DIS					GPIO[4:0]_BLINKING_EN				
R3ACh	RSVD												GPIO_DATA_INPUT_POLARITY_BIT_MAP																				
R3B0h	RSVD												GPIO_INPUT_DATA_BIT_MAP																				
R3C4h	RSVD		GPIO[11]_OUTPUT_SRC_SEL						GPIO[10]_OUTPUT_SRC_SEL				GPIO[9]_OUTPUT_SRC_SEL						GPIO[8]_OUTPUT_SRC_SEL					GPIO[7]_OUTPUT_SRC_SEL					GPIO[6]_OUTPUT_SRC_SEL				
R3C8h	RSVD				TIMEOUT_CNTR_VAL																											
R3D8h	RSVD		GPIO[5]_OUTPUT_SRC_SEL						GPIO[4]_OUTPUT_SRC_SEL				GPIO[3]_OUTPUT_SRC_SEL						GPIO[2]_OUTPUT_SRC_SEL					GPIO[1]_OUTPUT_SRC_SEL					GPIO[0]_OUTPUT_SRC_SEL				
R3E0h	RSVD		GPIO[17]_DATA_OUT						GPIO16_OUTPUT_SRC_SEL				GPIO[15]_DATA_OUT						GPIO[14]_OUTPUT_SRC_SEL					GPIO[13]_OUTPUT_SRC_SEL					GPIO[12]_OUTPUT_SRC_SEL				
R3E4h	RSVD																						GPIO[19]_SRC_SEL					GPIO[18]_OUTPUT_SRC_SEL				
R3E8h	RSVD																				CNTR_VAL_BLINK_RATE_SATA4							CNTR_VAL_BLINK_RATE				
R3ECh	RSVD		SATAH_CNTR_VAL_BLINK_RATE						SATA3_CNTR_VAL_BLINK_RATE				SATA2_CNTR_VAL_BLINK_RATE								SATA1_CNTR_VAL_BLINK_RATE							SATA0_CNTR_VAL_BLINK_RATE				
R3F0h	RSVD		GPIO[4]_CNTR_VAL_BLINK_RATE						GPIO[3]_CNTR_VAL_BLINK_RATE				GPIO[2]_CNTR_VAL_BLINK_RATE								GPIO[1]_CNTR_VAL_BLINK_RATE							GPIO[0]_CNTR_VAL_BLINK_RATE				
R3F4h	RSVD		GPIO[9]_CNTR_VAL_BLINK_RATE						GPIO[8]_CNTR_VAL_BLINK_RATE				GPIO[7]_CNTR_VAL_BLINK_RATE								GPIO[6]_CNTR_VAL_BLINK_RATE							GPIO[5]_CNTR_VAL_BLINK_RATE				
R3F8h	RSVD		GPIO[14]_CNTR_VAL_BLINK_RATE						GPIO[13]_CNTR_VAL_BLINK_RATE				GPIO[12]_CNTR_VAL_BLINK_RATE								GPIO[11]_CNTR_VAL_BLINK_RATE							GPIO[10]_CNTR_VAL_BLINK_RATE				
R3FCh	RSVD		GPIO[19]_CNTR_VAL_BLINK_RATE						GPIO[18]_CNTR_VAL_BLINK_RATE				GPIO[17]_CNTR_VAL_BLINK_RATE								GPIO[16]_CNTR_VAL_BLINK_RATE							GPIO[15]_CNTR_VAL_BLINK_RATE				
R00Eh	RSVD																						SSC_EN	TX_AMP_ADJ	RSVD							
R8Dh																	G1_TX_SLEW_CTRL_EN	G1_TX_SLEW_RATE_SEL		G1_TX_EMPH_EN	G1_TX_EMPH_AMP			RSVD	G1_TX_AMP				RSVD				
R8Fh																	G2_TX_SLEW_CTRL_EN	G2_TX_SLEW_RATE_SEL		G2_TX_EMPH_EN	G2_TX_EMPH_AMP			RSVD	G2_TX_AMP				RSVD				
R91h																	G3_TX_SLEW_CTRL_EN	G3_TX_SLEW_RATE_SEL		G3_TX_EMPH_EN	G3_TX_EMPH_AMP			RSVD	G3_TX_AMP				RSVD				
R100h	DEV_PORT_PHY_EVENT_CNTR_0																															
R101h	DEV_PORT_PHY_EVENT_CNTR_2																															
R3FCh	RSVD		GPIO[19]_CNTR_VAL_BLINK_RATE						GPIO[18]_CNTR_VAL_BLINK_RATE				GPIO[17]_CNTR_VAL_BLINK_RATE								GPIO[16]_CNTR_VAL_BLINK_RATE							GPIO[15]_CNTR_VAL_BLINK_RATE				

Table 8-18 Link Register Map Summary

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R00Eh	RSVD																						SSC_EN	TX_AMP_ADJ	RSVD							

Table 8-19 SATA PHY—Low-Power SERDES PHY Register Map Summary

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R8Dh																	G1_TX_SLEW_CTRL_EN	G1_TX_SLEW_RATE_SEL			G1_TX_EMPH_EN	G1_TX_EMPH_AMP				RSVD	G1_TX_AMP					RSVD
R8Fh																	G2_TX_SLEW_CTRL_EN	G2_TX_SLEW_RATE_SEL			G2_TX_EMPH_EN	G2_TX_EMPH_AMP				RSVD	G2_TX_AMP					RSVD
R91h																	G3_TX_SLEW_CTRL_EN	G3_TX_SLEW_RATE_SEL			G3_TX_EMPH_EN	G3_TX_EMPH_AMP				RSVD	G3_TX_AMP					RSVD

Table 8-20 Device Port PHY Event Counter Register Map Summary

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R100h	DEV_PORT_PHY_EVENT_CNTR_0																															
R101h	DEV_PORT_PHY_EVENT_CNTR_2																															

8.3 Register Description

This section contains the following subsections:

- General Status and Control Registers
- Vendor-Specific Port Multiplier Control Registers
- Host Port PHY Event Counter Registers
- SATA PHY and Link Registers
- Device Port PHY Event Counter Registers

8.3.1 General Status and Control Registers

R000h (VVVV1B4Bh) • Product Identifier

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	DEV_ID																VENDOR_ID															
Default Value	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	0	0	0	1	1	0	1	1	0	1	0	0	1	0	1	1

Bits	Field Name	Read/ Write	Default Value	Description
31:16	DEV_ID	R	VVVVh	Product Identifier. **9705h:** 1-to-5 Port Multiplier
15:0	VENDOR_ID	R	1B4Bh	Vendor Identifier.

R001h (0000A00Eh) • Revision Information

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD																PM_REV								RSVD				SPT_PM_12	SPT_PM_S1	SPPRT_PM_10	RSVD
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	1	1	1	0

Bits	Field Name	Read/ Write	Default Value	Description
31:16	RSVD	R	0000h	Reserved. Do not change the default value.
15:8	PM_REV	R	A0h	Port Multiplier Revision.
7:4	RSVD	R	0h	Reserved.
3	SPT_PM_12	R	1h	Support for Port Multiplier Specification 1.2.
2	SPT_PM_S1	R	1h	Support for Port Multiplier Specification 1.1.
1	SPPRT_PM_10	R	1h	Support for Port Multiplier Specification 1.0.
0	RSVD	R	0h	Reserved. Do not change the default value.

R002h (0000000Vh) • Port Information

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD																												PORT_NUM			
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	V	V	V	V

Bits	Field Name	Read/ Write	Default Value	Description
31:4	RSVD	R	0000000h	Reserved.
3:0	PORT_NUM	R	Vh	Number of Exposed Device Fan Out Ports. The default value is 6h if SEMB enabled and 5h if not enabled.

R020h (00000000h) • Error Information

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD																											P4_SEL_BIT_PSCR_OR	P3_SEL_BIT_PSCR_OR	P2_SEL_BIT_PSCR_OR	P1_SEL_BIT_PSCR_OR	P0_SEL_BIT_PSCR_OR
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field Name	Read/ Write	Default Value	Description
31:5	RSVD	R	0000000h	Reserved.
4	P4_SEL_BIT_PSCR_OR	R	0h	OR of Selectable Bits in Port 4 PSCR[1] (SError).
3	P3_SEL_BIT_PSCR_OR	R	0h	OR of Selectable Bits in Port 3 PSCR[1] (SError).
2	P2_SEL_BIT_PSCR_OR	R	0h	OR of Selectable Bits in Port 2 PSCR[1] (SError).
1	P1_SEL_BIT_PSCR_OR	R	0h	OR of Selectable Bits in Port 1 PSCR[1] (SError).
0	P0_SEL_BIT_PSCR_OR	R	0h	OR of Selectable Bits in Port 0 PSCR[1] (SError).

R021h (0400FFFFh) • Error Information Bit Enable

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	ERR_INFO_BIT_EN																															
Default Value	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Field Name	Read/ Write	Default Value	Description
31:0	ERR_INFO_BIT_EN	R/W	0400FFFFh	Error Information Bit Enable. When this bit is enabled use Error Information (R020h).

R022h (00000000h) • PHY Event Counter Control

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	H_PORTH_GLBL_CNT_RST	RSVD										P4_CNT_RST	P3_CNT_RST	P2_CNT_RST	P1_CNT_RST	P0_CNT_RST	RSVD																PHY_EVENT_CNT_EN
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field Name	Read/ Write	Default Value	Description
31	H_PORTH_GLBL_CNT_RST	R/W	0h	Host Port Global Counter Reset. **0h:** No action is taken **1h:** Immediately resets all PHY event counters associated with the device port. After the reset is complete, this bit is cleared to 0h.
30:21	RSVD	R	000h	Reserved.
20	P4_CNT_RST	R/W	0h	Port 4 Global Counter Reset. **0h:** No action is taken. **1h:** Immediately resets all PHY event counters associated with the device port. After the reset is complete, this bit is cleared to 0h.
19	P3_CNT_RST	R/W	0h	Port 3 Global Counter Reset. **0h:** No action is taken. **1h:** Immediately resets all PHY event counters associated with the device port. After the reset is complete, this bit is cleared to 0h.
18	P2_CNT_RST	R/W	0h	Port 2 Global Counter Reset. **0h:** No action is taken. **1h:** Immediately resets all PHY event counters associated with the device port. After the reset is complete, this bit is cleared to 0h.
17	P1_CNT_RST	R/W	0h	Port 1 Global Counter Reset. **0h:** No action is taken. **1h:** Immediately resets all PHY event counters associated with the device port. After the reset is complete, this bit is cleared to 0h.
16	P0_CNT_RST	R/W	0h	Port 0 Global Counter Reset. **0h:** No action is taken. **1h:** Immediately resets all PHY event counters associated with the device port. After the reset is complete, this bit is cleared to 0h.
15:1	RSVD	R/W	0000h	Reserved. Do not change the default value.
0	PHY_EVENT_CNT_EN	R/W	0h	PHY Event Counter Enabled. **0h:** All event counters stop counting and retain their current value. **1h:** Enable all PHY event counters.

R040h (0000001Fh) • Port Multiplier Revision 1 X Features Support

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD																											SPT_PHY_CNT	SPT_NOTIFY	SPT_SSC	SPT_PMREQ	SPT_BIST
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1

Bits	Field Name	Read/ Write	Default Value	Description
31:5	RSVD	R	0000000h	Reserved. Do not change the default value.
4	SPT_PHY_CNT	R	1h	Support PHY Event Counter. **0h:** Does not support PHY event counters. **1h:** Supports PHY event counters.
3	SPT_NOTIFY	R	1h	Support Asynchronous Notification. This bit toggles asynchronous set bit device (SDB) notification. **0h:** Does not support SDB notification. **1h:** Supports SDB notification.
2	SPT_SSC	R	1h	Support Dynamic SSC Transmit Enable. This bit toggles support for dynamic spread spectrum clock (SSC) transmission. **0h:** Does not support SSC transmit. **1h:** Supports SSC transmit.
1	SPT_PMREQ	R	1h	Support PMREQp. **0h:** Does not support issuing a PMREQp to the host. **1h:** Supports issuing a PMREQp to the host.
0	SPT_BIST	R	1h	Support BIST. **0h:** Does not support BIST. **1h:** Supports BIST.

R060h (00000001h) • Port Multiplier 1 X Feature Enable

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD																												NOTIFY_EN	SSC_EN	PMREQP_EN	BIST_EN
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Field Name	Read/ Write	Default Value	Description
31:4	RSVD	R	0000000h	Reserved. Do not change the default value.

Bits	Field Name	Read/ Write	Default Value	Description
3	NOTIFY_EN	R/W	0h	Asynchronous Notification Enable. This bit enables asynchronous set bit device (SDB) notification. **0h:** Disable **1h:** Enable
2	SSC_EN	R/W	0h	SSC Enable. This bit enables dynamic SSC transmitting. **0h:** Disable **1h:** Enable
1	PMREQP_EN	R/W	0h	PMREQ Enable. This bit enables the issuing of PMREQp to the host. **0h:** Disable **1h:** Enable
0	BIST_EN	R/W	1h	BIST Support Enable. **0h:** Disable **1h:** Enable

8.3.2 Vendor-Specific Port Multiplier Control Registers

R080h (00000000h) • PM Control

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD		SEMB_MEMBIST_TEST_FAIL	SEMB_MEMBIST_TEST_FIN	PORT_4_MEMBIST_TEST_FAIL	PORT_4_MEMBIST_TEST_FIN	PORT_3_MEMBIST_TEST_FAIL	PORT_3_MEMBIST_TEST_FIN	PORT_2_MEMBIST_TEST_FAIL	PORT_2_MEMBIST_TEST_FIN	PORT_1_MEMBIST_TEST_FAIL	PORT_1_MEMBIST_TEST_FIN	PORT_0_MEMBIST_TEST_FAIL	PORT_0_MEMBIST_TEST_FIN	PM_CTL_MEMBIST_TEST_FAIL	PM_CTL_MEMBIST_TEST_FIN	RSVD												NOP_COM_EN	ALL_DEV_EN	HOST_DEV_INV	I2C_SPEED_SEL
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field Name	Read/ Write	Default Value	Description
31:30	RSVD	R	0h	Reserved.
29	SEMB_MEMBIST_TEST_FAIL	R	0h	SEMB Memory BIST Test Fail.
28	SEMB_MEMBIST_TEST_FIN	R	0h	SEMB Memory BIST Test Finish.
27	PORT_4_MEMBIST_TEST_FAIL	R	0h	Port 4 Memory BIST Test Fail.
26	PORT_4_MEMBIST_TEST_FIN	R	0h	Port 4 Memory BIST Test Finish.
25	PORT_3_MEMBIST_TEST_FAIL	R	0h	Port 3 Memory BIST Test Fail.
24	PORT_3_MEMBIST_TEST_FIN	R	0h	Port 3 Memory BIST Test Finish.
23	PORT_2_MEMBIST_TEST_FAIL	R	0h	Port 2 Memory BIST Test Fail.
22	PORT_2_MEMBIST_TEST_FIN	R	0h	Port 2 Memory BIST Test Finish.
21	PORT_1_MEMBIST_TEST_FAIL	R	0h	Port 1 Memory BIST Test Fail.
20	PORT_1_MEMBIST_TEST_FIN	R	0h	Port 1 Memory BIST Test Finish.
19	PORT_0_MEMBIST_TEST_FAIL	R	0h	Port 0 Memory BIST Test Fail.
18	PORT_0_MEMBIST_TEST_FIN	R	0h	Port 0 Memory BIST Test Finish.
17	PM_CTL_MEMBIST_TEST_FAIL	R	0h	PM CTL Memory BIST Test Fail.
16	PM_CTL_MEMBIST_TEST_FIN	R	0h	PM CTL Memory BIST Test Finish.
15:4	RSVD	R	000h	Reserved.
3	NOP_COM_EN	R	0h	NOP Command Enable.

Bits	Field Name	Read/ Write	Default Value	Description
2	ALL_DEV_EN	R	0h	All Devices Enable.
1	HOST_DEV_INV	R	0h	Host Device Inversion.
0	I2C_SPEED_SEL	R	0h	I2C Speed Select.

R081h (00000000h) • Probe Control

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD																				PROBE_MON_SEL				PROBE_MOD_SEL				PROBE_SIG_SEL			
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field Name	Read/ Write	Default Value	Description
31:12	RSVD	R	00000h	Reserved.
11:8	PROBE_MON_SEL	R/W	0h	Probe Monitor Select.
7:4	PROBE_MOD_SEL	R/W	0h	Probe Module Select.
3:0	PROBE_SIG_SEL	R/W	0h	Probe Signal Select.

R082h (00000000h) • Probe Signal

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD																PROBE_SIG															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field Name	Read/ Write	Default Value	Description
31:16	RSVD	R	0000h	Reserved.
15:0	PROBE_SIG	R	0000h	Probe Signal.

R083h (0000003Eh) • PM Lock Control

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	LOCK_NOTIFY_EN	RSVD																									SET_DEV_BIT_FISREL_LOCK_EN	D2H_FIS_REL_LOCK_EN	SET_DEV_BIT_FIS_LOCK_EN	DMA_SETUP_FISLOCK_EN	H2D_FIS_LOCK_EN	PM_LOCK_EN
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0

Bits	Field Name	Read/ Write	Default Value	Description
31	LOCK_NOTIFY_EN	R/W	0h	Lock Notify Enable. When this bit is set to 0, PM lock enable (PM lock control [0]) is set to 1, and some ports are in a locked state, the control port postpones sending SDB until no port is in the lock state.
30:6	RSVD	R	0000000h	Reserved.
5	SET_DEV_BIT_FISREL_LOCK_EN	R/W	1h	Set Device BIT FIS Release Lock Enable.
4	D2H_FIS_REL_LOCK_EN	R/W	1h	D2H FIS Release Lock Enable.
3	SET_DEV_BIT_FIS_LOCK_EN	R/W	1h	Set Device BIT FIS Lock Enable.
2	DMA_SETUP_FISLOCK_EN	R/W	1h	DMA Setup FIS Lock Enable.
1	H2D_FIS_LOCK_EN	R/W	1h	H2D FIS Lock Enable.
0	PM_LOCK_EN	R/W	0h	PM Lock Enable.

R084h (00000000h) • PM Lock Status

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD																											PM_LOCK_VALID	PM_LOCK_PORT_ID			
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field Name	Read/ Write	Default Value	Description
31:5	RSVD	R	0000000h	Reserved.
4	PM_LOCK_VALID	R	0h	PM Lock Valid. When this bit is set to 1, a port is in a locked state.
3:0	PM_LOCK_PORT_ID	R	0h	PM Lock Port ID.

R086h (00002C2Bh) • SEMB I2C Control

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD			SEMB_INTR	SEMB_WR	SEMB_ADDR			SEMB_RD_WR_DATA								RSVD	SEP_TWOWIRE_SERIAL_ADD							RSVD	SEMB_TWOWIRE_SERIAL_ADD						
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	0	0	1	0	1	0	1	1

Bits	Field Name	Read/ Write	Default Value	Description
31:29	RSVD	R	0h	Reserved.
28	SEMB_INTR	R	0h	SEMB Interrupt. Refer to the Two-Wire Serial IP specification for more detail.
27	SEMB_WR	R/W	0h	SEMB Register Write. SEMB_WR, SEMB_ADDR, and SEMB_RD_WR_DATA signals provide an interface for the software to program the Two-Wire Serial register so that the software can control the interface of Two-Wire Serial. Refer to the Two-Wire Serial IP Specification for more detail.
26:24	SEMB_ADDR	R/W	0h	SEMB Register Address. Refer to the Two-Wire Serial IP Specification for more detail.
23:16	SEMB_RD_WR_DATA	R/W	00h	SEMB Read Write Data. Refer to the Two-Wire Serial IP Specification for more detail.
15	RSVD	R	0h	Reserved.
14:8	SEP_TWOWIRE_SERIAL_ADD	R/W	2Ch	SEP Two-Wire Serial Address.
7	RSVD	R	0h	Reserved.
6:0	SEMB_TWOWIRE_SERIAL_ADD	R/W	2Bh	SEMB Two-Wire Serial Address.

R087h (00900000h) • SEMB Time-out Value

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD								SEMB_TO_VAL																							
Default Value	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field Name	Read/ Write	Default Value	Description
31:24	RSVD	R	00h	Reserved.
23:0	SEMB_TO_VAL	R/W	900000h	SEMB Time-Out Value. SEMB time-out occurs when wait time larger than time-out value times cycle time.

R089h (00000000h) • PLL Control 1

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD	ANA_GROUP_TESTSEL			ANA_GROUP_GAINX2	ANA_GROUP_BYPASS	ANA_GROUP_BG_SEL		PLL_TEST_MON				PLL_SCC_RESET_EXT	PLL_SCC_FREQ_DIV															PLL_SSC_GAINX2	PLL_SSC_MODE	PLL_PU_SSC	PLL_SSC_EN
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field Name	Read/ Write	Default Value	Description
31	RSVD	R/W	0h	Reserved.
30:28	ANA_GROUP_TESTSEL	R/W	0h	Analog Group Test Select.
27	ANA_GROUP_GAINX2	R/W	0h	Analog Group Gain x2.
26	ANA_GROUP_BYPASS	R/W	0h	Analog Group Bypass.
25:24	ANA_GROUP_BG_SEL	R/W	0h	Analog Group BG_SEL.
23:20	PLL_TEST_MON	R/W	0h	PLL Test Monitor.
19	PLL_SCC_RESET_EXT	R/W	0h	PLL SCC Reset Extend.
18:4	PLL_SCC_FREQ_DIV	R/W	0000h	PLL SCC Frequency Divider.
3	PLL_SSC_GAINX2	R/W	0h	PLL SSC Gain x2.
2	PLL_SSC_MODE	R/W	0h	PLL SSC Mode.
1	PLL_PU_SSC	R/W	0h	PLL Power Up SSC.
0	PLL_SSC_EN	R/W	0h	PLL SSC Enable.

R08Ah (8000003Fh) • PLL Control 2

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	PU_PLL	RSVD	PLL_SSC_RNG														RSVD								RSVD	RSVD	SYSCLK_EN	SATA_DEV4_CLK_EN	SATA_DEV3_CLK_EN	SATA_DEV2_CLK_EN	SATA_DEV1_CLK_EN	SATA_DEV0_CLK_EN
Default Value	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Bits	Field Name	Read/ Write	Default Value	Description
31	PU_PLL	R/W	1h	Power-Up PLL (Asynchronous Reset).
30	RSVD	R/W	0h	Reserved.
29:16	PLL_SSC_RNG	R/W	0000h	PLL SSC Range.
15:8	RSVD	R	00h	Reserved.
7	RSVD	R	0h	Reserved.
6	RSVD	R	0h	Reserved.

Bits	Field Name	Read/ Write	Default Value	Description
5	SYSCLK_EN	R/W	1h	System Clock Enable.
4	SATA_DEV_4_CLK_EN	R/W	1h	SATA Device 4 Clock Enable.
3	SATA_DEV_3_CLK_EN	R/W	1h	SATA Device 3 Clock Enable.
2	SATA_DEV_2_CLK_EN	R/W	1h	SATA Device 2 Clock Enable.
1	SATA_DEV_1_CLK_EN	R/W	1h	SATA Device 1 Clock Enable.
0	SATA_DEV_0_CLK_EN	R/W	1h	SATA Device 0 Clock Enable.

R091h (F81E003Ah) • FIFO Size Control

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	FIFO_SIZE_THRESH_SEL					FIFO_SIZE_THRESH											RSVD								PM_CTL_FIFO_FLOW_CTL_THRSH							
Default Value	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	0

Bits	Field Name	Read/ Write	Default Value	Description
31:27	FIFO_SIZE_THRESH_SEL	R/W	1Fh	FIFO Size Threshold Select. Selects the port FIFO size threshold that is to be read or written.
26:16	FIFO_SIZE_THRESH	R/W	01Eh	FIFO Size Threshold. For received DATA FIS from all device ports, the PM stores the data in FIFO, then sends the data to the host if the amount of free space in the FIFO is less than the FIFO size threshold. **0h:** 0x32 **1h:** 1x32 ⋮ ⋮ **1FFh:** 511x32
15:8	RSVD	R	00h	Reserved. Do not change the default value.
7:0	PM_CTL_FIFO_FLOW_CTL_THRSH	R/W	3Ah	PM Control FIFO Flow Control Threshold. For received DATA FIS from all device port, the PM stores the data into FIFO. when FIFO residue is less then this value, notify link layer to send HOLD **000h:** 0 double word **001h:** 1 double word ⋮ ⋮ **3Ah:** 58 double word (default) ⋮ ⋮ **Fh:** 255 double word

R092h (00000666h) • Memory Control

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD																				SEMB_1P_MEM_WTC		SEMB_1P_MEM_RTC		PORT_2P_MEM_WTC		PORT_2P_MEM_RTC		PM_CTL_2P_MEM_WTC		PM_CTL_2P_MEM_RTC	
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	0	0	1	1	0

Bits	Field Name	Read/ Write	Default Value	Description
31:12	RSVD	R	00000h	Reserved.
11:10	SEMB_1P_MEM_WTC	R/W	1h	SEMB 1P Memory WTC.
9:8	SEMB_1P_MEM_RTC	R/W	2h	SEMB 1P Memory RTC.
7:6	PORT_2P_MEM_WTC	R/W	1h	Device Port 2P Memory WTC.
5:4	PORT_2P_MEM_RTC	R/W	2h	Device Port 2P Memory RTC.
3:2	PM_CTL_2P_MEM_WTC	R/W	1h	PM Control Port 2P Memory WTC.
1:0	PM_CTL_2P_MEM_RTC	R/W	2h	PM Control Port 2P Memory RTC.

R093h (00888888h) • SATA Port PHY Control

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD								PORT4_PU	PORT4_SPD_SEL			PORT3_PU	PORT3_SPEED_SEL			PORT2_PU	PORT2_SPEED_SEL			PORT1_PU	PORT1_SPEED_SEL			PORT0_PU	PORT0_SPEED_SEL			HOST_PORT_PU	HOST_PORT_SPEED_SEL		
Default Value	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0

Bits	Field Name	Read/ Write	Default Value	Description
31:24	RSVD	R	00h	Reserved.
23	PORT4_PU	R/W	1h	Port 4 Power Up.
22:20	PORT4_SPD_SEL	R/W	0h	Port 4 Speed Select.
19	PORT3_PU	R/W	1h	Port3 Power Up.
18:16	PORT3_SPEED_SEL	R/W	0h	Port3 Speed Select.
15	PORT2_PU	R/W	1h	Port2 Power Up.
14:12	PORT2_SPEED_SEL	R/W	0h	Port2 Speed Select.
11	PORT1_PU	R/W	1h	Port 1 Power Up.
10:8	PORT1_SPEED_SEL	R/W	0h	Port 1 Speed Select.
7	PORT0_PU	R/W	1h	Port 0 Power Up.
6:4	PORT0_SPEED_SEL	R/W	0h	Port 0 Speed Select.
3	HOST_PORT_PU	R/W	1h	Host Port Power Up.
2:0	HOST_PORT_SPEED_SEL	R/W	0h	Host Port Speed Select.

R0A0h (00000000h) • Side Bank Address Register

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	SPI_MEM_ACCESS	RSVD			UNIT_SEL				MEM_ADD																							
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field Name	Read/ Write	Default Value	Description
31	SPI_MEM_ACCESS	R/W	0h	Memory Access for SPI. **0h:** Other register access. **1h:** Read SPI memory.
30:28	RSVD	R/W	0h	Reserved. Do not change the default value.
27:24	UNIT_SEL	R/W	0h	Unit Select. **0h:** SPI controller register **1h:** UART controller register
23:0	MEM_ADD	R/W	000000h	Address for the Memory or Register.

R0A1h (00000000h) • Side Bank Data Register

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	SIDE_BANK_ACCESS																															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field Name	Read/ Write	Default Value	Description
31:0	SIDE_BANK_ACCESS	R/W	00000000h	Data Register of Side Bank Access.

8.3.3 Host Port PHY Event Counter Registers

R100h (00000000h) • Host Port PHY Event Counter 1

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	PHY_EVENT_CNT_1																															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field Name	Read/ Write	Default Value	Description
31:0	PHY_EVENT_CNT_1	R/W	00000000h	PHY Event Counter 1. This register contains both the counter identifier and the counter value: • Counter identifier: Read-only value 00002C01h. • Counter: 32-bit counter, contains number of signature D2H register FISes that were transmitted to the host from the control port.

8.3.4 General Purpose Input/Output (GPIO) Registers

R3A0h (00000000h) • GPIO Data Out

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD												GPIO[19:0]_DATA_OUTPUT																				
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field Name	Read/ Write	Default Value	Description
31:20	RSVD	R	000h	Reserved.
19:0	GPIO[19:0]_DATA_OUTPUT	R/W	00000h	GPIO[19:0] Data Output. When GPIO is in output mode, modify this register to control the output value.

R3A4h (000107C0h) • GPIO Data Out Enable

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	OUTPUT_EN_POLARITY	RSVD											GPIO_OUTPUT_EN																			
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0

Bits	Field Name	Read/ Write	Default Value	Description
31	OUTPUT_EN_POLARITY	R	0h	Output Enable Polarity. **0h:** Positive **1h:** Negative GPIO_OUTPUT_EN (R3A4h [19:0]) is reversed.
30:20	RSVD	R	000h	Reserved.

Bits	Field Name	Read/ Write	Default Value	Description
19:0	GPIO_OUTPUT_EN	R/W	107C0h	GPIO Output Enable. GPIO 6, 7, 8, 9, 10, and 16 are enabled by default.

R3A8h (00000000h) • GPIO Blink Enable

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD												GPIO[19:11]_BLINKING_EN									GPIO[10:5]_BLINKING_DIS						GPIO[4:0]_BLINKING_EN				
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field Name	Read/ Write	Default Value	Description
31:20	RSVD	R	000h	Reserved.
19:11	GPIO[19:11]_BLINKING_EN	R/W	000h	GPIO[19:11] Blinking Enable. **0h:** Disable **1h:** Enable
10:5	GPIO[10:5]_BLINKING_DIS	R/W	00h	GPIO[10:5] Blinking Disable. **0h:** Enable **1h:** Disable
4:0	GPIO[4:0]_BLINKING_EN	R/W	00h	GPIO[4:0] Blinking Enable. **0h:** Disable **1h:** Enable

R3ACh (00000000h) • GPIO Data In Polarity

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD												GPIO_DATA_INPUT_POLARITY_BIT_MAP																				
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field Name	Read/ Write	Default Value	Description
31:20	RSVD	R	000h	Reserved.
19:0	GPIO_DATA_INPUT_POLARITY_BIT_MAP	R/W	00000h	GPIO Data Input Polarity Bit Map. **0h:** Positive polarity **1h:** Negative polarity

R3B0h (00000000h) • GPIO Data In

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD												GPIO_INPUT_DATA_BIT_MAP																				
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field Name	Read/ Write	Default Value	Description
31:20	RSVD	R	000h	Reserved.
19:0	GPIO_INPUT_DATA_BIT_MAP	R/W	00000h	GPIO Input Data Bit Map.

R3C4h (2AF624C3h) • GPIO [6] through GPIO [11] Port Source Select

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD		GPIO[11]_OUTPUT_SRC_SEL					GPIO[10]_OUTPUT_SRC_SEL					GPIO[9]_OUTPUT_SRC_SEL					GPIO[8]_OUTPUT_SRC_SEL					GPIO[7]_OUTPUT_SRC_SEL					GPIO[6]_OUTPUT_SRC_SEL				
Default Value	0	0	1	0	1	0	1	0	1	1	1	1	0	1	1	0	0	0	1	0	0	1	0	0	1	1	0	0	0	0	1	1

Bits	Field Name	Read/ Write	Default Value	Description
31:30	RSVD	R	0h	Reserved.
29:25	GPIO[11]_OUTPUT_SRC_SEL	R/W	15h	GPIO [11] Output Source Select. **0h:** SATA 0_LINK and SATA 0_ACT or SATA 1_LINK and SATA 1_ACT or SATA 2_LINK and SATA 2_ACT or SATA 3_LINK and SATA 3_ACT or SATA 4_LINK and SATA 4_ACT **1h:** SATA 0_ACT or SATA 1_ACT or SATA 2_ACT or SATA 3_ACT or SATA 4_ACT **2h:** SATA 0_LINK or SATA 1_LINK or SATA 2_LINK or SATA 3_LINK or SATA 4_LINK **3h:** SATA 0_LINK and SATA 0_ACT **4h:** SATA 0_ACT **5h:** SATA 0_LINK **6h:** SATA 1_LINK and SATA 1_ACT **7h:** SATA 1_ACT **8h:** SATA 1_LINK **9h:** SATA 2_LINK and SATA 2_ACT **Ah:** SATA 2_ACT **Bh:** SATA 2_LINK **Ch:** SATA 3_LINK and SATA3_ACT **Dh:** SATA 3_ACT **Eh:** SATA 3_LINK **Fh:** SATA 4_LINK and SATA4_ACT **10h:** SATA 4_ACT **11h:** SATA 4_LINK **12h:** SATA H_LINK and SATA H_ACT **13h:** SATA H_ACT **14h:** SATA H_LINK **15h:** GPIO_DATA_OUT[11]

Bits	Field Name	Read/ Write	Default Value	Description
24:20	GPIO[10]_OUTPUT_SRC_SEL	R/W	0Fh	GPIO [10] Output Source Select. **0h:** SATA 0_LINK and SATA 0_ACT or SATA 1_LINK and SATA 1_ACT or SATA 2_LINK and SATA 2_ACT or SATA 3_LINK and SATA 3_ACT or SATA 4_LINK and SATA 4_ACT **1h:** SATA 0_ACT or SATA 1_ACT or SATA 2_ACT or SATA 3_ACT or SATA 4_ACT **2h:** SATA 0_LINK or SATA 1_LINK or SATA 2_LINK or SATA 3_LINK or SATA 4_LINK **3h:** SATA 0_LINK and SATA 0_ACT **4h:** SATA 0_ACT **5h:** SATA 0_LINK **6h:** SATA 1_LINK and SATA 1_ACT **7h:** SATA 1_ACT **8h:** SATA 1_LINK **9h:** SATA 2_LINK and SATA 2_ACT **Ah:** SATA 2_ACT **Bh:** SATA 2_LINK **Ch:** SATA 3_LINK and SATA3_ACT **Dh:** SATA 3_ACT **Eh:** SATA 3_LINK **Fh:** SATA 4_LINK and SATA4_ACT **10h:** SATA 4_ACT **11h:** SATA 4_LINK **12h:** SATA H_LINK and SATA H_ACT **13h:** SATA H_ACT **14h:** SATA H_LINK **15h:** GPIO_DATA_OUT[10]

Bits	Field Name	Read/ Write	Default Value	Description
19:15	GPIO[9]_OUTPUT_SRC_SEL	R/W	0Ch	GPIO [9] Output Source Select. **0h:** SATA 0_LINK and SATA 0_ACT or SATA 1_LINK and SATA 1_ACT or SATA 2_LINK and SATA 2_ACT or SATA 3_LINK and SATA 3_ACT or SATA 4_LINK and SATA 4_ACT **1h:** SATA 0_ACT or SATA 1_ACT or SATA 2_ACT or SATA 3_ACT or SATA 4_ACT **2h:** SATA 0_LINK or SATA 1_LINK or SATA 2_LINK or SATA 3_LINK or SATA 4_LINK **3h:** SATA 0_LINK and SATA 0_ACT **4h:** SATA 0_ACT **5h:** SATA 0_LINK **6h:** SATA 1_LINK and SATA 1_ACT **7h:** SATA 1_ACT **8h:** SATA 1_LINK **9h:** SATA 2_LINK and SATA 2_ACT **Ah:** SATA 2_ACT **Bh:** SATA 2_LINK **Ch:** SATA 3_LINK and SATA3_ACT **Dh:** SATA 3_ACT **Eh:** SATA 3_LINK **Fh:** SATA 4_LINK and SATA4_ACT **10h:** SATA 4_ACT **11h:** SATA 4_LINK **12h:** SATA H_LINK and SATA H_ACT **13h:** SATA H_ACT **14h:** SATA H_LINK **15h:** GPIO_DATA_OUT[9]

Bits	Field Name	Read/ Write	Default Value	Description
14:10	GPIO[8]_OUTPUT_SRC_SEL	R/W	09h	GPIO [8] Output Source Select. **0h:** SATA 0_LINK and SATA 0_ACT or SATA 1_LINK and SATA 1_ACT or SATA 2_LINK and SATA 2_ACT or SATA 3_LINK and SATA 3_ACT or SATA 4_LINK and SATA 4_ACT **1h:** SATA 0_ACT or SATA 1_ACT or SATA 2_ACT or SATA 3_ACT or SATA 4_ACT **2h:** SATA 0_LINK or SATA 1_LINK or SATA 2_LINK or SATA 3_LINK or SATA 4_LINK **3h:** SATA 0_LINK and SATA 0_ACT **4h:** SATA 0_ACT **5h:** SATA 0_LINK **6h:** SATA 1_LINK and SATA 1_ACT **7h:** SATA 1_ACT **8h:** SATA 1_LINK **9h:** SATA 2_LINK and SATA 2_ACT **Ah:** SATA 2_ACT **Bh:** SATA 2_LINK **Ch:** SATA 3_LINK and SATA3_ACT **Dh:** SATA 3_ACT **Eh:** SATA 3_LINK **Fh:** SATA 4_LINK and SATA4_ACT **10h:** SATA 4_ACT **11h:** SATA 4_LINK **12h:** SATA H_LINK and SATA H_ACT **13h:** SATA H_ACT **14h:** SATA H_LINK **15h:** GPIO_DATA_OUT[8]

Bits	Field Name	Read/ Write	Default Value	Description
9:5	GPIO[7]_OUTPUT_SRC_SEL	R/W	06h	GPIO [7] Output Source Select. **0h:** SATA 0_LINK and SATA 0_ACT or SATA 1_LINK and SATA 1_ACT or SATA 2_LINK and SATA 2_ACT or SATA 3_LINK and SATA 3_ACT or SATA 4_LINK and SATA 4_ACT **1h:** SATA 0_ACT or SATA 1_ACT or SATA 2_ACT or SATA 3_ACT or SATA 4_ACT **2h:** SATA 0_LINK or SATA 1_LINK or SATA 2_LINK or SATA 3_LINK or SATA 4_LINK **3h:** SATA 0_LINK and SATA 0_ACT **4h:** SATA 0_ACT **5h:** SATA 0_LINK **6h:** SATA 1_LINK and SATA 1_ACT **7h:** SATA 1_ACT **8h:** SATA 1_LINK **9h:** SATA 2_LINK and SATA 2_ACT **Ah:** SATA 2_ACT **Bh:** SATA 2_LINK **Ch:** SATA 3_LINK and SATA3_ACT **Dh:** SATA 3_ACT **Eh:** SATA 3_LINK **Fh:** SATA 4_LINK and SATA4_ACT **10h:** SATA 4_ACT **11h:** SATA 4_LINK **12h:** SATA H_LINK and SATA H_ACT **13h:** SATA H_ACT **14h:** SATA H_LINK **15h:** GPIO_DATA_OUT[7]

Bits	Field Name	Read/ Write	Default Value	Description
4:0	GPIO[6]_OUTPUT_SRC_SEL	R/W	03h	GPIO [6] Output Source Select. **0h:** SATA 0_LINK and SATA 0_ACT or SATA 1_LINK and SATA 1_ACT or SATA 2_LINK and SATA 2_ACT or SATA 3_LINK and SATA 3_ACT or SATA 4_LINK and SATA 4_ACT **1h:** SATA 0_ACT or SATA 1_ACT or SATA 2_ACT or SATA 3_ACT or SATA 4_ACT **2h:** SATA 0_LINK or SATA 1_LINK or SATA 2_LINK or SATA 3_LINK or SATA 4_LINK **3h:** SATA 0_LINK and SATA 0_ACT **4h:** SATA 0_ACT **5h:** SATA 0_LINK **6h:** SATA 1_LINK and SATA 1_ACT **7h:** SATA 1_ACT **8h:** SATA 1_LINK **9h:** SATA 2_LINK and SATA 2_ACT **Ah:** SATA 2_ACT **Bh:** SATA 2_LINK **Ch:** SATA 3_LINK and SATA3_ACT **Dh:** SATA 3_ACT **Eh:** SATA 3_LINK **Fh:** SATA 4_LINK and SATA4_ACT **10h:** SATA 4_ACT **11h:** SATA 4_LINK **12h:** SATA H_LINK and SATA H_ACT **13h:** SATA H_ACT **14h:** SATA H_LINK **15h:** GPIO_DATA_OUT[6]

R3C8h (047868C0h) • Power-Control Logic Time-Out Control Register

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD			TIMEOUT_CNTR_VAL																												
Default Value	0	0	0	0	0	1	0	0	0	1	1	1	1	0	0	0	0	1	1	0	1	0	0	0	1	1	0	0	0	0	0	0

Bits	Field Name	Read/ Write	Default Value	Description
31:29	RSVD	R	0h	Reserved.
28:0	TIMEOUT_CNTR_VAL	R/W	047868C0h	Time-out Counter Value. The time-out counter value based on 25 MHz clock.

R3D8h (255AD6B5h) • GPIO [0] through GPIO [5] Port Source Select

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD		GPIO[5]_OUTPUT_SRC_SEL					GPIO[4]_OUTPUT_SRC_SEL					GPIO[3]_OUTPUT_SRC_SEL					GPIO[2]_OUTPUT_SRC_SEL					GPIO[1]_OUTPUT_SRC_SEL					GPIO[0]_OUTPUT_SRC_SEL				
Default Value	0	0	1	0	0	1	0	1	0	1	0	1	1	0	1	0	1	1	0	1	0	1	1	0	1	0	1	1	0	1	0	1

Bits	Field Name	Read/ Write	Default Value	Description
31:30	RSVD	R	0h	Reserved.
29:25	GPIO[5]_OUTPUT_SRC_SEL	R/W	12h	GPIO [5] Output Source Select. **0h:** SATA0_LINK and SATA0_ACT or SATA1_LINK and SATA1_ACT or SATA2_LINK and SATA2_ACT or SATA3_LINK and SATA3_ACT or SATA4_LINK and SATA4_ACT. **1h:** SATA 0_ACT or SATA 1_ACT or SATA 2_ACT or SATA 3_ACT or SATA 4_ACT. **2h:** SATA 0_LINK or SATA 1_LINK or SATA 2_LINK or SATA 3_LINK or SATA 4_LINK. **3h:** SATA 0_LINK and SATA 0_ACT **4h:** SATA 0_ACT **5h:** SATA 0_LINK **6h:** SATA 1_LINK and SATA 1_ACT **7h:** SATA 1_ACT **8h:** SATA 1_LINK **9h:** SATA 2_LINK and SATA 2_ACT **Ah:** SATA 2_ACT **Bh:** SATA 2_LINK **Ch:** SATA 3_LINK and SATA3_ACT **Dh:** SATA 3_ACT **Eh:** SATA 3_LINK **Fh:** SATA 4_LINK and SATA4_ACT **10h:** SATA 4_ACT **11h:** SATA 4_LINK **12h:** SATA H_LINK and SATA H_ACT **13h:** SATA H_ACT **14h:** SATA H_LINK **15h:** GPIO_DATA_OUT[5]

Bits	Field Name	Read/ Write	Default Value	Description
24:20	GPIO[4]_OUTPUT_SRC_SEL	R/W	15h	GPIO [4] Output Source Select. **0h:** SATA0_LINK and SATA0_ACT or SATA1_LINK and SATA1_ACT or SATA2_LINK and SATA2_ACT or SATA3_LINK and SATA3_ACT or SATA4_LINK and SATA4_ACT. **1h:** SATA 0_ACT or SATA 1_ACT or SATA 2_ACT or SATA 3_ACT or SATA 4_ACT. **2h:** SATA 0_LINK or SATA 1_LINK or SATA 2_LINK or SATA 3_LINK or SATA 4_LINK. **3h:** SATA 0_LINK and SATA 0_ACT **4h:** SATA 0_ACT **5h:** SATA 0_LINK **6h:** SATA 1_LINK and SATA 1_ACT **7h:** SATA 1_ACT **8h:** SATA 1_LINK **9h:** SATA 2_LINK and SATA 2_ACT **Ah:** SATA 2_ACT **Bh:** SATA 2_LINK **Ch:** SATA 3_LINK and SATA3_ACT **Dh:** SATA 3_ACT **Eh:** SATA 3_LINK **Fh:** SATA 4_LINK and SATA4_ACT **10h:** SATA 4_ACT **11h:** SATA 4_LINK **12h:** SATA H_LINK and SATA H_ACT **13h:** SATA H_ACT **14h:** SATA H_LINK **15h:** GPIO_DATA_OUT[4] **16h:** Send SDB 1µs pulse output **17h:** EM error

Bits	Field Name	Read/ Write	Default Value	Description
19:15	GPIO[3]_OUTPUT_SRC_SEL	R/W	15h	GPIO [3] Output Source Select. **0h:** SATA0_LINK and SATA0_ACT or SATA1_LINK and SATA1_ACT or SATA2_LINK and SATA2_ACT or SATA3_LINK and SATA3_ACT or SATA4_LINK and SATA4_ACT. **1h:** SATA 0_ACT or SATA 1_ACT or SATA 2_ACT or SATA 3_ACT or SATA 4_ACT. **2h:** SATA 0_LINK or SATA 1_LINK or SATA 2_LINK or SATA 3_LINK or SATA 4_LINK. **3h:** SATA 0_LINK and SATA 0_ACT **4h:** SATA 0_ACT **5h:** SATA 0_LINK **6h:** SATA 1_LINK and SATA 1_ACT **7h:** SATA 1_ACT **8h:** SATA 1_LINK **9h:** SATA 2_LINK and SATA 2_ACT **Ah:** SATA 2_ACT **Bh:** SATA 2_LINK **Ch:** SATA 3_LINK and SATA3_ACT **Dh:** SATA 3_ACT **Eh:** SATA 3_LINK **Fh:** SATA 4_LINK and SATA4_ACT **10h:** SATA 4_ACT **11h:** SATA 4_LINK **12h:** SATA H_LINK and SATA H_ACT **13h:** SATA H_ACT **14h:** SATA H_LINK **15h:** GPIO_DATA_OUT[3]

Bits	Field Name	Read/ Write	Default Value	Description
14:10	GPIO[2]_OUTPUT_SRC_SEL	R/W	15h	GPIO [2] Output Source Select. **0h:** SATA0_LINK and SATA0_ACT or SATA1_LINK and SATA1_ACT or SATA2_LINK and SATA2_ACT or SATA3_LINK and SATA3_ACT or SATA4_LINK and SATA4_ACT. **1h:** SATA 0_ACT or SATA 1_ACT or SATA 2_ACT or SATA 3_ACT or SATA 4_ACT. **2h:** SATA 0_LINK or SATA 1_LINK or SATA 2_LINK or SATA 3_LINK or SATA 4_LINK. **3h:** SATA 0_LINK and SATA 0_ACT **4h:** SATA 0_ACT **5h:** SATA 0_LINK **6h:** SATA 1_LINK and SATA 1_ACT **7h:** SATA 1_ACT **8h:** SATA 1_LINK **9h:** SATA 2_LINK and SATA 2_ACT **Ah:** SATA 2_ACT **Bh:** SATA 2_LINK **Ch:** SATA 3_LINK and SATA3_ACT **Dh:** SATA 3_ACT **Eh:** SATA 3_LINK **Fh:** SATA 4_LINK and SATA4_ACT **10h:** SATA 4_ACT **11h:** SATA 4_LINK **12h:** SATA H_LINK and SATA H_ACT **13h:** SATA H_ACT **14h:** SATA H_LINK **15h:** GPIO_DATA_OUT[2]

Bits	Field Name	Read/ Write	Default Value	Description
9:5	GPIO[1]_OUTPUT_SRC_SEL	R/W	15h	GPIO [1] Output Source Select. **0h:** SATA0_LINK and SATA0_ACT or SATA1_LINK and SATA1_ACT or SATA2_LINK and SATA2_ACT or SATA3_LINK and SATA3_ACT or SATA4_LINK and SATA4_ACT. **1h:** SATA 0_ACT or SATA 1_ACT or SATA 2_ACT or SATA 3_ACT or SATA 4_ACT. **2h:** SATA 0_LINK or SATA 1_LINK or SATA 2_LINK or SATA 3_LINK or SATA 4_LINK. **3h:** SATA 0_LINK and SATA 0_ACT **4h:** SATA 0_ACT **5h:** SATA 0_LINK **6h:** SATA 1_LINK and SATA 1_ACT **7h:** SATA 1_ACT **8h:** SATA 1_LINK **9h:** SATA 2_LINK and SATA 2_ACT **Ah:** SATA 2_ACT **Bh:** SATA 2_LINK **Ch:** SATA 3_LINK and SATA3_ACT **Dh:** SATA 3_ACT **Eh:** SATA 3_LINK **Fh:** SATA 4_LINK and SATA4_ACT **10h:** SATA 4_ACT **11h:** SATA 4_LINK **12h:** SATA H_LINK and SATA H_ACT **13h:** SATA H_ACT **14h:** SATA H_LINK **15h:** GPIO_DATA_OUT[1]

Bits	Field Name	Read/ Write	Default Value	Description
4:0	GPIO[0]_OUTPUT_SRC_SEL	R/W	15h	GPIO [0] Output Source Select. **0h:** SATA0_LINK and SATA0_ACT or SATA1_LINK and SATA1_ACT or SATA2_LINK and SATA2_ACT or SATA3_LINK and SATA3_ACT or SATA4_LINK and SATA4_ACT. **1h:** SATA 0_ACT or SATA 1_ACT or SATA 2_ACT or SATA 3_ACT or SATA 4_ACT. **2h:** SATA 0_LINK or SATA 1_LINK or SATA 2_LINK or SATA 3_LINK or SATA 4_LINK. **3h:** SATA 0_LINK and SATA 0_ACT **4h:** SATA 0_ACT **5h:** SATA 0_LINK **6h:** SATA 1_LINK and SATA 1_ACT **7h:** SATA 1_ACT **8h:** SATA 1_LINK **9h:** SATA 2_LINK and SATA 2_ACT **Ah:** SATA 2_ACT **Bh:** SATA 2_LINK **Ch:** SATA 3_LINK and SATA3_ACT **Dh:** SATA 3_ACT **Eh:** SATA 3_LINK **Fh:** SATA 4_LINK and SATA4_ACT **10h:** SATA 4_ACT **11h:** SATA 4_LINK **12h:** SATA H_LINK and SATA H_ACT **13h:** SATA H_ACT **14h:** SATA H_LINK **15h:** GPIO_DATA_OUT[0]

R3E0h (2A2AD6B5h) • GPIO[12] through GPIO[17] Port Source Select

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD		GPIO[17]_DATA_OUT					GPIO16_OUTPUT_SRC_SEL					GPIO[15]_DATA_OUT					GPIO[14]_OUTPUT_SRC_SEL					GPIO[13]_OUTPUT_SRC_SEL					GPIO[12]_OUTPUT_SRC_SEL				
Default Value	0	0	1	0	1	0	1	0	0	0	1	0	1	0	1	0	1	1	0	1	0	1	1	0	1	0	1	1	0	1	0	1

Bits	Field Name	Read/ Write	Default Value	Description
31:30	RSVD	R	0h	Reserved.
29:25	GPIO[17]_DATA_OUT	R/W	15h	GPIO [17] Data Out.
24:20	GPIO16_OUTPUT_SRC_SEL	R/W	02h	GPIO [16] Output Source Select. **2h:** System alert level output, em error output **15h:** GPIO_DATA_OUT[16]
19:15	GPIO[15]_DATA_OUT	R/W	15h	GPIO [15] Data Out.
14:10	GPIO[14]_OUTPUT_SRC_SEL	R/W	15h	GPIO [14] Output Source Select. **0h:** SATA0_LINK and SATA0_ACT or SATA1_LINK and SATA1_ACT or SATA2_LINK and SATA2_ACT or SATA3_LINK and SATA3_ACT or SATA4_LINK and SATA4_ACT. **1h:** SATA 0_ACT or SATA 1_ACT or SATA 2_ACT or SATA 3_ACT or SATA 4_ACT. **2h:** SATA 0_LINK or SATA 1_LINK or SATA 2_LINK or SATA 3_LINK or SATA 4_LINK. **3h:** SATA 0_LINK and SATA 0_ACT **4h:** SATA 0_ACT **5h:** SATA 0_LINK **6h:** SATA 1_LINK and SATA 1_ACT **7h:** SATA 1_ACT **8h:** SATA 1_LINK **9h:** SATA 2_LINK and SATA 2_ACT **Ah:** SATA 2_ACT **Bh:** SATA 2_LINK **Ch:** SATA 3_LINK and SATA3_ACT **Dh:** SATA 3_ACT **Eh:** SATA 3_LINK **Fh:** SATA 4_LINK and SATA4_ACT **10h:** SATA 4_ACT **11h:** SATA 4_LINK **12h:** SATA H_LINK and SATA H_ACT **13h:** SATA H_ACT **14h:** SATA H_LINK **15h:** GPIO_DATA_OUT[14]

Bits	Field Name	Read/ Write	Default Value	Description
9:5	GPIO[13]_OUTPUT_SRC_SEL	R/W	15h	GPIO [13] Output Source Select. **0h:** SATA0_LINK and SATA0_ACT or SATA1_LINK and SATA1_ACT or SATA2_LINK and SATA2_ACT or SATA3_LINK and SATA3_ACT or SATA4_LINK and SATA4_ACT. **1h:** SATA 0_ACT or SATA 1_ACT or SATA 2_ACT or SATA 3_ACT or SATA 4_ACT. **2h:** SATA 0_LINK or SATA 1_LINK or SATA 2_LINK or SATA 3_LINK or SATA 4_LINK. **3h:** SATA 0_LINK and SATA 0_ACT **4h:** SATA 0_ACT **5h:** SATA 0_LINK **6h:** SATA 1_LINK and SATA 1_ACT **7h:** SATA 1_ACT **8h:** SATA 1_LINK **9h:** SATA 2_LINK and SATA 2_ACT **Ah:** SATA 2_ACT **Bh:** SATA 2_LINK **Ch:** SATA 3_LINK and SATA3_ACT **Dh:** SATA 3_ACT **Eh:** SATA 3_LINK **Fh:** SATA 4_LINK and SATA4_ACT **10h:** SATA 4_ACT **11h:** SATA 4_LINK **12h:** SATA H_LINK and SATA H_ACT **13h:** SATA H_ACT **14h:** SATA H_LINK **15h:** GPIO_DATA_OUT[13]

Bits	Field Name	Read/ Write	Default Value	Description
4:0	GPIO[12]_OUTPUT_SRC_SEL	R/W	15h	GPIO [12] Output Source Select. **0h:** SATA0_LINK and SATA0_ACT or SATA1_LINK and SATA1_ACT or SATA2_LINK and SATA2_ACT or SATA3_LINK and SATA3_ACT or SATA4_LINK and SATA4_ACT. **1h:** SATA 0_ACT or SATA 1_ACT or SATA 2_ACT or SATA 3_ACT or SATA 4_ACT. **2h:** SATA 0_LINK or SATA 1_LINK or SATA 2_LINK or SATA 3_LINK or SATA 4_LINK. **3h:** SATA 0_LINK and SATA 0_ACT **4h:** SATA 0_ACT **5h:** SATA 0_LINK **6h:** SATA 1_LINK and SATA 1_ACT **7h:** SATA 1_ACT **8h:** SATA 1_LINK **9h:** SATA 2_LINK and SATA 2_ACT **Ah:** SATA 2_ACT **Bh:** SATA 2_LINK **Ch:** SATA 3_LINK and SATA3_ACT **Dh:** SATA 3_ACT **Eh:** SATA 3_LINK **Fh:** SATA 4_LINK and SATA4_ACT **10h:** SATA 4_ACT **11h:** SATA 4_LINK **12h:** SATA H_LINK and SATA H_ACT **13h:** SATA H_ACT **14h:** SATA H_LINK **15h:** GPIO_DATA_OUT[12]

R3E4h (000002B5h) • GPIO[18] through GPIO[19] Port Source Select

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD																						GPIO[19]_SRC_SEL					GPIO[18]_OUTPUT_SRC_SEL				
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	1	0	1	0	1

Bits	Field Name	Read/ Write	Default Value	Description
31:10	RSVD	R	000000h	Reserved.
9:5	GPIO[19]_SRC_SEL	R/W	15h	GPIO [19] Source Select. **1h:** POW_CTRL_IN **2h:** Reserved. ⋮ **14h:** Reserved. **15h:** GPIO_DATA_OUT[19]
4:0	GPIO[18]_OUTPUT_SRC_SEL	R/W	15h	GPIO [18] Output Source Select. **1h:** POW_CTRL_OUT **2h:** Reserved. ⋮ **14h:** Reserved. **15h:** GPIO_DATA_OUT[18]

R3E8h (00000041h) • Blink Rate Counter Register for SATA4 and Overall Link

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD																				CNTR_VAL_BLINK_RATE_SATA4						CNTR_VAL_BLINK_RATE					
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1

Bits	Field Name	Read/ Write	Default Value	Description
31:12	RSVD	R	00000h	Reserved.
11:6	CNTR_VAL_BLINK_RATE_SATA4	R/W	01h	Blink Rate Counter Value for SATA4. The counter value for blink rate based on 10 Hz clock for the following: • SATA4_ACT • SATA4_LINK • SATA4_ACT_LINK By default the blink period is 100 ms. (10 Hz blink rate)

Bits	Field Name	Read/ Write	Default Value	Description
5:0	CNTR_VAL_BLINK_RATE	R/W	01h	Blink Rate Counter Value. The counter value for blink rate based on 10 Hz clock for the following: • SATA0_ACT or SATA1_ACT or SATA2_ACT or SATA3_ACT or SATA4_ACT, • SATA0_LINK or SATA1_LINK or SATA2_LINK or SATA3_LINK or SATA4_LINK, • SATA0_LINK and SATA0_ACT or SATA1_LINK and SATA1_ACT or SATA2_LINK and SATA2_ACT or SATA3_LINK and SATA3_ACT or SATA4_LINK and SATA4_ACT By default the blink period is 100 ms. (10 Hz blink rate).

R3ECh (01041041h) • Blink Rate Counter Register for SATA0/1/2/3/H

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD		SATAH_CNTR_VAL_BLINK_RATE						SATA3_CNTR_VAL_BLINK_RATE						SATA2_CNTR_VAL_BLINK_RATE						SATA1_CNTR_VAL_BLINK_RATE						SATA0_CNTR_VAL_BLINK_RATE					
Default Value	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1

Bits	Field Name	Read/ Write	Default Value	Description
31:30	RSVD	R	0h	Reserved.
29:24	SATAH_CNTR_VAL_BLINK_RATE	R/W	01h	SATAH Blink Rate Counter Value. The counter value for blink rate based on 10 Hz clock for the following: • SATAH_ACT • SATAH_LINK • SATAH_ACT_LINK By default the blink period is 100 ms (10 Hz blink rate).
23:18	SATA3_CNTR_VAL_BLINK_RATE	R/W	01h	SATA3 Blink Rate Counter Value. The counter value for blink rate based on 10 Hz clock for the following: • SATA3_ACT • SATA3_LINK • SATA3_ACT_LINK By default the blink period is 100 ms (10 Hz blink rate).

Bits	Field Name	Read/ Write	Default Value	Description
17:12	SATA2_CNTR_VAL_BLINK_RATE	R/W	01h	SATA2 Blink Rate Counter Value. The counter value for blink rate based on 10 Hz clock for the following: • SATA2_ACT • SATA2_LINK • SATA2_ACT_LINK By default the blink period is 100 ms. (10 Hz blink rate)
11:6	SATA1_CNTR_VAL_BLINK_RATE	R/W	01h	SATA1 Blink Rate Counter Value. The counter value for blink rate based on 10 Hz clock for the following: • SATA1_ACT • SATA1_LINK • SATA1_ACT_LINK By default the blink period is 100 ms. (10 Hz blink rate)
5:0	SATA0_CNTR_VAL_BLINK_RATE	R/W	01h	SATA0 Blink Rate Counter Value. The counter value for blink rate based on 10Hz clock for the following: • SATA0_ACT • SATA0_LINK • SATA0_ACT_LINK By default the blink period is 100 ms. (10 Hz blink rate)

R3F0h (01041041h) • Blink Rate Counter Register for GPIO_OUT[4] through GPIO_OUT[0]

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD		GPIO[4]_CNTR_VAL_BLINK_RATE						GPIO[3]_CNTR_VAL_BLINK_RATE						GPIO[2]_CNTR_VAL_BLINK_RATE						GPIO[1]_CNTR_VAL_BLINK_RATE						GPIO[0]_CNTR_VAL_BLINK_RATE					
Default Value	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1

Bits	Field Name	Read/ Write	Default Value	Description
31:30	RSVD	R	0h	Reserved.
29:24	GPIO[4]_CNTR_VAL_BLINK_RATE	R/W	01h	GPIO_OUT[4] Counter Value Blink Rate. This field indicates the counter value for GPIO_OUT[4] blink rate based on 10Hz clock. By default the blink period is 100 ms. (10 Hz blink rate).
23:18	GPIO[3]_CNTR_VAL_BLINK_RATE	R/W	01h	GPIO_OUT[3] Counter Value Blink Rate. This field indicates the counter value for GPIO_OUT[3] blink rate based on 10Hz clock. By default the blink period is 100 ms. (10 Hz blink rate).
17:12	GPIO[2]_CNTR_VAL_BLINK_RATE	R/W	01h	GPIO_OUT[2] Counter Value Blink Rate. This field indicates the counter value for GPIO_OUT[2] blink rate based on 10 Hz clock. By default the blink period is 100 ms. (10 Hz blink rate).

Bits	Field Name	Read/ Write	Default Value	Description
11:6	GPIO[1]_CNTR_VAL_ BLINK_RATE	R/W	01h	GPIO_OUT[1] Counter Value Blink Rate. This field indicates the counter value for GPIO_OUT[1] blink rate based on 10Hz clock. By default the blink period is 100ms. (10Hz blink rate).
5:0	GPIO[0]_CNTR_VAL_ BLINK_RATE	R/W	01h	GPIO_OUT[0] Counter Value Blink Rate. This field indicates the counter value for GPIO_OUT[0] blink rate based on 10Hz clock. By default the blink period is 100 ms. (10 Hz blink rate)

R3F4h (01041041h) • Blink Rate Counter Register for GPIO_OUT[9] through GPIO_OUT[5]

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD		GPIO[9]_CNTR_VAL_BLINK_RATE						GPIO[8]_CNTR_VAL_BLINK_RATE						GPIO[7]_CNTR_VAL_BLINK_RATE						GPIO[6]_CNTR_VAL_BLINK_RATE						GPIO[5]_CNTR_VAL_BLINK_RATE					
Default Value	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1

Bits	Field Name	Read/ Write	Default Value	Description
31:30	RSVD	R	0h	Reserved.
29:24	GPIO[9]_CNTR_VAL_ BLINK_RATE	R/W	01h	GPIO_OUT[9] Counter Value Blink Rate. This field indicates the counter value for GPIO_OUT[9] blink rate based on 10 Hz clock. By default the blink period is 100 ms. (10 Hz blink rate).
23:18	GPIO[8]_CNTR_VAL_ BLINK_RATE	R/W	01h	GPIO_OUT[8] Counter Value Blink Rate. This field indicates the counter value for GPIO_OUT[8] blink rate based on 10Hz clock. By default the blink period is 100 ms. (10 Hz blink rate).
17:12	GPIO[7]_CNTR_VAL_ BLINK_RATE	R/W	01h	GPIO_OUT[7] Counter Value Blink Rate. This field indicates the counter value for GPIO_OUT[7] blink rate based on 10 Hz clock. By default the blink period is 100 ms. (10 Hz blink rate).
11:6	GPIO[6]_CNTR_VAL_ BLINK_RATE	R/W	01h	GPIO_OUT[6] Counter Value Blink Rate. This field indicates the counter value for GPIO_OUT[6] blink rate based on 10Hz clock. By default the blink period is 100ms. (10Hz blink rate).
5:0	GPIO[5]_CNTR_VAL_ BLINK_RATE	R/W	01h	GPIO_OUT[5] Counter Value Blink Rate. This field indicates the counter value for GPIO_OUT[5] blink rate based on 10Hz clock. By default the blink period is 100 ms. (10 Hz blink rate)

R3F8h (01041041h) • Blink Rate Counter Register for GPIO_OUT[14] through GPIO_OUT[10]

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD		GPIO[14]_CNTR_VAL_BLINK_RATE						GPIO[13]_CNTR_VAL_BLINK_RATE						GPIO[12]_CNTR_VAL_BLINK_RATE						GPIO[11]_CNTR_VAL_BLINK_RATE						GPIO[10]_CNTR_VAL_BLINK_RATE					
Default Value	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1

Bits	Field Name	Read/ Write	Default Value	Description
31:30	RSVD	R	0h	Reserved.
29:24	GPIO[14]_CNTR_VAL_BLINK_RATE	R/W	01h	GPIO_OUT[14] Counter Value Blink Rate. This field indicates the counter value for GPIO_OUT[14] blink rate based on 10 Hz clock. By default the blink period is 100 ms. (10 Hz blink rate).
23:18	GPIO[13]_CNTR_VAL_BLINK_RATE	R/W	01h	GPIO_OUT[13] Counter Value Blink Rate. This field indicates the counter value for GPIO_OUT[13] blink rate based on 10Hz clock. By default the blink period is 100 ms. (10 Hz blink rate).
17:12	GPIO[12]_CNTR_VAL_BLINK_RATE	R/W	01h	GPIO_OUT[12] Counter Value Blink Rate. This field indicates the counter value for GPIO_OUT[12] blink rate based on 10 Hz clock. By default the blink period is 100 ms. (10 Hz blink rate).
11:6	GPIO[11]_CNTR_VAL_BLINK_RATE	R/W	01h	GPIO_OUT[11] Counter Value Blink Rate. This field indicates the counter value for GPIO_OUT[11] blink rate based on 10Hz clock. By default the blink period is 100ms. (10Hz blink rate).
5:0	GPIO[10]_CNTR_VAL_BLINK_RATE	R/W	01h	GPIO_OUT[10] Counter Value Blink Rate. This field indicates the counter value for GPIO_OUT[10] blink rate based on 10Hz clock. By default the blink period is 100 ms. (10 Hz blink rate)

R3FCh (01041041h) • Blink Rate Counter Register for GPIO_OUT[19] through GPIO_OUT[15]

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD		GPIO[19]_CNTR_VAL_BLINK_RATE						GPIO[18]_CNTR_VAL_BLINK_RATE						GPIO[17]_CNTR_VAL_BLINK_RATE						GPIO[16]_CNTR_VAL_BLINK_RATE						GPIO[15]_CNTR_VAL_BLINK_RATE					
Default Value	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1

Bits	Field Name	Read/ Write	Default Value	Description
31:30	RSVD	R	0h	Reserved.
29:24	GPIO[19]_CNTR_VAL_BLINK_RATE	R/W	01h	GPIO_OUT[19] Counter Value Blink Rate. This field indicates the counter value for GPIO_OUT[19] blink rate based on 10 Hz clock. By default the blink period is 100 ms. (10 Hz blink rate).
23:18	GPIO[18]_CNTR_VAL_BLINK_RATE	R/W	01h	GPIO_OUT[18] Counter Value Blink Rate. This field indicates the counter value for GPIO_OUT[18] blink rate based on 10Hz clock. By default the blink period is 100 ms. (10 Hz blink rate).

Bits	Field Name	Read/ Write	Default Value	Description
17:12	GPIO[17]_CNTR_VAL_ BLINK_RATE	R/W	01h	GPIO_OUT[17] Counter Value Blink Rate. This field indicates the counter value for GPIO_OUT[17] blink rate based on 10 Hz clock. By default the blink period is 100 ms. (10 Hz blink rate).
11:6	GPIO[16]_CNTR_VAL_ BLINK_RATE	R/W	01h	GPIO_OUT[16] Counter Value Blink Rate. This field indicates the counter value for GPIO_OUT[16] blink rate based on 10Hz clock. By default the blink period is 100ms. (10Hz blink rate).
5:0	GPIO[15]_CNTR_VAL_ BLINK_RATE	R/W	01h	GPIO_OUT[15] Counter Value Blink Rate. This field indicates the counter value for GPIO_OUT[15] blink rate based on 10Hz clock. By default the blink period is 100 ms. (10 Hz blink rate)

8.3.5 SATA PHY and Link Registers

This section contains the following subsections:

- Link Registers
- SATA PHY—Low-Power SERDES PHY Registers

8.3.5.1 Link Registers

R00Eh (00002001h) • PHY Reserved Input Control

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD																						SSC_EN	TX_AMP_ADJ	RSVD							
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Name	Read/ Write	Default Value	Description
31:10	RSVD	R/W	000008h	Reserved. Do not change the default value.
9	SSC_EN	R/W	0h	Tx Spread Spectrum Enable. **0h:** Disable. **1h:** Enable.
8	TX_AMP_ADJ	R/W	0h	Transmitter Amplitude Adjust. For each reduction in range, additional power savings can be realized.
7:0	RSVD	R/W	01h	Reserved. Do not change the default value.

8.3.5.2 SATA PHY—Low-Power SERDES PHY Registers

R8Dh (C958h) • Generation 1 Setting 0

Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	G1_TX_SLEW_CTRL_EN	G1_TX_SLEW_RATE_SEL			G1_TX_EMPH_EN	G1_TX_EMPH_AMP				RSVD	G1_TX_AMP					RSVD
Default Value	1	1	0	0	1	0	0	1	0	1	0	1	1	0	0	0

Bits	Field Name	Read/ Write	Default Value	Description
15	G1_TX_SLEW_CTRL_EN	R/W	1h	Transmitter Slew Control Enable. This setting is used for 1.5 Gbps in SATA.
14:12	G1_TX_SLEW_RATE_SEL	R/W	4h	Transmitter Slew Rate Select. **0h:** Fastest edge ⋮ ⋮ **7h:** Slowest edge The difference between the slowest and the fastest setting is about 100 ps. This setting is used for 1.5 Gbps in SATA.
11	G1_TX_EMPH_EN	R/W	1h	Transmitter Emphasis Enable. This setting is used for 1.5 Gbps in SATA.
10:7	G1_TX_EMPH_AMP	R/W	2h	Transmitter Emphasis Amplitude. Approximately 4% per step at the package pin. **0h:** 4% **1h:** 8% ⋮ ⋮ **Ch:** 48% Settings Dh - Fh are not supported.
6	RSVD	R/W	1h	Reserved. Do not change the default value.
5:1	G1_TX_AMP	R/W	0Ch	Transmitter Amplitude. This setting is used for 1.5 Gbps in SATA.
0	RSVD	R/W	0h	Reserved. Do not change the default value.

R8Fh (AA62h) • Generation 2 Setting 0

Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	G2_TX_SLEW_CTRL_EN	G2_TX_SLEW_RATE_SEL			G2_TX_EMPH_EN	G2_TX_EMPH_AMP				RSVD	G2_TX_AMP					RSVD
Default Value	1	0	1	0	1	0	1	0	0	1	1	0	0	0	1	0

Bits	Field Name	Read/ Write	Default Value	Description
15	G2_TX_SLEW_CTRL_EN	R/W	1h	Transmitter Slew Control Enable. This setting is used for 3 Gbps in SATA.

Bits	Field Name	Read/ Write	Default Value	Description
14:12	G2_TX_SLEW_RATE_SEL	R/W	2h	Transmitter Slew Rate Select. **0h:** Fastest edge ⋮ ⋮ **7h:** Slowest edge The difference between the slowest and the fastest setting is about 100 ps. This setting is used for 3 Gbps in SATA.
11	G2_TX_EMPH_EN	R/W	1h	Transmitter Emphasis Enable. This setting is used for 3 Gbps in SATA.
10:7	G2_TX_EMPH_AMP	R/W	4h	Transmitter Emphasis Amplitude. Approximately 4% per step at the package pin. **0h:** 4% **1h:** 8% ⋮ ⋮ **Ch:** 48% **Others:** Not supported.
6	RSVD	R/W	1h	Reserved. Do not change the default value.
5:1	G2_TX_AMP	R/W	11h	Transmitter Amplitude. This setting is used for 3 Gbps in SATA.
0	RSVD	R/W	0h	Reserved. Do not change the default value.

R91h (0BEBh) • Generation 3 Setting 0

Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	G3_TX_SLEW_CTRL_EN	G3_TX_SLEW_RATE_SEL			G3_TX_EMPH_EN	G3_TX_EMPH_AMP				RSVD	G3_TX_AMP					RSVD
Default Value	0	0	0	0	1	0	1	1	1	1	1	0	1	0	1	1

Bits	Field Name	Read/ Write	Default Value	Description
15	G3_TX_SLEW_CTRL_EN	R/W	0h	Transmitter Slew Control Enable. This setting is used for 6 Gbps in SATA.
14:12	G3_TX_SLEW_RATE_SEL	R/W	0h	Transmitter Slew Rate Select. **0h:** Fastest edge ⋮ ⋮ **7h:** Slowest edge The difference between the slowest and the fastest setting is about 100 ps This setting is used for 6 Gbps in SATA.

Bits	Field Name	Read/ Write	Default Value	Description
11	G3_TX_EMPH_EN	R/W	1h	Transmitter Emphasis Enable. This setting is used for 6 Gbps in SATA.
10:7	G3_TX_EMPH_AMP	R/W	7h	Transmitter Emphasis Amplitude. Approximately 4% per step at the package pin. **0h:** 4% **1h:** 8% ⋮ ⋮ **Ch:** 48% Settings Dh - Fh are not supported.
6	RSVD	R/W	1h	Reserved. Do not change the default value.
5:1	G3_TX_AMP	R/W	15h	Transmitter Amplitude. This setting is used for 6 Gbps in SATA.
0	RSVD	R/W	1h	Reserved. Do not change the default value.

8.3.6 Device Port PHY Event Counter Registers

R100h (00000000h) • Device Port PHY Event Counter 0

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	DEV_PORT_PHY_EVENT_CNTR_0																															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field Name	Read/ Write	Default Value	Description
31:0	DEV_PORT_PHY_EVENT_CNTR_0	R/W	00000000h	Device Port PHY Event Counter 0. This register contains both the identifier and the counter value. Counter identifier: 00002C00h. Counter: 32-bit counter, contains number of transmitted H2D non-data FISes to which the port multiplier responded with R_ERR due to collision.

R101h (00000000h) • Device Port PHY Event Counter 2

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	DEV_PORT_PHY_EVENT_CNTR_2																															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field Name	Read/ Write	Default Value	Description
31:0	DEV_PORT_PHY_EVENT_CNTR_2	R/W	00000000h	Device Port PHY Event Counter 2. This register contains both the identifier and the counter value. Counter identifier: 00002C02h. Counter: 32-bit counter, contains number of corrupted CRC values that were transmitted to the host.

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9 ELECTRICAL SPECIFICATIONS

This chapter contains the following sections:

9.1 Absolute Maximum Ratings

The following table describes the 88SM9705 absolute Maximum Ratings:

Table 9-1 Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Absolute Digital Power Supply Voltage	VDD_{ABS}		-0.5	1.0	1.1	V
Absolute Digital I/O pad Supply Voltage	$VDDIO_{ABS}$		-0.5	3.3	3.63	V
Absolute Analog Power Supply Voltage for Timebase Generators (TBG)	$VAA1_{ABS}$		-0.5	1.8	1.98	V
Absolute Analog Power Supply Voltage for PHY	$VAA2_{ABS}$		-0.5	1.8	1.98	V
Absolute Input Voltage	Vin_{ABS}		-0.4		vddio + 0.4	V
Absolute Storage Temperature	$Tstor_{ABS}$		-55		85	°C
Absolute Junction Temperature	$Tjunc_{ABS}$				125	°C

9.2 Power Requirements

The following table describes the 88SM9705 power requirements.

Table 9-2 Total Power Dissipation

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Absolute digital I/O pad power supply	I_{VDDIO}			20		mA
Absolute digital power supply	I_{VDD}			300		mA
Absolute analog power supply for TBG	I_{VAA1}			10		mA
Absolute analog power supply for PHY	I_{VAA2}			400		mA

9.3 Recommended/Typical Operating Conditions

Table 9-3 Recommended/Typical Operating Conditions

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Ambient Operating Temperature			0		70	°C
Junction Operating Temperature			0		125	°C
Operating Digital Power Supply Voltage	VDD_{OP}		1.0 - 5%	1.0	1.0 + 5%	V
Operating Digital I/O Pad Supply Voltage	$VDDIO_{OP}$		3.3 - 5%	3.3	3.3 + 5%	V
Operating Analog Power Supply Voltage for TBG	$VAA1_{OP}$		1.8 - 5%	1.8	1.8 + 5%	V
Operating Analog Power Supply Voltage for PHY	$VAA2_{OP}$		1.8 - 5%	1.8	1.8 + 5%	V

9.4 DC Characteristics

Table 9-4 DC Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Low Voltage	V_{IL}		-0.4		0.8	V
Input High Voltage	V_{IH}		2.0		VDDIO + 0.4	V
Output Low Voltage	V_{OL}	I_{OL}=4 mA, VDDP=3.3V	-0.4	0.13	0.4	V
Output High Voltage	V_{OH}	I_{OL}=-2 mA, VDDP=3.3V	2.4	3.3		V

9.5 Thermal Data

It is recommended to read application note AN-63 Thermal Management for Selected Marvell® Products and the ThetaJC, ThetaJA, and Temperature Calculations White Paper, available from Marvell, before designing a system. These documents describe the basic understanding of thermal management of integrated circuits (ICs) and guidelines to ensure optimal operating conditions for Marvell products.

Table 9-5 provides the thermal data for the 88SM9705. It shows the values for the package thermal parameters for the 84-lead Quad Flat Non-Lead package (QFN 84) mounted on a 4-layer PCB. The simulation was performed according to JEDEC standards.‘

Table 9-5 Package Thermal Data, 4-Layer PCB*

Parameter	Definition	Airflow Value			
		0 m/s	1 m/s	2 m/s	3 m/s
θ_{JA}	Thermal Resistance: Junction to Ambient	28.2 C/W	27.6C/W	26.5 C/W	25.8 C/W
θ_{JB}	Thermal Resistance: Junction to Board	16.70 C/W	–	–	–
θ_{JC}	Thermal Resistance: Junction to Case	14.90 C/W	–	–	–
Ψ_{JT}	Thermal Characterization: Junction to Top	0.48	0.78	0.94	1.05
Ψ_{JB}	Thermal Characterization: Junction to Board	16.5	16.4	16.3	16.2

* All data is based on parts mounted on a 3” x 4.5”, JEDEC 4L PCB.

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