

MARVELL® MSB0101 Connectivity South Bridge

Low-cost PCIe 3.0, USB 3.1 (Gen 1), or SATA III Connectivity

PRODUCT OVERVIEW

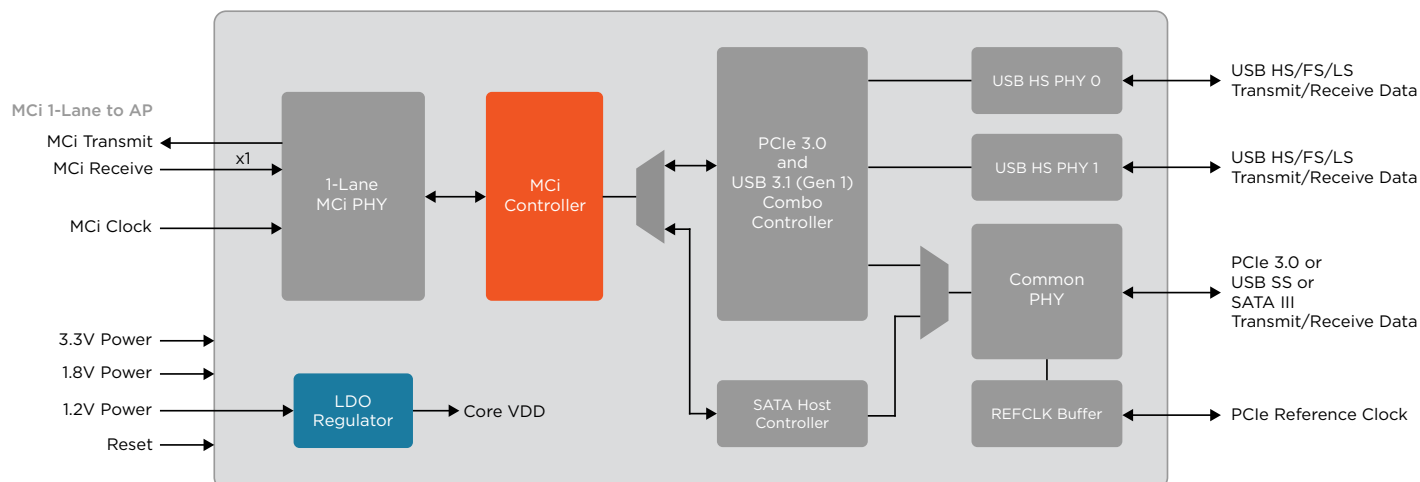
The Marvell® MSB0101 is a low-cost connectivity solution in Marvell's MoChi™ South Bridge (SB) family of products. The MSB0101 can be configured as a PCIe 3.0 controller in either Root Complex (RC) or Endpoint (EP) mode, a USB 3.1 (Gen 1) controller providing both Host or Device capabilities, or a SATA III Host controller. The table below shows the interface options available in the various operation modes of the MSB0101. Utilizing this MoChi solution offers developers many advantages, including: 1) scalability across product needs, 2) possibility to add/replace features with drastically improved time-to-market, and 3) flexibility in board placement.

MODE	SATA	PCIe	USB (SS and HS/Fs/LS*)		USB (HS/Fs/LS*)	
			HOST	DEVICE	HOST	DEVICE
SATA	✓	--	--	--	2 or 1	1
PCIe	--	✓	--	--	2 or 1	1
USB	Host	--	--	✓	1	--
	Device	--	--	--	✓	--

*LS not supported in device mode

The MSB0101 is connected through its single-lane MoChi Interconnect (MCi) interface to Marvell's MCi-enabled Application Processor (AP). The MCi interface is transparent and, therefore, MSB0101 appears to the application as an integrated function in the AP.

BLOCK DIAGRAM



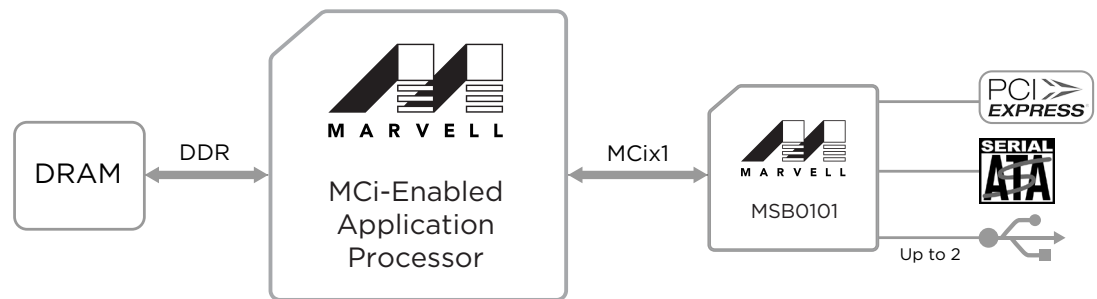
Marvell MSB0101 Block Diagram

KEY FEATURES AND BENEFITS

FEATURES		BENEFITS
Package		<ul style="list-style-type: none"> • Small footprint 4x4 mm QFN (32 pin, 0.4 mm pitch)
MCi Interface		<ul style="list-style-type: none"> • 1 lane (up to 8 Gbps) • 25, 26, 30, or 40 MHz shared MCi clock
Power Supply		<ul style="list-style-type: none"> • 1.2V, 1.8V, and 3.3V supplies required • Built in, on-chip LDO regulator for internal core supply
Low Power		<ul style="list-style-type: none"> • PCIe: L1 PM substates with clock support, Latency Tolerance Reporting (LTR) • USB 3.1: U1, U2, and U3 power management with remote wake up • Reference clock removal and power gating when in Sleep mode
PCIe Interface		<ul style="list-style-type: none"> • PCIe 3.1 compliance supporting speeds of 8 GT/s, 5 GT/s, and 2.5 GT/s • Supports dual-mode, RC, or EP • Separate Reference Clock with Independent Spread (SRIS) spectrum clocking
SATA Interface		<ul style="list-style-type: none"> • Compliant with SATA III • Hot-plug, asynchronous signal recovery
USB Controller	Host	<ul style="list-style-type: none"> • 1 SS/HS/FS/LS and 1 HS/FS/LS root hub port compliant with USB 3.1 (Gen 1) and xHCI 1.1 • Up to 32 device slots and 128 endpoints
	Device	<ul style="list-style-type: none"> • 1 SS/HS/FS port compliant with USB 3.1 (Gen 1) • Endpoints: 8 IN with 2 supporting bulk streaming, 8 OUT with 2 supporting bulk streaming, and 1 control

TARGET APPLICATIONS

- I/O expansion in any Marvell MoChi platform
- Imaging platforms (printers, cameras)
- Consumer electronic devices
- Digital entertainment (set-top boxes and DTV)
- Internet of Things (IoT)
- Gaming platforms
- Network devices (access points, mobile routers, network-attached servers)
- Personal computers (laptops)



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