



88SE9215 R1.1

One-Lane PCIe 2.0 to Four-Port 6
Gbps SATA I/O Controller

Datasheet

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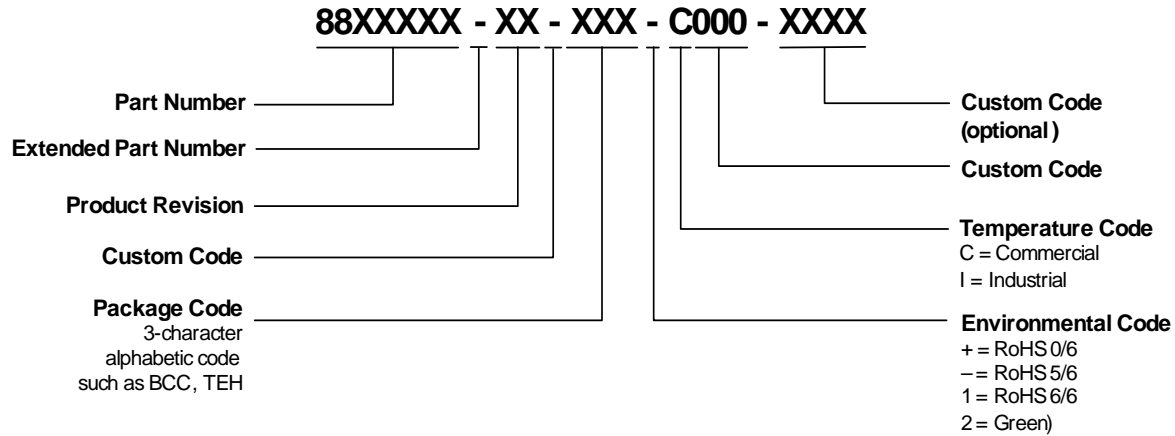
Patent(s) Pending—Products identified in this document may be covered by one or more Marvell patents and/or patent applications.

ORDERING INFORMATION

Ordering Part Numbers and Package Markings

The following figure shows the ordering part numbering scheme for the 88SE9215 part. For complete ordering information, contact your Marvell FAE or sales representative.

Sample Ordering Part Number



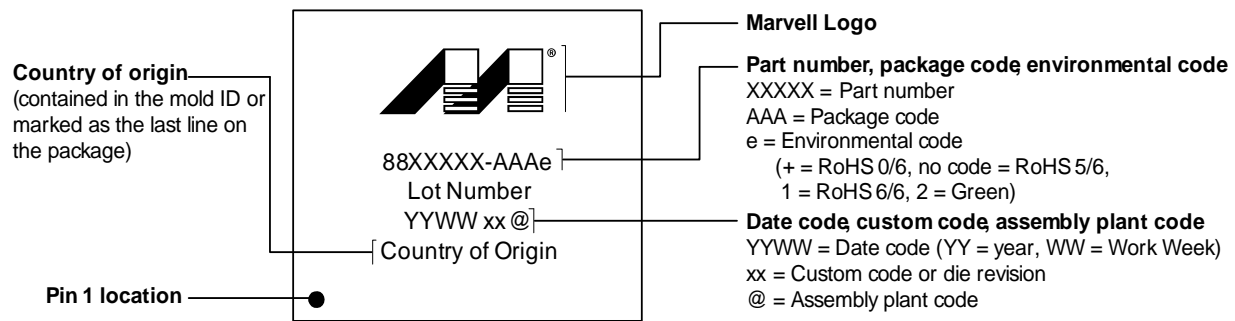
The standard ordering part numbers for the respective solutions are indicated in the following table.

Ordering Part Numbers

| Part Number | Description |
|---------------------|---|
| 88SE9215A1-NAA2C000 | 76-pin QFN 9 mm x 9 mm, One-Lane PCIe 2.0 to four-port 6 Gbps SATA Controller. |
| 88SE9215A1-NAA2I000 | 76-pin Industrial Grade QFN 9 mm x 9 mm, One-Lane PCIe 2.0 to four-port 6 Gbps SATA Controller. |

The next figure shows a typical Marvell package marking.

88SE9215 Package Marking and Pin 1 Location



Note: The above drawing is not drawn to scale. The location of markings is approximate. Add-on marks are not represented. Flip chips vary widely in their markings and flip chip examples are not shown here. For flip chips, the markings may be omitted per customer requirement.



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CHANGE HISTORY

The following table identifies the document change history for Rev. C.

Document Changes *

| Location | Type | Description | Date |
|----------|--------|--|------------------|
| Global | Update | Removed preliminary from document title. | January 25, 2016 |

* The type of change is categorized as: Parameter, Revision, or Update. A Parameter change is a change to a spec value, a Revision change is one that originates from the chip Revision Notice, and an Update change includes all other document updates.



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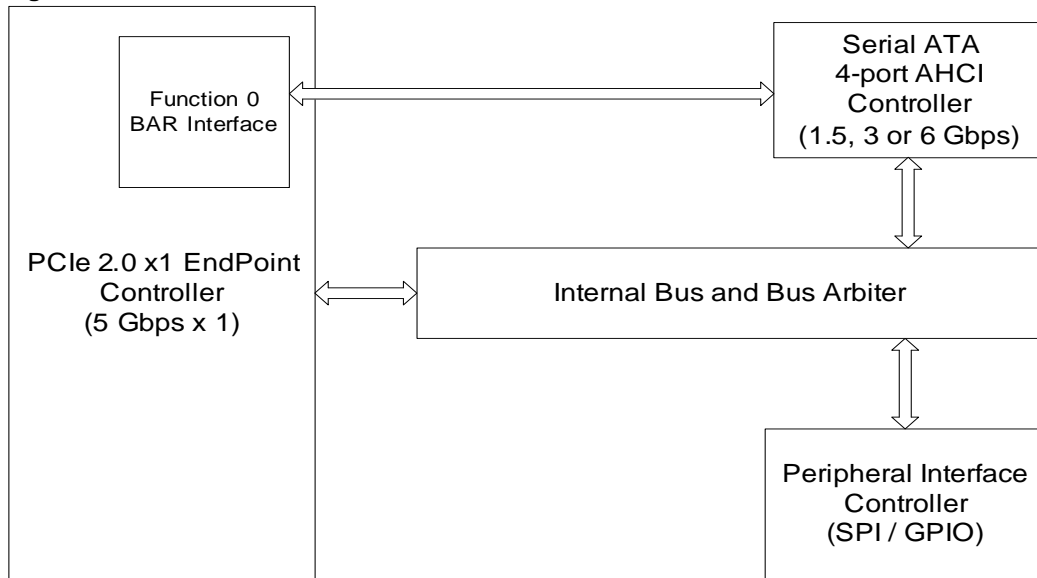
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1 OVERVIEW

The 88SE9215 is a four-port, 3 Gbps or 6 Gbps SATA Host Bus Adapter that provides a one-lane PCIe 2.0 interface and SATA controller functions. The 88SE9215 supplies four 6 Gbps SATA ports.

The 88SE9215 supports devices compliant with the Serial ATA International Organization: Serial ATA Revision 3.1 specification. Figure 1-1 shows the system block diagram.

Figure 1-1 SE9215 Architecture





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2 FEATURES

This chapter contains the following information:

- General
- PCIe
- SATA Controller
- SPI Interface Controller
- Peripheral Interface Controller



2.1 General

- 55 nm CMOS process, 1.0V digital core, 1.8V analog, and 3.3V I/O power supplies.
- Reference clock frequency of 25 MHz, provided by an external clock source or generated by an external crystal oscillator.

2.2 PCIe

- PCIe 2.0 endpoint device.
- Compliant with PCIe 2.0 specifications.
- Supports communication speed of 2.5 Gbps and 5 Gbps.
- Supports AHCI programming interface registers for the SATA controller.
- Supports aggressive power management.
- Supports error reporting, recovery and correction.
- Supports Message Signaled Interrupt (MSI).

2.3 SATA Controller

- Compliant with Serial ATA Specification 3.1.
- Supports communication speeds of 6 Gbps, 3 Gbps, and 1.5 Gbps.
- Supports programmable transmitter signal levels.
- Supports Gen 1i, Gen 1x, Gen 2i, Gen 2m, Gen 2x, and Gen 3i.
- Supports four SATA ports.
- Supports AHCI 1.0 programming interface.
- Supports Native Command Queuing (NCQ).
- Supports Port Multiplier FIS based switching or command based switching.
- Supports Partial and Slumber Power Management states.
- Supports Staggered Spin-up.

2.4 SPI Interface Controller

- A four-pin interface provides read and write access to an external SPI flash or SPI ROM device.
- Vendor specific information stored in the external device is read by the controller during the chip power-up.
- PCI BootROMs of PCIe function 0 can also be stored in the external SPI device and read through the Expansion ROM BAR and the SPI interface controller.



2.5 Peripheral Interface Controller

- Eight General Purpose I/O (GPIO) ports.
- Each of the GPIO pins can be assigned to act as a general input or output pin.
- Each of the GPIO inputs can be programmed to generate an edge-sensitive or a level-sensitive maskable interrupt.
- Each of the GPIO outputs can be programmed for a connected LED to blink at a user-defined fixed rate. The default rate is 100 ms.
-

3 PACKAGE

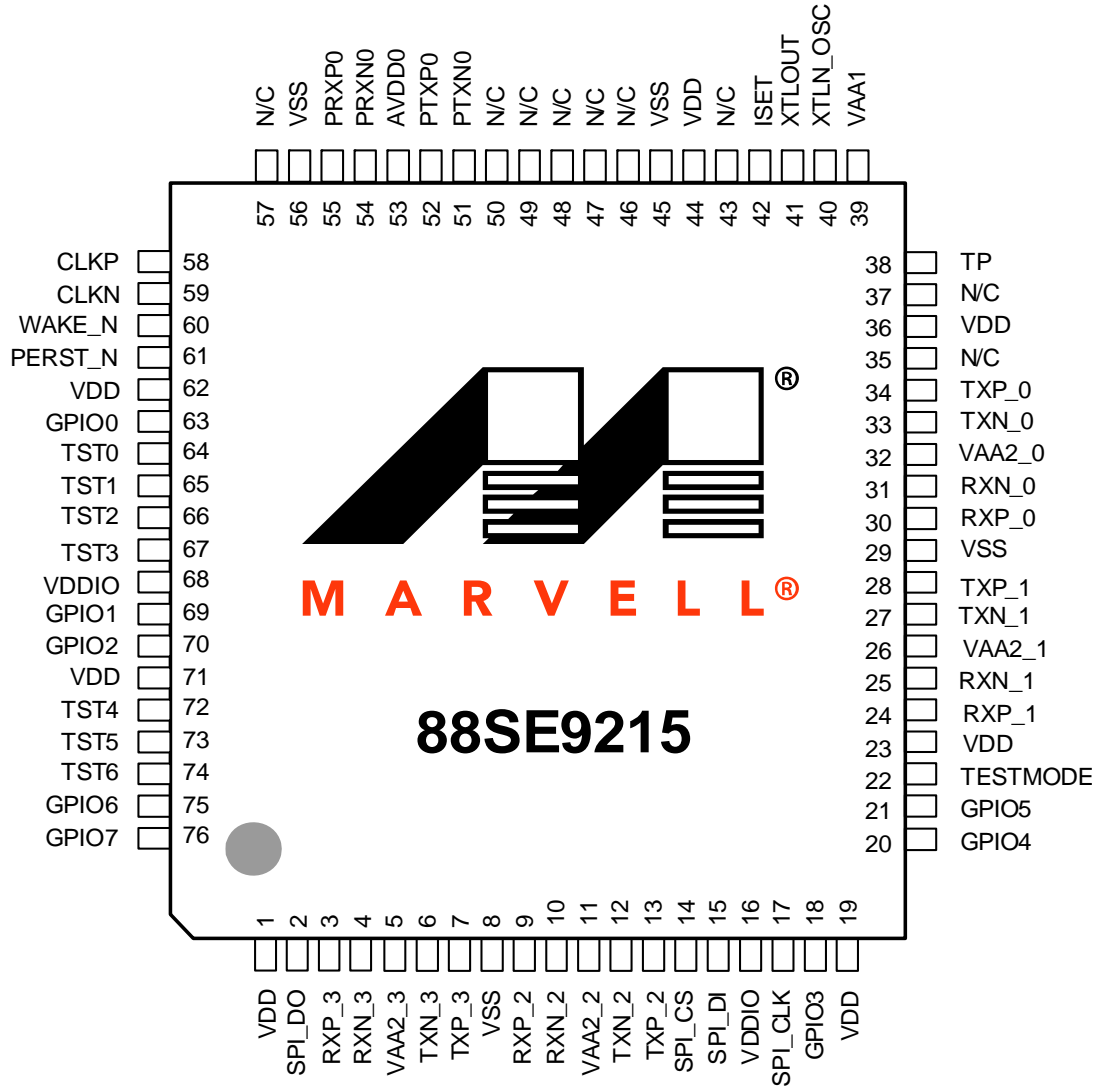
This chapter contains the following information:

- Pin Diagram
- Mechanical Dimensions
- Signal Descriptions

3.1 Pin Diagram

The 76-pin QFN pin diagram is illustrated in Figure 3-1.

Figure 3-1 SE9215 Pin Diagram

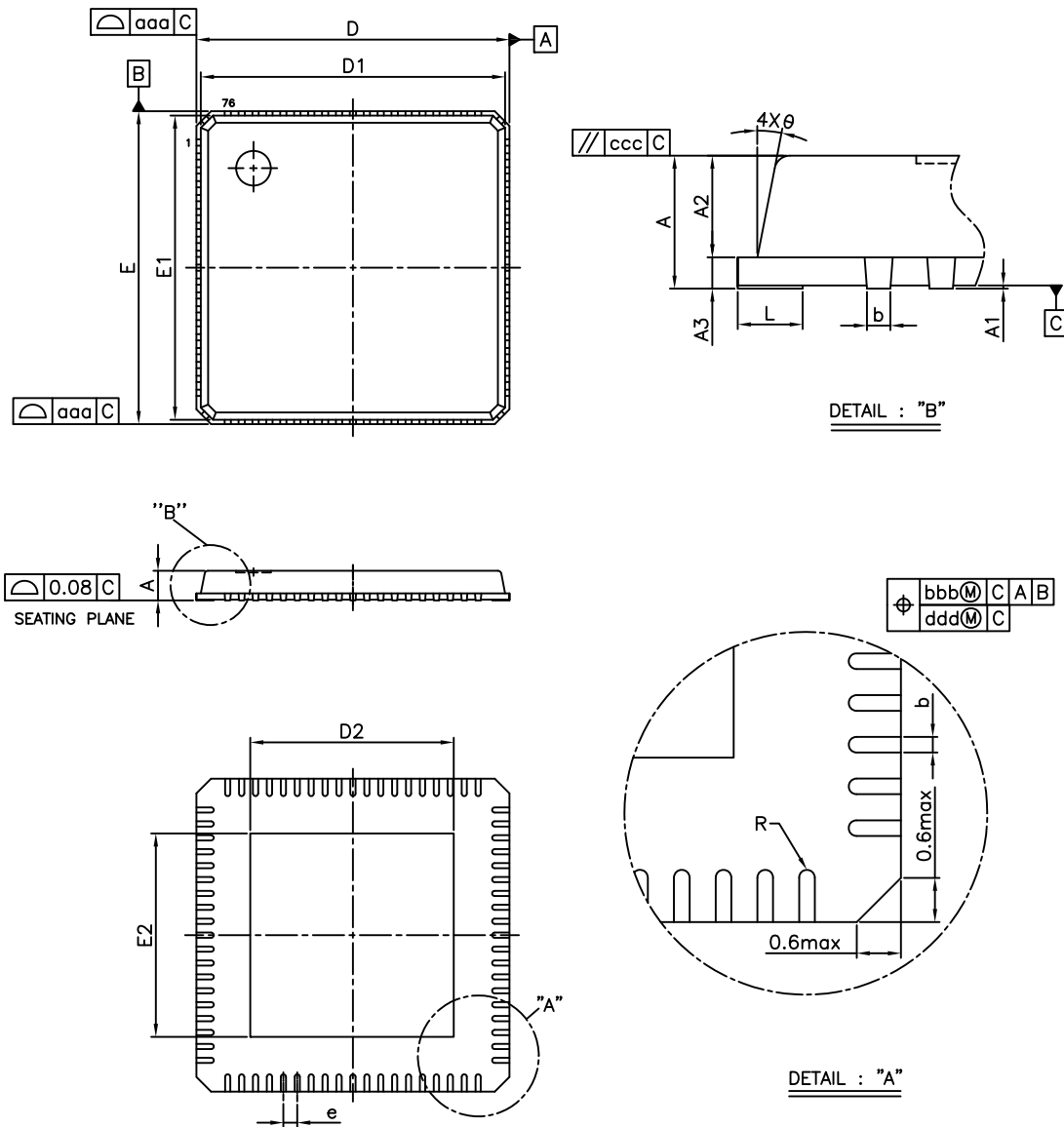


Note: The center area beneath the chip is the Exposed Die Pad (Epad). When designing the PCB, create a solder pad for the Epad and connect the Epad to ground.

3.2 Mechanical Dimensions

The package mechanical drawing is shown in Figure 3-2.

Figure 3-2 Package Mechanical Diagram



The package mechanical dimensions are shown in Figure .

Figure 3-3 Package Mechanical Dimensions

| Symbol | Dimension in mm | | | Dimension in inch | | |
|---------|-----------------|------|------|-------------------|-------|-------|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.80 | 0.85 | 1.00 | 0.031 | 0.033 | 0.039 |
| A1 | 0.00 | 0.02 | 0.05 | 0.000 | 0.001 | 0.002 |
| A2 | ---- | 0.65 | 1.00 | ---- | 0.026 | 0.039 |
| A3 | 0.20 REF | | | 0.008 REF | | |
| b | 0.15 | 0.20 | 0.25 | 0.006 | 0.008 | 0.010 |
| D | 9.00 BSC | | | 0.354 BSC | | |
| D1 | 8.75 BSC | | | 0.344 BSC | | |
| E | 9.00 BSC | | | 0.354 BSC | | |
| E1 | 8.75 BSC | | | 0.344 BSC | | |
| e | 0.40 BSC | | | 0.016 BSC | | |
| θ | 0° | ---- | 14° | 0° | ---- | 14° |
| R | 0.075 | ---- | ---- | 0.003 | ---- | ---- |
| aaa | ---- | ---- | 0.15 | ---- | ---- | 0.006 |
| bbb | ---- | ---- | 0.10 | ---- | ---- | 0.004 |
| ccc | ---- | ---- | 0.10 | ---- | ---- | 0.004 |
| ddd | ---- | ---- | 0.05 | ---- | ---- | 0.002 |
| chamfer | ---- | ---- | 0.60 | ---- | ---- | 0.024 |

| Exposed Die Pad Size / Lead length Options | | | |
|--|--------|-----------------|-------------------|
| Option | Symbol | Dimension in mm | Dimension in inch |
| #3 | D2 | 4.90 ± 0.20 | 0.193 ± 0.008 |
| | E2 | 4.90 ± 0.20 | 0.193 ± 0.008 |
| | L | 0.40 ± 0.10 | 0.016 ± 0.004 |

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT: PROPSD JEDEC MO-220.

3.3 Signal Descriptions

This section contains the following information:

- [Signal Descriptions Overview](#)
- [Pin Type Definitions](#)
- [Signal Descriptions](#)

3.3.1 Signal Descriptions Overview

This section contains the pin types and signal descriptions for the 88SE9215 package.

3.3.2 Pin Type Definitions

Pin type definitions are shown in Table 3-1.

Table 3-1 Pin Type Definitions

| Pin Type | Definition |
|----------|-------------------------------|
| I/O | Input and Output |
| I | Input Only |
| O | Output Only |
| A | Analog |
| PU | Internal Pull-Up when Input |
| PD | Internal Pull-Down when Input |
| OD | Open-Drain Pad |
| Ground | Ground |
| Power | Power |

3.3.3 Signal Descriptions

This section outlines the 88SE9215 pin descriptions. All signals ending with the letter N indicate an active-low signal.

Table 3-2 PCIe Interface Signals

| Signal Name | Signal Number | Type | Description |
|-------------|---------------|-------|---|
| PERST_N | 61 | I, PU | PCI Platform Reset. Active low, indicates when the applied power is within the specified tolerance and stable. |
| WAKE_N | 60 | O, OD | PCI Wake-Up. An open-drain, active low signal that is driven low by a PCIe function to reactivate the PCIe Link hierarchy's main power rails and reference clocks. Note: For applications that support a wake-up function, connect this pin to the WAKE# signal of a PCIe card slot or system board. Connect an external pull-up resistor from the PCIe card slot or system board to the 3.3V auxiliary supply. For applications that do not support a wake-up function, keep the WAKE_N pin on the 88SE9215 open. |
| CLKP | 58 | I, A | Reference Clock. |
| CLKN | 59 | | Low voltage differential signals. The clock frequency has to be 100 MHz. |
| PRXP0 | 55 | I, A | PCIe differential signals to the controller's receiver. |
| PRXN0 | 54 | | |
| PTXP0 | 52 | O, A | PCIe differential signals from the controller's transmitter. |
| PTXN0 | 51 | | |

Table 3-3 Serial ATA Interface Signals

| Signal Name | Signal Number | Type | Description |
|-------------|---------------|------|--|
| TXN_0 | 33 | O, A | Serial ATA Transmitter Differential Outputs. |
| TXP_0 | 34 | | |
| TXN_1 | 27 | | |
| TXP_1 | 28 | | |
| TXN_2 | 12 | | |
| TXP_2 | 13 | | |
| TXN_3 | 6 | | |
| TXP_3 | 7 | | |
| RXN_0 | 31 | I, A | Serial ATA Receiver Differential Inputs. |
| RXP_0 | 30 | | |
| RXN_1 | 25 | | |
| RXP_1 | 24 | | |
| RXN_2 | 10 | | |
| RXP_2 | 9 | | |
| RXN_3 | 4 | | |
| RXP_3 | 3 | | |

Table 3-4 Reference Signals

| Signal Name | Signal Number | Type | Description |
|-------------|---------------|--------|--|
| ISET | 42 | I/O, A | Reference Current for Crystal Oscillator and PLL. This pin has to be connected to an external 6.04 kΩ 1% resistor to Ground. |
| XTLOUT | 41 | O, A | Crystal Output. |
| XTLIN_OSC | 40 | I, A | Reference Clock Input. This signal can be from an oscillator, or connected to a crystal with the XTLOUT pin. The clock frequency must be 25 MHz ± 80 ppm. |

Table 3-5 General Purpose I/O Signals

| Signal Name | Signal Number | Type | Description |
|-------------|---------------|---------|----------------------|
| GPIO0 | 63 | I/O, PU | General Purpose I/O. |
| GPIO1 | 69 | | |
| GPIO2 | 70 | | |
| GPIO3 | 18 | | |
| GPIO5 | 21 | | |
| GPIO4 | 20 | | |
| GPIO6 | 75 | | |
| GPIO7 | 76 | | |

Table 3-6 SPI Flash Interface Signals

| Signal Name | Signal Number | Type | Description |
|-------------|---------------|-------|--|
| SPI_CLK | 17 | O | SPI Interface Clock. |
| SPI_DI | 15 | I, PU | Serial Data In. Connect to the serial flash device's serial data output (DO). |
| SPI_CS | 14 | O | SPI Interface Chip Select. |
| SPI_DO | 2 | O | Serial Data Out. Connect to the serial flash device's serial data input (DI). |

Table 3-7 Test Mode Interface Signals

| Signal Name | Signal Number | Type | Description |
|-------------|---------------|--------|---|
| TP | 38 | I/O, A | Analog Test Point for PCIe PHY, SATA PHY, crystal oscillator, and PLL. |
| TST0 | 64 | I/O | Test Pin 0. |
| TST1 | 65 | I/O | Test Pin 1. |
| TST2 | 66 | I/O | Test Pin 2. This pin is reserved for chip test purposes only. Keep floating. |
| TST3 | 67 | I/O | Test Pin 3. This pin is reserved for chip test purposes only. Keep floating. |
| TST4 | 72 | I/O | Test Pin 4. This pin is reserved for chip test purposes only. Keep floating. |
| TST5 | 73 | I/O | Test Pin 5. This pin is reserved for chip test purposes only. Keep floating. |
| TST6 | 74 | I/O | Test Pin 6. This pin is reserved for chip test purposes only. Keep floating. |
| TESTMODE | 22 | I, PD | Test Mode. Enables chip test modes. |

Table 3-8 Power and Ground Pins

| Signal Name | Signal Number | Type | Description |
|-------------|---------------|-------|--|
| VAA2_0 | 32 | Power | Analog Power. |
| VAA2_1 | 26 | | 1.8V analog power supply for SATA PHY. |
| VAA2_2 | 11 | | |
| VAA2_3 | 5 | | |
| VAA1 | 39 | Power | Analog Power. 1.8V analog power for crystal oscillator, reference current generator, and PLL. |

Table 3-8 Power and Ground Pins (continued)

| Signal Name | Signal Number | Type | Description |
|-------------|------------------------------|-------|---|
| AVDD0 | 53 | Power | Analog Power. 1.8V analog power supply for PCIe PHY. |
| VDDIO | 16, 68 | Power | I/O Power. 3.3V analog power supply for digital I/Os. |
| VDD | 1, 19, 23, 36, 44, 62, 71 | Power | 1.0V Core Digital Power. |
| VSS | 8, 29, 45, 56 | Power | Ground. The main ground is the exposed die-pad (ePad) on the bottom side of the package. |

Table 3-9 No Connect Signals

| Signal Name | Signal Number | Type | Description |
|-------------|----------------|------|-------------|
| N/C | 35, 37, 43, 57 | N/A | No Connect. |



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4 LAYOUT GUIDELINES

The chapter contains the following information:

- [Layout Guidelines Overview](#)
- [Board Schematic Example](#)
- [Layer Stack-Up](#)
- [Power Supply](#)
- [PCB Trace Routing](#)
- [Recommended Layout](#)

Refer to Chapter 3, [Package](#), for package information.



4.1 Layout Guidelines Overview

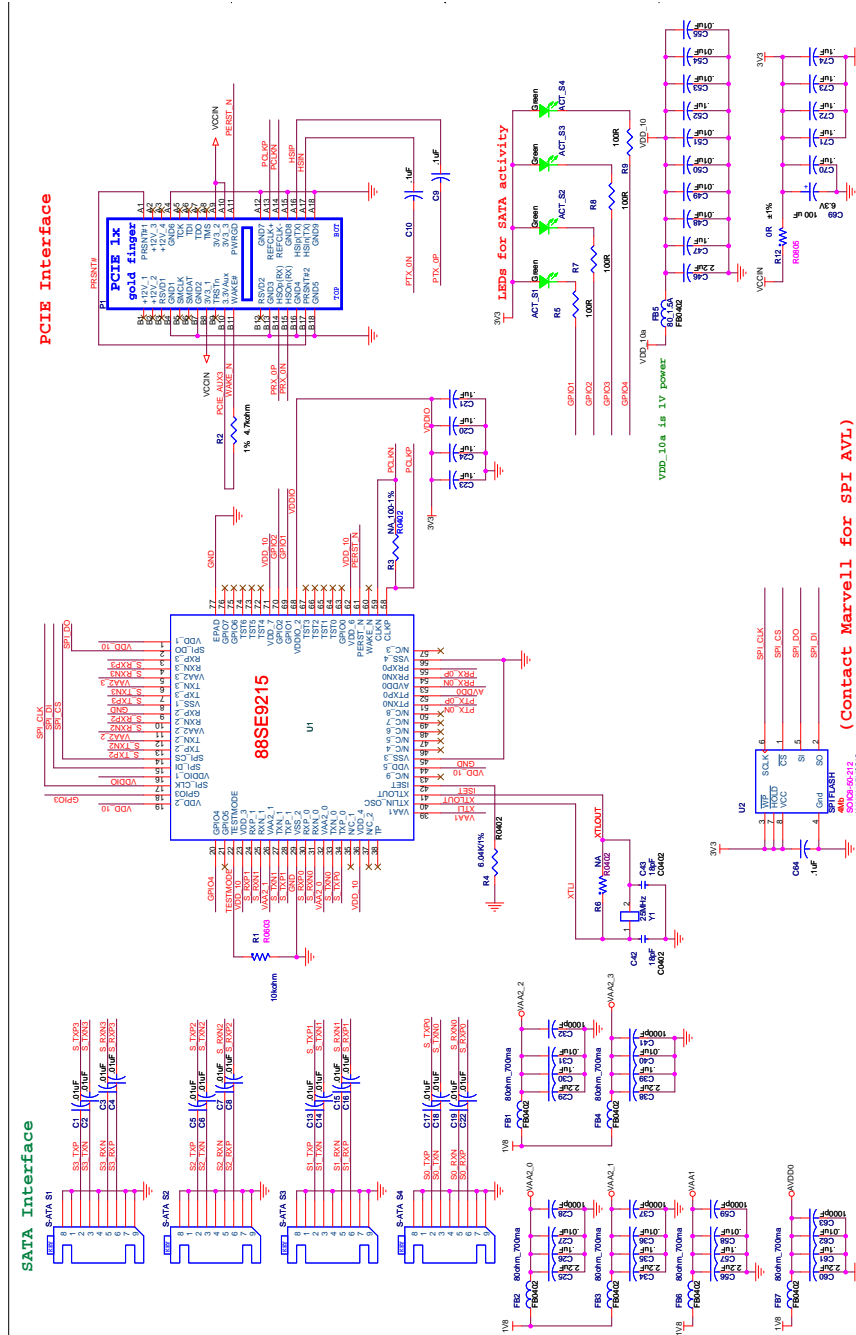
This chapter describes the system recommendations from the Marvell Semiconductor design and application engineers who work with the 88SE9215. This chapter is written for those who are designing schematics and printed circuit boards for an 88SE9215-based system. Whenever possible, the PCB designer should try to follow the suggestions provided in this chapter.

The information in this chapter is preliminary. Please consult with Marvell Semiconductor design and application engineers before starting your PCB design.

4.2 Board Schematic Example

The board schematic consists of the major interfaces of the 88SE9215 including SATA and PCIe. Figure 4-1 shows an example of board schematic.

Figure 4-1 SE9215 Example Board Schematic



Note: This diagram is for reference only. Contact your Marvell field applications engineer for the latest schematics.

4.3 Layer Stack-Up

This section contains the following information:

- [Layer Stack-Up Overview](#)
- [Layer 1–Topside, Parts, Slow and High Speed Signal Routes, and Power Routes](#)
- [Layer 2–Solid Ground Plane](#)
- [Layer 3–Power Plane](#)
- [Layer 4–Bottom Layer, Slow and High-Speed Signal Routes, and Power Routes](#)

4.3.1 Layer Stack-Up Overview

The following layer stack up is recommended:

- [Layer 1–Topside, Parts, Slow and High Speed Signal Routes, and Power Routes](#)
- [Layer 2–Solid Ground Plane](#)
- [Layer 3–Power Plane](#)
- [Layer 4–Bottom Layer, Slow and High-Speed Signal Routes, and Power Routes](#)

5 mil traces and 5 mil spacing are the recommended minimum requirements.

4.3.2 Layer 1–Topside, Parts, Slow and High Speed Signal Routes, and Power Routes

All active parts are to be placed on the topside. Some of the differential pairs for SATA and PCIe are routed on the top layer, differential 100 ohm impedance needs to be maintained for those high speed signals.

4.3.3 Layer 2–Solid Ground Plane

A solid ground plane should be located directly below the top layer of the PCB. This layer should be a minimum distance below the top layer in order to reduce the amount of crosstalk and EMI. There should be no cutouts in the ground plane. Use of 1 ounce copper is recommended.

4.3.4 Layer 3–Power Plane

Use solid planes on layer 3 to supply power to the ICs on the PCB. Avoid narrow traces and necks on this plane.

4.3.5 Layer 4–Bottom Layer, Slow and High-Speed Signal Routes, and Power Routes

Some of the differential pairs for SATA and PCIe are routed on the top layer, differential 100Ω impedance needs to be maintained for those high speed signals. The high speed signals have the return current on the third layer, which is the power plane. Make sure there is no cut-out under the signal path.

4.4 Power Supply

This section contains the following information:

- [Power Supply Overview](#)
- [VDD Power \(1.0V\)](#)
- [Analog Power Supply \(1.8V\)](#)
- [Bias Current Resistor \(RSET\)](#)

4.4.1 Power Supply Overview

The 88SE9215 operates using the following power supplies:

- [VDD Power \(1.0V\)](#) for the digital core
- [Analog Power Supply \(1.8V\)](#)

4.4.2 VDD Power (1.0V)

All digital power pins (VDD pins) must be connected directly to a VDD plane in the power layer with short and wide traces to minimize digital power-trace inductances.

Use vias close to the VDD pins to connect to this plane and avoid using the traces on the top layer. Marvell recommends placing capacitors around the three sides of the PCB near VDD pins with the following dimensions:

- 1 μF (1 capacitor)
- 0.1 μF (2 capacitors)
- 2.2 μF (1 ceramic capacitor)

The 2.2 μF ceramic decoupling capacitor is needed to filter the lower frequency power-supply noise.

To reduce system noise, the use of high-frequency surface-mount monolithic ceramic bypass capacitors should be placed as close as possible to the channel VDD pins. At least one decoupling capacitor should be placed on each side of the IC package.

Short and wide copper traces should be used to minimize parasitic inductances. Low-value capacitors (1,000–10,000 pF) are preferable over higher values because they are more effective at higher frequencies.

4.4.3 Analog Power Supply (1.8V)

The PCIe analog supply provides power for the PCIe link's high speed serial signals. To ensure high speed link operation, use a series of bypass capacitors for the supplies. A typical capacitor value combination is 1 μF , 0.1 μF , and 2.2 μF .



4.4.4 Bias Current Resistor (RSET)

Connect a 6.04K Ω (1%) resistor between the ISET pin and the adjacent top ground plane. This resistor should lie as close as possible to the ISET pin.

4.5 PCB Trace Routing

The stack-up parameters for the reference board are shown in Table 4-1.

Table 4-1 PCB Board Stack-up Parameters

| Layer | Layer Description | Copper Weight (oz) | Target Impedance ($\pm 10\%$) |
|-------|-------------------|--------------------|---------------------------------|
| 1 | Signal | 0.5 | 50 |
| 2 | GND | 1 | N/A |
| 3 | Power | 1 | N/A |
| 4 | Signal | 0.5 | 50 |

4.6 Recommended Layout

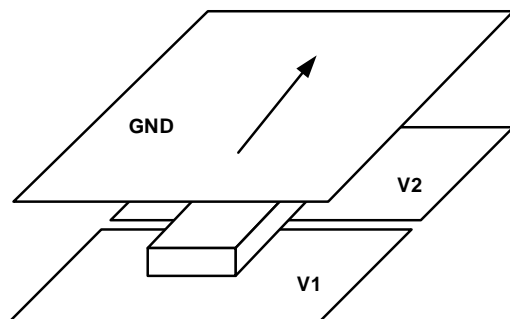
Solid ground planes are recommended. However, special care should be taken when routing VAA and VSS pins.

The following general tips describe what should be considered when determining your stack-up and board routing. These tips are not meant to substitute for consulting with a signal-integrity expert or doing your own simulations.

Note: Specific numbers or rules-of-thumb are not used here because they might not be applicable in every situation.

- Do not split ground planes.
Keep good spacing between possible sensitive analog circuitry on your board and the digital signals to sufficiently isolate noise. A solid ground plane is necessary to provide a good return path for routing layers. Try to provide at least one ground plane adjacent to all routing layers (see Figure 4-2).
- Keep trace layers as close as possible to the adjacent ground or power planes.
This helps minimize crosstalk and improve noise control on the planes.

Figure 4-2 Trace Has At Least One Solid Plane For Return Path



- When routing adjacent to only a power plane, do not cross splits.
Route traces only over the power plane that supplies both the driver and the load. Otherwise, provide a decoupling capacitor near the trace at the end that is not supplied by the adjacent power plane.
- Critical signals should avoid running parallel and close to or directly over a gap.
This would change the impedance of the trace.
- Separate analog powers onto opposing planes.
This helps minimize the coupling area that an analog plane has with an adjacent digital plane.
- For dual strip-line routing, traces should only cross at 90 degrees.
Avoid more than two routing layers in a row to minimize tandem crosstalk and to better control impedance.
- Planes should be evenly distributed in order to minimize warping.
- Calculating or modeling impedance should be made prior to routing.
This helps ensure that a reasonable trace thickness is used and that the desired board thickness is available. Consult with your board fabricator for accurate impedance.

- Allow good separation between fast signals to avoid crosstalk. Crosstalk increases as the parallel traces get longer.
- When packages become smaller, route traces over a split power plane
Smaller packages force vias to become smaller, thereby reducing board thickness and layer counts, which might create the need to route traces over a split power plane. Some alternatives to provide return path for these signals are listed below.

Caution must be used when applying these techniques. Digital traces should not cross over analog planes, and vice-versa. All of these rules must be followed closely to prevent noise contamination problems that might arise due to routing over the wrong plane.

By tightly controlling the return path, control noise on the power and ground planes can be controlled.

- Place a ground layer close enough to the split power plane in order to couple enough to provide buried capacitance, such as SIG-PWR-GND (see Figure 4-3). Return signals that encounter splits in this situation simply jumps to the ground plane, over the split, and back to the other power plane. Buried capacitance provides the benefit of adding low inductance decoupling to your board. Your fabricator may charge for a special license fee and special materials. To determine the amount of capacitance your planes provide, use the following equation:

$$C = 1.249 \cdot 10^{-13} \cdot E_r \cdot L \cdot W / H$$

Where E_r is the dielectric coefficient, $L \cdot W$ represents the area of copper, and H is the separation between planes.

- Provide return-path capacitors that connect to both power planes and jumps the split. Place them close to the traces so that there is one capacitor for every four or five traces. The capacitors would then provide the return path (see Figure 4-4).
- Allow only static or slow signals on layers where they are adjacent to split planes.

Figure 4-3 shows the ground layer close to the split power plane.

Figure 4-3 Close Power and Ground Planes Provide Coupling For Good Return Path

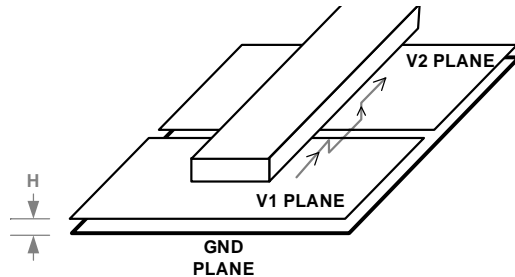
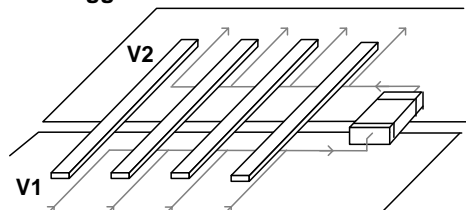


Figure 4-4 shows the thermal ground plane in relation to the return-path capacitor.

Figure 4-4 Suggested Thermal Ground Plane On Opposite Side of Chip





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5 ELECTRICAL SPECIFICATIONS

This chapter contains the following information:

- Absolute Maximum Ratings
- Recommended Operating Conditions
- Power Requirements
- DC Electrical Characteristics
- Thermal Data

5.1 Absolute Maximum Ratings

Table 5-1 defines the absolute maximum ratings for the 88SE9215.

Table 5-1 Absolute Maximum Ratings*

| Parameter | Symbol | Minimum | Maximum | Units |
|--|-----------------------|---------|---------|-------|
| Absolute Analog Power for PCIe PHY | AVDD0 _{abs} | -0.5 | 1.98 | V |
| Absolute Analog Power for Crystal Oscillator and PLL | VAA1 _{abs} | -0.5 | 1.98 | V |
| Absolute Analog Power for SATA PHY | VAA2_0 _{abs} | -0.5 | 1.98 | V |
| Absolute Analog Power for SATA PHY | VAA2_1 _{abs} | -0.5 | 1.98 | V |
| Absolute Digital Core Power | VDD _{abs} | -0.5 | 1.10 | V |
| Absolute Digital I/O Power | VDDIO _{abs} | -0.5 | 3.63 | V |

* Estimated values are provided until characterization is complete.

5.2 Recommended Operating Conditions

Table 5-2 defines the recommended operating conditions for the 88SE9215.

Table 5-2 Recommended Operating Conditions*

| Parameter | Symbol | Minimum | Type | Maximum | Units |
|---|----------------------|---------|------|---------|-------|
| Analog Power for PCIe PHY | AVDD0 _{op} | 1.71 | 1.8 | 1.89 | V |
| Analog Power for Crystal Oscillator and PLL | VAA1 _{op} | 1.71 | 1.8 | 1.89 | V |
| Analog Power for SATA PHY | VAA2_0 _{op} | 1.71 | 1.8 | 1.89 | V |
| Analog Power for SATA PHY | VAA2_1 _{op} | 1.71 | 1.8 | 1.89 | V |
| Digital Core Power | VDD _{op} | 0.95 | 1.0 | 1.05 | V |
| Digital I/O Power | VDDIO _{op} | 3.135 | 3.3 | 3.465 | V |
| Internal Bias Reference | ISET _{op} | 5.738 | 6.04 | 6.342 | KΩ |
| Ambient Operating Temperature, Commercial | N/A | 0 | N/A | 85 | °C |
| Ambient Operating Temperature, Industrial | N/A | -40 | N/A | 85 | °C |
| Junction Operating Temperature, Commercial | N/A | 0 | N/A | 125 | °C |
| Junction Operating Temperature, Industrial | N/A | -20 | N/A | 125 | °C |

* Estimated values are provided until characterization is complete.

5.3 Power Requirements

Table 5-3 defines the power requirements for the 88SE9215.

Table 5-3 Power Requirements*

| Parameter | Symbol | Maximum | Units |
|---|---------------------|---------|-------|
| Analog Power for PCIe PHY Transmitter | I _{AVDD0} | 55 | mA |
| Analog Power for Crystal Oscillator and PLL | I _{VAA1} | 10 | mA |
| Analog Power for SATA PHY | I _{VAA2_0} | 70 | mA |
| Analog Power for SATA PHY | I _{VAA2_1} | 70 | mA |
| Digital Core Power | I _{VDD} | 1500 | mA |
| Digital I/O Power (3.3V)† | I _{VDDIO} | 50 | mA |

* Estimated values are provided until characterization is complete.

† The digital I/O power supply can be either 3.3V or 1.8V.

5.4 DC Electrical Characteristics

Table 5-4 defines the DC electrical characteristics for the 88SE9215.

Table 5-4 DC Electrical Characteristics*

| Parameter | Symbol | Test Condition | Minimum | Maximum | Units |
|---------------------------|----------|---------------------------------|-----------------------|------------------------|---------|
| Input Low Level Voltage | V_{IL} | N/A | -0.4 | $0.25 \times V_{DDIO}$ | V |
| Input High Level Voltage | V_{IH} | N/A | $0.8 \times V_{DDIO}$ | 5.5 | V |
| Output Low Level Current | I_{OL} | $V_{PAD} = 0.4V$ | 5 | N/A | mA |
| Output High Level Current | I_{OH} | $V_{PAD} = V_{DDIO} - 0.4V$ | 5 | N/A | mA |
| Pull Up Strength | I_{PU} | $V_{PAD} = 0.5 \times V_{DDIO}$ | 10 | N/A | μA |
| Pull Down Strength | I_{PD} | $V_{PAD} = 0.5 \times V_{DDIO}$ | 10 | N/A | μA |
| Input Leakage Current | I_{LK} | $0 < V_{PAD} < V_{DDIO}$ | N/A | 10 | μA |
| Input Capacitance | C_{IN} | $0 < V_{PAD} < 5.5V$ | N/A | 5 | pF |

* Estimated values are provided until characterization is complete.

5.5 Thermal Data

It is recommended to read application note *AN-63 Thermal Management for Selected Marvell® Products* (Document Number MV-S300281-00) and the *ThetaJC, ThetaJA, and Temperature Calculations White Paper*, available from Marvell, before designing a system. These documents describe the basic understanding of thermal management of integrated circuits (ICs) and guidelines to ensure optimal operating conditions for Marvell products.

Note: In addition to the airflow requirement, a heat sink is required to assist the thermal dissipation.

Table 5-5 provides the thermal data for the 88SE9215. The simulation was performed according to JEDEC standards.

Table 5-5 shows the values for the package thermal parameters for the 76-lead Quad Flat Non-Lead package (QFN 76) mounted on a 4-layer PCB.

Table 5-5 Package Thermal Data

| Parameter | Definition | Airflow Value | | | |
|---------------|---|---------------|-----------|-----------|-----------|
| | | 0 m/s | 1 m/s | 2 m/s | 3 m/s |
| θ_{JA} | Thermal resistance: junction to ambient | 29.9 C/W | 26.6 C/W | 25.5 C/W | 24.8 C/W |
| Ψ_{JB} | Thermal characterization parameter: junction to bottom surface center of the package. | 15.60 C/W | 15.59 C/W | 15.58 C/W | 15.57 C/W |
| Ψ_{JT} | Thermal characterization parameter: junction to top center | 0.63 C/W | 0.93 C/W | 1.17 C/W | 1.34 C/W |



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