88SE9480/88SE9485 R3.3

Eight-Lane PCI-Express 2.0 to Eight-Port SAS/SATA 6 Gbps RAID I/O Controller

Preliminary Datasheet

Doc No. MV-S105606-00 Rev. J

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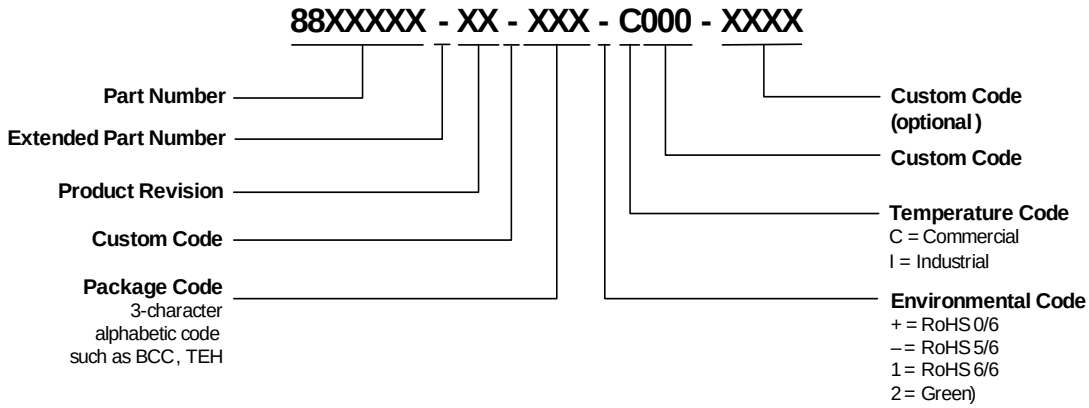
ORDERING INFORMATION

Ordering Part Numbers and Package Markings

The following figure shows the ordering part numbering scheme for the 88SE9480/88SE9485 part. For complete ordering information, contact your Marvell FAE or sales representative.

Sample Ordering Part Number



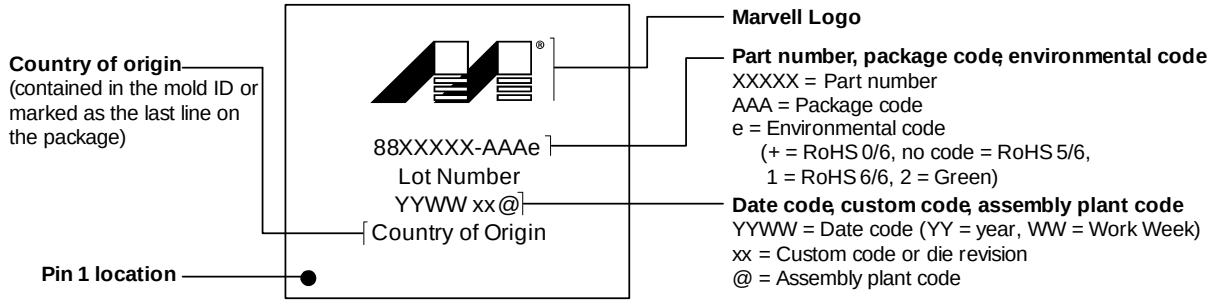
The standard ordering part numbers for the respective solutions are indicated in the following table.

Ordering Part Numbers

Part Number	Description
88SE9480C3-BJA2C000	484-Ball HSBGA 23 × 23 mm
88SE9485C3-BJA2C000	484-Ball HSBGA 23 × 23 mm This product does not support Marvell RAID stack.

The next figure shows a typical Marvell package marking.

88SE9480/88SE9485 Package Marking and Pin 1 Location



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CHANGE HISTORY

The following table identifies the document change history for Rev. J.

Document Changes *

Location	Type	Description	Date
Page 1-1	Update	Updated the description for chapter 1, Overview: from The 88SE9480/88SE9485 is an eight-port, 6.0 Gbps SAS/SATA controller that provides a one- four-, or eight-lane PCIe 2.0 host interface, and supports advanced RAID topologies. The 88SE9xx5 is similar to the 88SE9xx0, but does not support the Marvell RAID stack. to The 88SE9480/88SE9485 is an eight-port, 6.0 Gbps SAS/SATA controller that provides a one-, two-, four-, or eight-lane PCIe 2.0 host interface, and supports advanced RAID topologies. The 88SE9xx5 is similar to the 88SE9xx0, but does not support the Marvell RAID stack.	December 8, 2014
Page 2-2	Update	Updated the description for section 2.1, General.	December 5, 2014
Page 3-5	Update	Updated Table 3-1, Signal Type Definitions.	December 8, 2014
Page 3-8	Update	Updated the description for PIN_TEST[9:8] in Table 3-2, General Purpose I/O Signals: from PIN_TEST[9:8]–PCIe maximum lane width **0h:** x8 **1h:** x1 **2h:** x4 **3h:** x8 to PIN_TEST[9:8]–PCIe maximum lane width **0h:** x8 ***Note:*** *Always use 0h.*	January 14, 2015

Document Changes * (continued)

Location	Type	Description	Date
Page 4-3 Page 4-4 Page 4-5 page 4-6	Update	Updated the following schematics for section 4.1, 88SE9480/88SE9485 Board Schematics: • Figure 4-1, 88SE9480/88SE9485 PCIe and SAS • Figure 4-2, 88SE9480/88SE9485 Bootstrap, NI, SPI, UART, I2C, LED • Figure 4-3, 88SE9480/88E9485 Power and Ground • Figure 4-4, 88SE9480/88SE9485 Power Regulators	June 27, 2014
Page 5-4	Parameter	Updated Table 5-3, DC Electrical Characteristics: • Corrected the Maximum value of Input Low Voltage of Digital I/O from 0.8 to 0.3 × VDDOx. • Corrected the Minimum value of Input High Voltage of Digital I/O from 2.0 to 0.7 × VDDOx. • Corrected the Maximum value of Input High Voltage of Digital I/O from 3.6 to VDDOx + 0.4. • Corrected the Typical value of Output High Voltage of Digital I/O from VDDO1/VDDO2 to VDDOx.	December 18, 2014

* The type of change is categorized as: Parameter, Revision, or Update. A Parameter change is a change to a spec value, a Revision change is one that originates from the chip Revision Notice, and an Update change includes all other document updates.

CONTENTS

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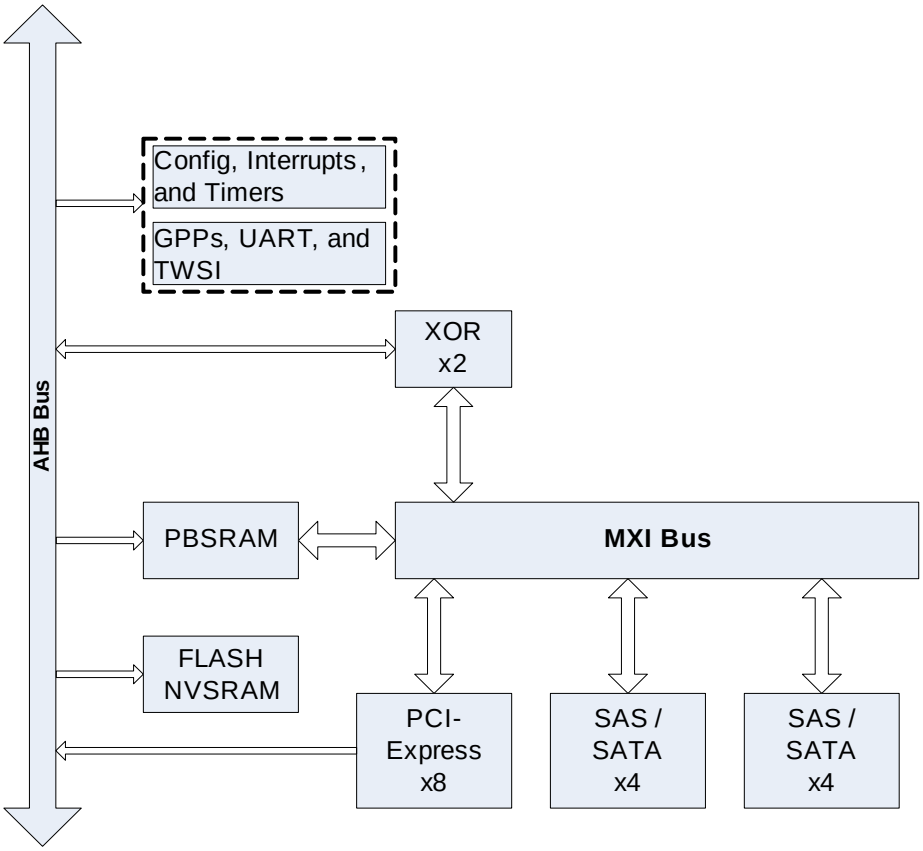
1 OVERVIEW

The 88SE9480/88SE9485 is an eight-port, 6.0 Gbps SAS/SATA controller that provides a one-, two-, four-, or eight-lane PCIe 2.0 host interface, and supports advanced RAID topologies. The 88SE9xx5 is similar to the 88SE9xx0, but does not support the Marvell RAID stack.

The 88SE9480/88SE9485 controller brings a high-performance, low-cost 6.0 Gbps per port combined SAS and SATA solution to HBA, workstation, and server designs utilizing a one-, four-, or eight-lane PCIe 2.0 interface. The 88SE9480/88SE9485 integrates eight high-performance SAS/SATA PHYs and a self-configuring eight-lane PCIe core. Each of the eight PHYs is capable of 1.5 Gbps, 3.0 Gbps, and 6.0 Gbps SAS and SATA link rates. The 88SE9480/88SE9485 supports ANSI Serial Attached SCSI - 2.0 (SAS-2.0). The controller also supports the SATA protocol defined in the Serial ATA, Revision 3.0 Specification.

Figure 1-1 shows the system block diagram.

Figure 1-1 88SE9480/88SE9485 (8-port) Block



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2 FEATURES

The chapter contains the following sections:

2.1 General

- Eight 6 Gbps SAS/SATA ports.
- Choice of x1, x2, x4, or x8 lane PCIe 2.0 host interface.
- Supports three Serial Device Bus (I2C) controllers for communicating with hardware monitoring ICs.
- Supports two industry standard 57600 UARTs.
- Supports two SFF-8485 compliant SGPIO ports.
- Supports autodetection of SAS or native SATA device.
- Up to 4096 concurrent I/O operations (2048 per 4 ports).
- Up to 128 concurrent SATA Devices (64 per 4 ports).
- No hardware limit on the number of SAS devices supported.
- 55 nm CMOS process, 1.0V digital core, 2.5V analog power supply, and 3.3V I/O supply.
- Estimated power (8-port): 6W.[1]
- Up to 34 LED/GPIO ports.
- Supports hardware RAID 5 and RAID 6 acceleration.
- Supports Data Path Parity Protection (DPP).

1.

2.2 PCIe

- Supports x1, x2, x4, or x8 lane PCIe 2.0 Interface (5.0 Gbps).
- Supports four fully independent PCIe functions.
- Supports independent interrupt mechanisms for each PCIe function.
- Supports Message Signal Interrupts (MSI).
- All registers memory mapped.
- Supports PCIe Power Management: D0, D1, $D3_{COLD}$, $D3_{HOT}$.

2.3 SAS (Direct Attach or Expander)

- Serial Attached SCSI (SAS-2.0) compliant.
- Supports 6 Gbps, 3 Gbps, and 1.5 Gbps devices.
- Supports SAS Multiplexing. Up to 16 logical ports when multiplexing is enabled on all PHYs.
- Supports SSC, with independent control for each PHY using SSC_EN (R060h [17]).
- Supports wide SAS ports. Up to four wide when multiplexing is disabled, and up to eight wide when multiplexing is enabled.
- Supports Serial SCSI Protocol (SSP), initiator and target mode.
- Supports SAS Management Protocol (SMP), initiator mode.
- Supports Serial ATA Tunneling Protocol (STP), initiator mode.
  - Non-zero offset and non-sequential data delivery.
  - ATA and ATAPI commands.
  - Native Command Queuing (NCQ).
- Supports T10 Protection Information Model. DIF fields can be inserted, checked, replaced, and/or removed.
- Supports Transport Layer Retries.
- Supports hardware assisted Scatter-Gather.

2.4 SATA (Direct Attach)

- Serial ATA Revision 3.0 (6 Gbps) compliant, with speed negotiation to 3.0 Gbps and 1.5 Gbps.
- Supports programmable SATA signaling levels, including Gen1x, Gen2i, and Gen2x.
- Supports ATA and ATAPI commands.
- Supports Native Command Queuing (NCQ).
  - Non-zero offset and non-sequential data delivery.
  - 32 outstanding commands per device.
- Supports Port Multiplier.
  - FIS based Switching on NCQ and legacy commands.
- Supports Host mode and Device mode of operation.
- Supports hardware assisted Scatter-Gather.

2.5 XOR Engine

- Supports Advanced RAID features including:
  - Dual XOR RAID 6.
  - P + Q + Copy, or Q + Q + Q RAID 6.
  - Memory Block Fill.
  - Zero Result Check.
- Generates up to 3 checksums concurrently, including any combination of P and Q.
- Independent GF Multiply coefficient for each of 3 concurrent Q checksum calculations.
- Supports rebuilding three failed drives simultaneously with a single read of remaining good drives.
- Supports chained XOR Descriptor Tables, with up to 32 operations in each table.
- Supports Scatter-Gather transfers using a common PRD format.
- Supports CRC32 checksum generation and checking.

2.6 Peripherals

- Supports up to 4 MB of external NVSRAM memory (x8/x16).
- Supports up to 4 MB of external PBSRAM memory (x32).
- Supports up to 8 MB of external Parallel Flash memory (x8/x16).
- Supports up to 16 MB of external SPI Flash memory.

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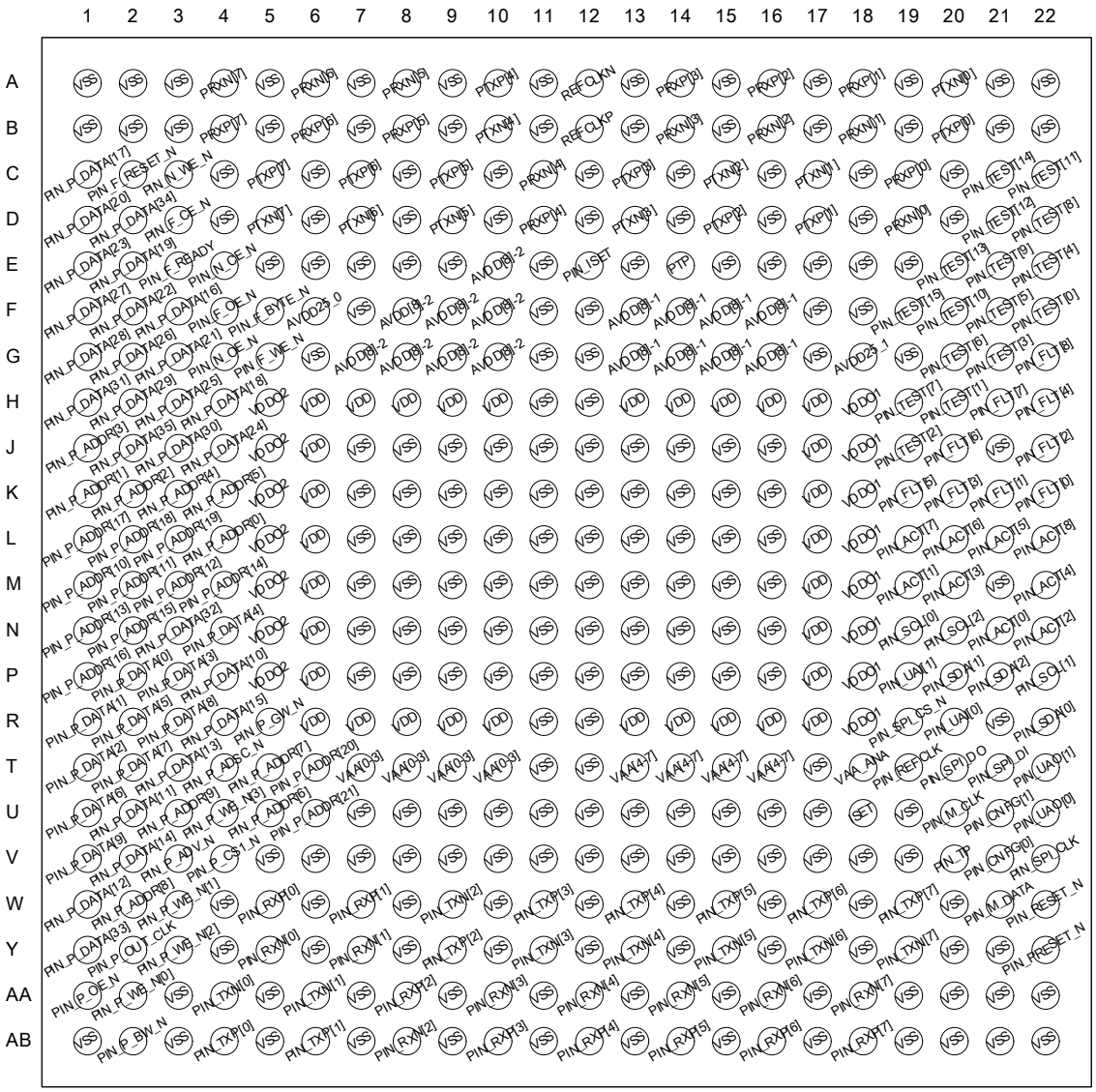
3 PACKAGE

This chapter contains the following sections:

3.1 Ball Diagram

The 484-pin HSBGA ball diagram is illustrated in Figure 3-1.

Figure 3-1 Ball Diagram



3.2 Mechanical Dimensions

The package mechanical drawing is shown in Figure 3-2 and the mechanical dimensions are shown in Figure 3-3.

Figure 3-2 Package Mechanical Drawing (BJA)

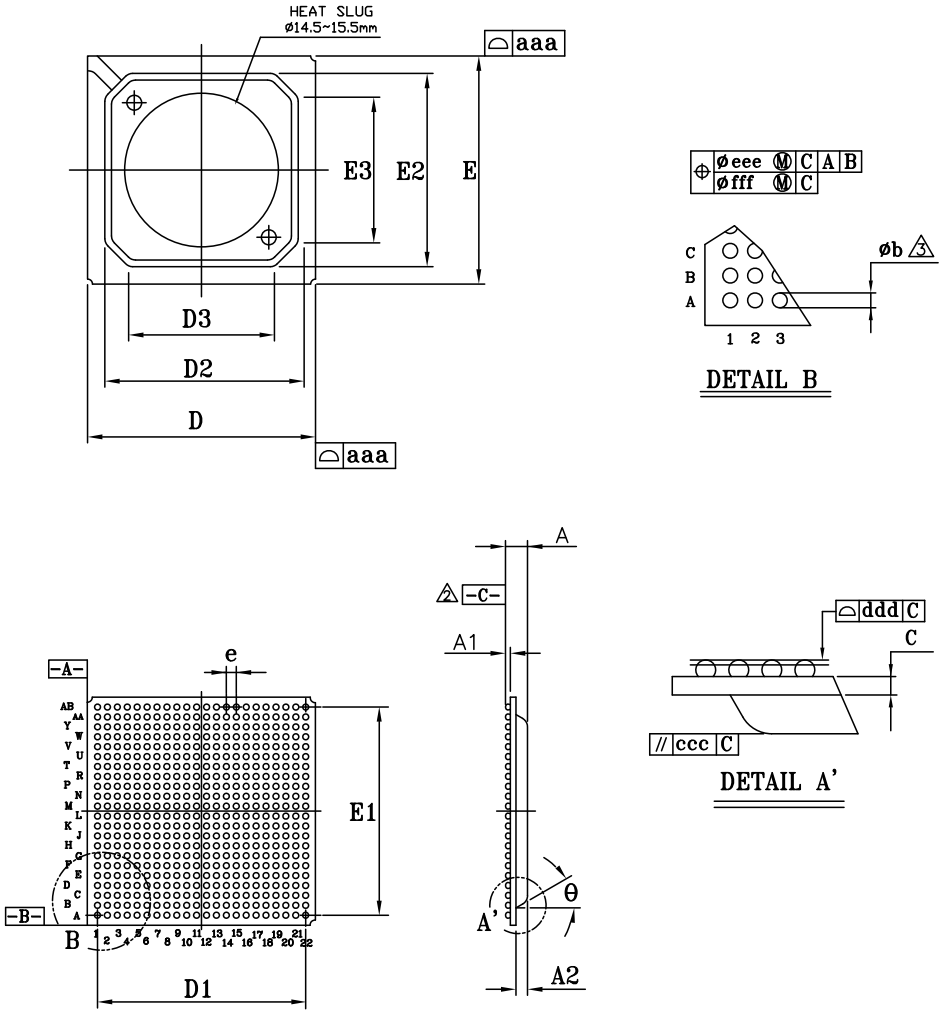


Figure 3-3 Package Mechanical Dimensions (BJA)

Symbol	dimension in mm			dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	2.23	2.43	---	0.088	0.096
A1	0.40	0.50	0.60	0.016	0.020	0.024
A2	1.12	1.17	1.22	0.044	0.046	0.048
b	0.50	0.60	0.70	0.020	0.024	0.028
c	0.51	0.56	0.61	0.020	0.022	0.024
D	22.80	23.00	23.20	0.898	0.906	0.913
D1	---	21.00	---	---	0.827	---
D2	19.30	19.50	19.70	0.760	0.768	0.776
D3	---	14.70	---	---	0.579	---
E	22.80	23.00	23.20	0.898	0.906	0.913
E1	---	21.00	---	---	0.827	---
E2	19.30	19.50	19.70	0.760	0.768	0.776
E3	---	14.70	---	---	0.579	---
e	---	1.00	---	---	0.039	---
aaa	0.20			0.008		
ccc	0.25			0.010		
ddd	0.15			0.006		
eee	0.25			0.010		
fff	0.10			0.004		
θ	30° TYP			30° TYP		

NOTE:

1. CONTROLLING DIMENSION: MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25 mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
5. REFERENCE DOCUMENT : JEDEC MS-034
6. SPECIAL CHARACTERISTICS C CLASS: ccc , ddd

3.3 Signal Descriptions

This section includes information on signal definitions and descriptions:

- Signal Definitions
- Signal Descriptions

3.3.1 Signal Definitions

Signal type definitions are shown in Table 3-1.

Table 3-1 Signal Type Definitions

Signal Type	Definition
I/O	Input and output
I	Input only
O	Output only
OC	Open Collector
OD	Open-Drain pad
Ground	Ground
Power	Power
NC	No Connect*
DNC	Do Not Connect†
N/A	Not Applicable

* Pin is floating and is not connected internally to any active circuitry nor has any electrical continuity to any other pin

† Device pin to which there may or may not be an internal connection, but to which no external connections are allowed.

3.3.2 Signal Descriptions

This section outlines the 88SE9480/88SE9485 signal descriptions. Signals ending with the letter “N” are active-low signals.

Table 3-2 General Purpose I/O Signals

Signal Name	Signal Number	Type	Description
PIN_ACT[8]	L22	I/O, OC	Activity LED.
PIN_ACT[7]	L19		Active low.
PIN_ACT[6]	L20		PIN_ACT is active when SAS/SATA PHY is transmitting or receiving.
PIN_ACT[5]	L21		
PIN_ACT[4]	M22		These pins can be used as GPIO.
PIN_ACT[3]	M20		PIN_ACT[7:0]–SAS/SATA PHY[7:0] activity.
PIN_ACT[2]	N22		
PIN_ACT[1]	M19		PIN_ACT[8]–Global Activity. Enabled when any SAS/SATA PHY is active.
PIN_ACT[0]	N21		

Table 3-2 General Purpose I/O Signals (continued)

Signal Name	Signal Number	Type	Description
PIN_FLT[8] PIN_FLT[7] PIN_FLT[6] PIN_FLT[5] PIN_FLT[4] PIN_FLT[3] PIN_FLT[2] PIN_FLT[1] PIN_FLT[0]	G22 H21 J20 K19 H22 K20 J22 K21 K22	I/O, OC	Fault LED. Active low signals. PIN_FLT is active when PHY is not ready or when PHY is ready and there is any PHY related error or connection error. These pins can be used as GPIO, SGPIO, I2C, or FLT_LED. See GPIO_FLT_CFG (R10080h [7:0]) and I2C_SGPIO_FLT_PAD_SEL (R10104h [9:8]). Pins used as Fault LED: • PIN_FLT[8]: Global Fault indication. The indicator is on when any SAS/SATA_PHY has a fault. • PIN_FLT[7:0] corresponds to SAS/SATA_PHY7 through PHY0. ***Note:*** *When PHY is not ready, PIN_FLT[7:0] is always on. After the PHY is ready, a fault occurs.* Pins used as SGPIO: • PIN_FLT[8]: Same as FLT mode. • PIN_FLT[7:4]: SGPIO1 SCLK, SLOAD, SDOUT, SDIN • PIN_FLT[3:0]: SGPIO0 SCLK,SLOAD,SDOUT,SDIN Used as I2C: • PIN_FLT[8]: Same as FLT Mode • PIN_FLT[7:6]: I2C2 CLK, DATA • PIN_FLT[5:4]: Not used • PIN_FLT[3:2]: I2C1 CLK, DATA • PIN_FLT[1:0]: Not used

Table 3-2 General Purpose I/O Signals (continued)

Signal Name	Signal Number	Type	Description
PIN_TEST[15]	F19	I/O	Configuration and test pins.
PIN_TEST[14]	C21		These pins can be used as GPIO.
PIN_TEST[13]	E20		PIN_TEST[15]-PCIe power-up disable
PIN_TEST[12]	D21		**0h**: Enable PCIe after power-up
PIN_TEST[11]	C22		**1h:** Disable PCIe after power-up
PIN_TEST[10]	F20		Not applicable to this chip. This signal needs pull-down.
PIN_TEST[9]	E21		PIN_TEST[14:13]–Chip reference clock selection
PIN_TEST[8]	D22		**0h:** 20 MHz
PIN_TEST[7]	H19		**1h:** 50 MHz
PIN_TEST[6]	G20		**2h:** 100 MHz
PIN_TEST[5]	F21		**3h:** 75 MHz
PIN_TEST[4]	E22		PIN_TEST[12:11]–Reserved
PIN_TEST[3]	G21		PIN_TEST[10]–PCIe ROM location
PIN_TEST[2]	J19		**0h:** Parallel Flash
PIN_TEST[1]	H20		**1h:** Serial Flash
PIN_TEST[0]	F22		PIN_TEST[9:8]–PCIe maximum lane width
			0h: x8
			*Always use 0h.*PIN_TEST[7:6]–Reserved
			PIN_TEST[5]—PCIe configuration access enable.
			0h: PCIe responds to configuration access.
			1h: PCIe returns a retry configuration access.
			Not applicable to this chip. This signal needs pull-down.
			PIN_TEST[4]–Parallel Flash x8/x16
			0h: Byte mode
			1h: Word mode
			PIN_TEST[3:2]–Reserved
			PIN_TEST[1]–UART baudrate
			0h: 57600
			1h: Reserved
			PIN_TEST[0]–UART mode
			0h: Reserved
			1h: Terminal mode

Table 3-3 Clock and Reset Signals

Signal Name	Signal Number	Type	Description
PIN_REFCLK	T19	I	Reference clock input. 2.5V, ± 350 ppm.
PIN_RESET_N	W22	I	Power-on reset.

Table 3-3 Clock and Reset Signals (continued)

Signal Name	Signal Number	Type	Description
PIN_PRESET_N	Y22	I	PCIe Reset
PIN_TP	V20	O	SAS/SATA analog test port.

Table 3-4 I2C Signals

Signal Name	Signal Number	Type	Description
PIN_SCL[2]	N20	I/O, OC	I2C clock.
PIN_SCL[1]	P22		
PIN_SCL[0]	N19		
PIN_SDA[2]	P21	I/O, OC	I2C data.
PIN_SDA[1]	P20		
PIN_SDA[0]	R22		

Table 3-5 UART Signals

Signal Name	Signal Number	Type	Description
PIN_UAI[1]	P19	I	UART input.
PIN_UAI[0]	R20		
PIN_UAO[1]	T22	O	UART output.
PIN_UAO[0]	U22		

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Table 3-6 Parallel Flash Signals

Signal Name	Signal Number	Type	Description
PIN_F_BYTE_N	F5	O	Parallel flash Byte mode.
PIN_F_CE_N	D3	O	Parallel flash chip select.
PIN_F_OE_N	F4	O	Parallel flash output enable.
PIN_F_READY	E3	I	Parallel flash ready signal. Requires external pull-up resistor.
PIN_F_RESET_N	C2	O	Parallel flash reset.
PIN_F_WE_N	G5	O	Parallel flash write enable.

Table 3-6 Parallel Flash Signals (continued)

Signal Name	Signal Number	Type	Description
PIN_P_ADDR[21]	U6	O	Shared address bus for parallel flash, NVSRAM and PBSRAM. For Parallel Flash, signals are word addresses. For NVSRAM, signals are WORD addresses. For PBSRAM, signals are Dword addresses.
PIN_P_ADDR[20]	T6		
PIN_P_ADDR[19]	L3		
PIN_P_ADDR[18]	L2		
PIN_P_ADDR[17]	L1		
PIN_P_ADDR[16]	P1		
PIN_P_ADDR[15]	N2		
PIN_P_ADDR[14]	M4		
PIN_P_ADDR[13]	N1		
PIN_P_ADDR[12]	M3		
PIN_P_ADDR[11]	M2		
PIN_P_ADDR[10]	M1		
PIN_P_ADDR[9]	U3		
PIN_P_ADDR[8]	W2		
PIN_P_ADDR[7]	T5		
PIN_P_ADDR[6]	U5		
PIN_P_ADDR[5]	K4		
PIN_P_ADDR[4]	K3		
PIN_P_ADDR[3]	J1		
PIN_P_ADDR[2]	K2		
PIN_P_ADDR[1]]	K1		
PIN_P_ADDR[0]	L4		

Table 3-6 Parallel Flash Signals (continued)

Signal Name	Signal Number	Type	Description
PIN_P_DATA[35]	J2	I/O	Shared Data Bus for Parallel Flash/NVSRAM/PBSRAM.
PIN_P_DATA[34]	D2		For Parallel Flash, DATA[15:0] are used.
PIN_P_DATA[33]	Y1		In Byte mode, DATA[15] is address bit 0. DATA[7:0] are data.
PIN_P_DATA[32]	N3		
PIN_P_DATA[31]	H1		In Word mode, DATA[15:0] are data.
PIN_P_DATA[30]	J3		For NVSRAM, DATA[15:0] are used.
PIN_P_DATA[29]	H2		For PBSRAM, DATA[35:0] are used.
PIN_P_DATA[28]	G1		DATA[35] is parity for Byte 3.
PIN_P_DATA[27]	F1		DATA[34] is parity for Byte 2.
PIN_P_DATA[26]	G2		DATA[33] is parity for Byte 1.
PIN_P_DATA[25]	H3		DATA[32] is parity for Byte 0.
PIN_P_DATA[24]	J4		
PIN_P_DATA[23]	E1		
PIN_P_DATA[22]	F2		
PIN_P_DATA[21]	G3		
PIN_P_DATA[20]	D1		
PIN_P_DATA[19]	E2		
PIN_P_DATA[18]	H4		
PIN_P_DATA[17]	C1		
PIN_P_DATA[16]	F3		
PIN_P_DATA[15]	R4		
PIN_P_DATA[14]	V2		
PIN_P_DATA[13]	T3		
PIN_P_DATA[12]	W1		
PIN_P_DATA[11]	U2		
PIN_P_DATA[10]	P4		
PIN_P_DATA[9]	V1		
PIN_P_DATA[8]	R3		
PIN_P_DATA[7]	T2		
PIN_P_DATA[6]	U1		
PIN_P_DATA[5]	R2		
PIN_P_DATA[4]	N4		
PIN_P_DATA[3]	P3		
PIN_P_DATA[2]	T1		
PIN_P_DATA[1]]	R1		
PIN_P_DATA[0]	P2		

Table 3-7 NVSRAM Signals

Signal Name	Signal Number	Type	Description
PIN_N_CE_N	E4	O	nvSRAM chip select.
PIN_N_OE_N	G4	O	nvSRAM output enable.
PIN_N_WE_N	C3	O	nvSRAM write enable.

Table 3-8 PBSRAM Signals

Signal Name	Signal Number	Type	Description
PIN_P_ADSC_N	T4	O	PBSRAM ASDC mode.
PIN_P_ADV_N	V3	O	PBSRAM address advance.
PIN_P_BW_N	AB2	O	PBSRAM BW.
PIN_P_CS1_N	V4	O	PBSRAM chip select.
PIN_P_GW_N	R5	O	PBSRAM global write enable.
PIN_P_OE_N	AA1	O	PBSRAM output enable.
PIN_P_OUT_CLK	Y2	O	PBSRAM clock.
PIN_P_WE_N[3]	U4	O	PBSRAM write enable.
PIN_P_WE_N[2]	Y3		
PIN_P_WE_N[1]	W3		
PIN_P_WE_N[0]	AA2		

Table 3-9 System Interface Signals

Signal Name	Signal Number	Type	Description
PIN_CNFG[1] PIN_CNFG[0]	U21 V21	I	Configuration. **00:** Normal Functional mode. **Others:**Test Mode.
REFCLKP	B12	I	PCIe reference clock input. 100MHz ± 300ppm.No internal clock termination.
REFCLKN	A12	I	PCIe reference clock input. 100MHz ± 300ppm.No internal clock termination.

Table 3-10 SPI Interface Signals

Signal Name	Signal Number	Type	Description
PIN_SPI_DI	T21	I	SPI data input.
PIN_SPI_CLK	V22	O	SPI clock.
PIN_SPI_CS_N	R19	O	SPI chip select.
PIN_SPI_DO	T20	O	SPI data output.

Table 3-11 PCIe Interface Signals

Signal Name	Signal Number	Type	Description
ISET	U18	I/O	Reference Current for PCI-Express PHY. This pin must be connected to an external 6.04 kΩ, 1% resistor to ground.
PIN_ISET	E12	I	Chip reference resistor 5 kΩ.
PTP	E14	O	Analog test port for PCIe.
PIN_M_CLK	U20	I	PCIe debugging MDIO interface, clock.
PIN_M_DATA	W21	I/O	PCIe debugging MDIO interface, data.

Table 3-12 SAS/SATA Transmitter and Receiver Interface Signals

Signal Name	Signal Number		Type	Description
PIN_RXP[7]	AB18	–	I	PIN_RXP[7:0]–SAS/SATA PHY 7–0 Receiver Differential Signal.
PIN_RXP[6]	AB16	–		
PIN_RXP[5]	AB14	–		
PIN_RXP[4]	AB12	–		
PIN_RXP[3]	AB10			
PIN_RXP[2]	AA8			
PIN_RXP[1]	W7			
PIN_RXP[0]	W5			
PIN_RXN[7]	AA18	–	I	PIN_RXN[7:0]–SAS/SATA PHY 7–0 Receiver Differential Signals.
PIN_RXN[6]	AA16	–		
PIN_RXN[5]	AA14	–		
PIN_RXN[4]	AA12	–		
PIN_RXN[3]	AA10			
PIN_RXN[2]	AB8			
PIN_RXN[1]	Y7			
PIN_RXN[0]	Y5			

Table 3-12 SAS/SATA Transmitter and Receiver Interface Signals (continued)

Signal Name	Signal Number		Type	Description
PIN_TXP[7]	W19	–	O	PIN_TXP[7:0]–SAS/SATA PHY 7–0 Transmitter Differential Signals.
PIN_TXP[6]	W17	–		
PIN_TXP[5]	W15	–		
PIN_TXP[4]	W13	–		
PIN_TXP[3]	W11			
PIN_TXP[2]	Y9			
PIN_TXP[1]	AB6			
PIN_TXP[0]	AB4			
PIN_TXN[7]	Y19		O	PIN_TXN[7:0]–SAS/SATA PHY 7–0 Transmitter Differential Signals.
PIN_TXN[6]	Y17			
PIN_TXN[5]	Y15			
PIN_TXN[4]	Y13			
PIN_TXN[3]	Y11			
PIN_TXN[2]	W9			
PIN_TXN[1]	AA6			
PIN_TXN[0]	AA4			

Table 3-13 PCIe Transmitter and Receiver Interface Signals

Signal Name	Signal Number		Type	Description
PRXP[7]	B4	–	I	PRXP[7:0]–PCI-Express Lane 7–0 Receiver Differential Signal (PCIe Rx +/-).
PRXP[6]	B6	–		
PRXP[5]	B8	–		
PRXP[4]	D11	–		
PRXP[3]	A14			
PRXP[2]	A16			
PRXP[1]	A18			
PRXP[0]	C19			
PRXN[7]	A4	–	I	PRXN[7:0]–PCI-Express Lane 7–0 Receiver Differential Signals (PCIe Rx +/-).
PRXN[6]	A6	–		
PRXN[5]	A8	–		
PRXN[4]	C11	–		
PRXN[3]	B14			
PRXN[2]	B16			
PRXN[1]	B18			
PRXN[0]	D19			

Table 3-13 PCIe Transmitter and Receiver Interface Signals (continued)

Signal Name	Signal Number		Type	Description
PTXP[7]	C5	–	O	PTXP[7:0]–PCI-Express Lane 7–0 Transmitter Differential Signals (PCIe Tx -/+).
PTXP[6]	C7	–		
PTXP[5]	C9	–		
PTXP[4]	A10	–		
PTXP[3]	C13			
PTXP[2]	D15			
PTXP[1]	D17			
PTXP[0]	B20			
PTXN[7]	D5	–	O	PTXN[7:0]–PCI-Express Lane 7–0 Transmitter Differential Signals (PCIe Tx -/+).
PTXN[6]	D7	–		
PTXN[5]	D9	–		
PTXN[4]	B10	–		
PTXN[3]	D13			
PTXN[2]	C15			
PTXN[1]	C17			
PTXN[0]	A20			

Table 3-14 Power Interface Signals

Signal Name	Signal Number	Type	Description
AVDD25_0	F6	Power, I	I/O Pad Power 2.5V.
AVDD25_1	G18	Power, I	I/O Pad Power 2.5V.
AVDD[8]-1	F13, F14, F15, F16, G13, G14, G15, G16	Power, I	1.8V analog power for PCI-Express PHY. AVDD[8] is for PLL and the current source.
AVDD[8]-2	F8, F9. E10, F10, G7, G8, G9, G10	Power, I	1.8V analog power for PCI-Express PHY. AVDD[8] is for PLL and the current source.
VAA[0-3]	T7, T8, T9, T10	Power, I	2.5V analog power for SAS/SATA PHY.
VAA[4-7]	T13, T14, T15, T16	Power, I	2.5V analog power for SAS/SATA PHY.
VAA_ANA	T18	Power, I	2.5V analog power for PLL.

Table 3-14 Power Interface Signals (continued)

Signal Name	Signal Number	Type	Description
VDD	H6, H7, H8, H9, H10, H13, H14, H15, H16, H17, J6, J17, K6, K17, L6, L17, M6, M17, N6, N17, P6, P17, R6, R7, R8, R9, R10, R13, R14, R15, R16, R17	Power, I	1.0V digital core power.
VDDO1	H18, J18, K18, L18, M18, N18, P18, R18	Power, I	Digital Power. 3.3V I/O Power to supply digital and I/Os.
VDDO2	H5, J5, K5, L5, M5, N5, P5		

Table 3-14 Power Interface Signals (continued)

Signal Name	Signal Number	Type	Description
VSS	A1, A2, A3, A5, A7, A9, A11, A13, A15, A17, A19, A21, A22, AA3, AA5, AA7, AA9, AA11, AA13, AA15, AA17, AA19–AA22, AB1, AB3, AB5, AB7, AB9, AB11, AB13, AB15, AB17, AB19–AB22, B1, B2, B3, B5, B7, B9, B11, B13, B15, B17, B19, B21, B22, C4, C6, C8, C10, C12, C14, C16, C18, C20, D4, D6, D8, D10, D12, D14, D16, D18, D20, E5, E6, E7, E8, E9, E11, E13, E15, E16, E17, E18, E19, F7, F11, F12, F17, F18, G6, G11, G12, G17, G19, H11, H12	Ground	Ground.

Table 3-14 Power Interface Signals (continued)

Signal Name	Signal Number	Type	Description
VSS	J7–J16, J21, K7–K16, L7–L16, M7–M16, M21, N7–N16, P7–P16, R11, R12, R21, T11, T12, T17, U7–U17, U19, V5–V19, W4, W6, W8, W10, W12, W14, W16, W18, W20, Y4, Y6, Y8, Y10, Y12, Y14, Y16, Y18, Y20, Y21	Ground	Ground.

4 LAYOUT GUIDELINES

This chapter describes the system recommendations from the Marvell Semiconductor design and application engineers who work with the 88SE9480/88SE9485. It is written for those who are designing schematics and printed circuit boards for an 88SE9480/88SE9485-based system. Whenever possible, the PCB designer should try to follow the suggestions provided in this chapter.

The information in this chapter is preliminary. Please consult with Marvell Semiconductor design and application engineers before starting your PCB design.

This chapter contains the following sections:

Refer to Chapter 3, Package, for package information.

4.1 88SE9480/88SE9485 Board Schematics

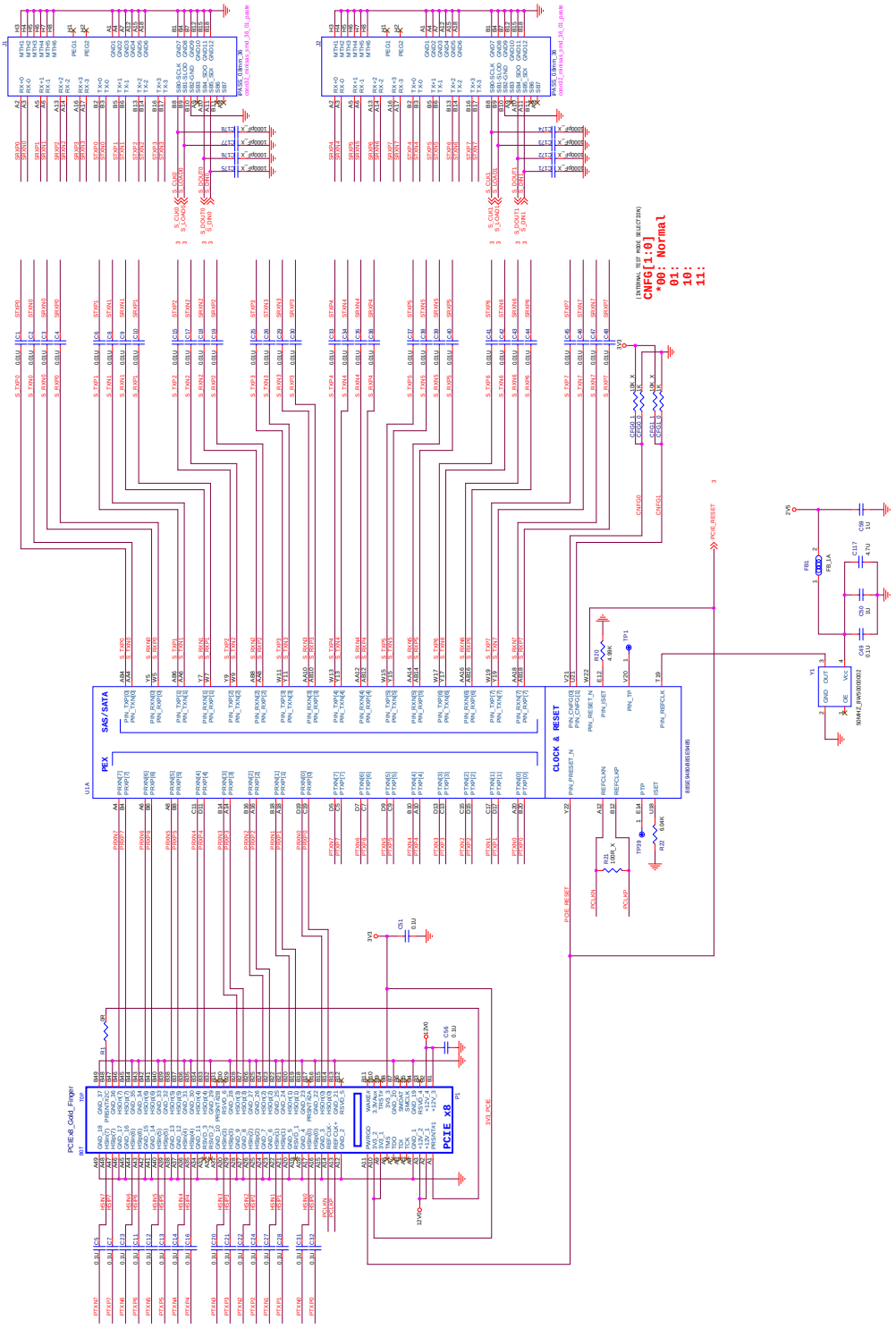
This section contains board schematics for the 88SE9480/88SE9485.

It contains the following figures:

- Figure 4-1, 88SE9480/88SE9485 PCIe and SAS
- Figure 4-2, 88SE9480/88SE9485 Bootstrap, NI, SPI, UART, I2C, LED
- Figure 4-3, 88SE9480/88E9485 Power and Ground

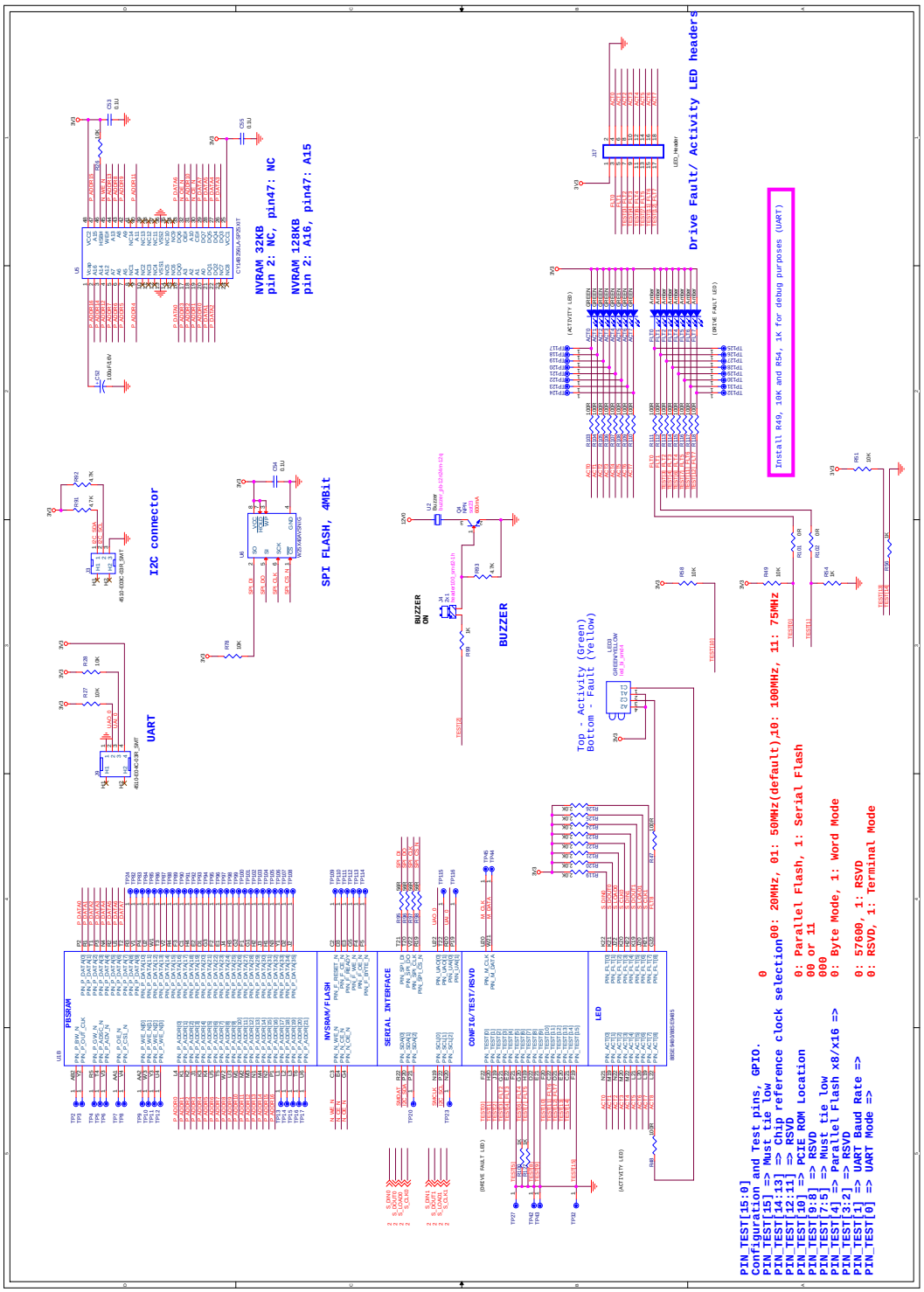
- Figure 4-4, 88SE9480/88SE9485 Power Regulators

Figure 4-1 88SE9480/88SE9485 PCIe and SAS



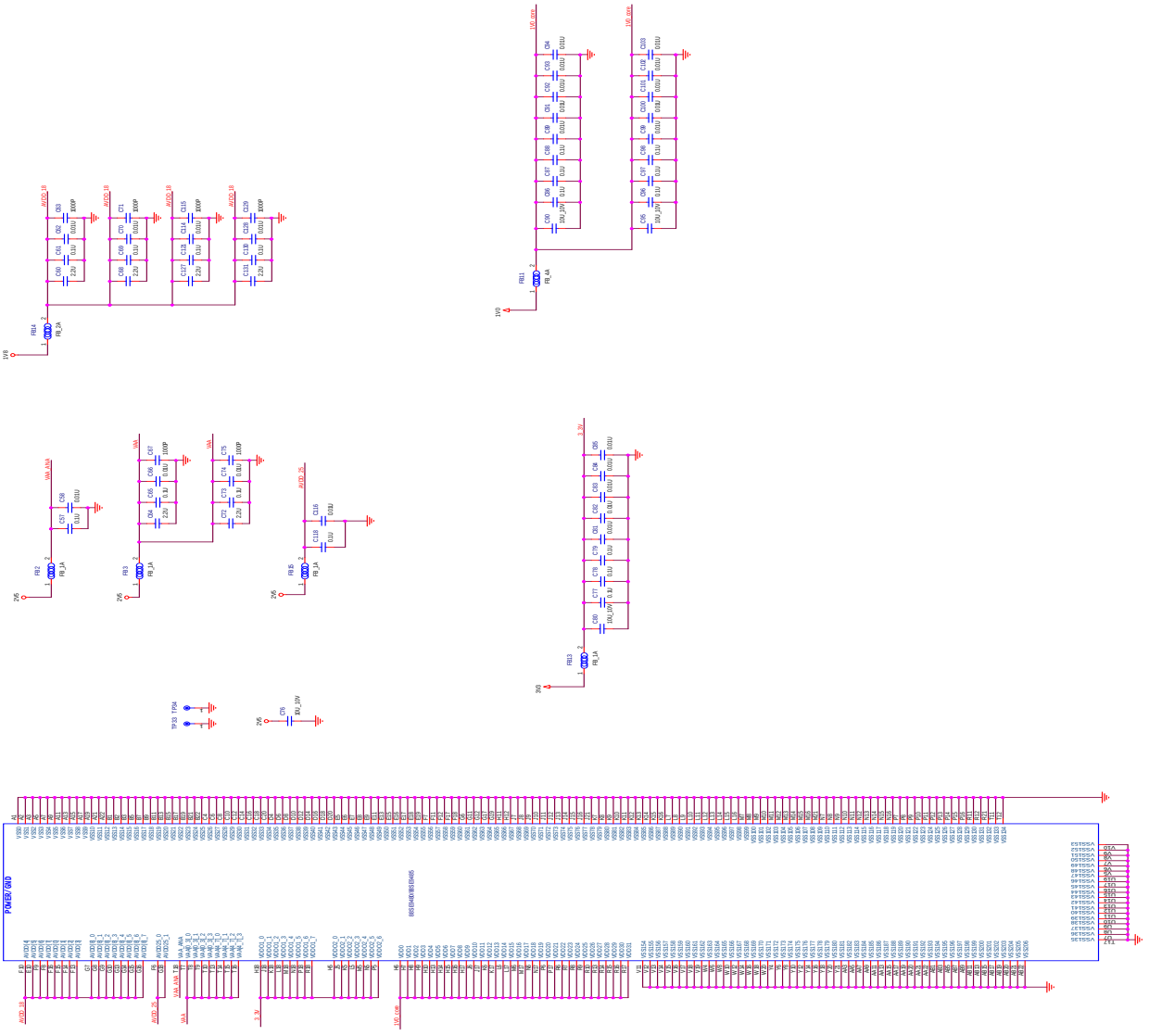
Note: This diagram is for reference only. Contact your Marvell field applications engineer for the latest schematics.

Figure 4-2 88SE9480/88SE9485 Bootstrap, NI, SPI, UART, I2C, LED



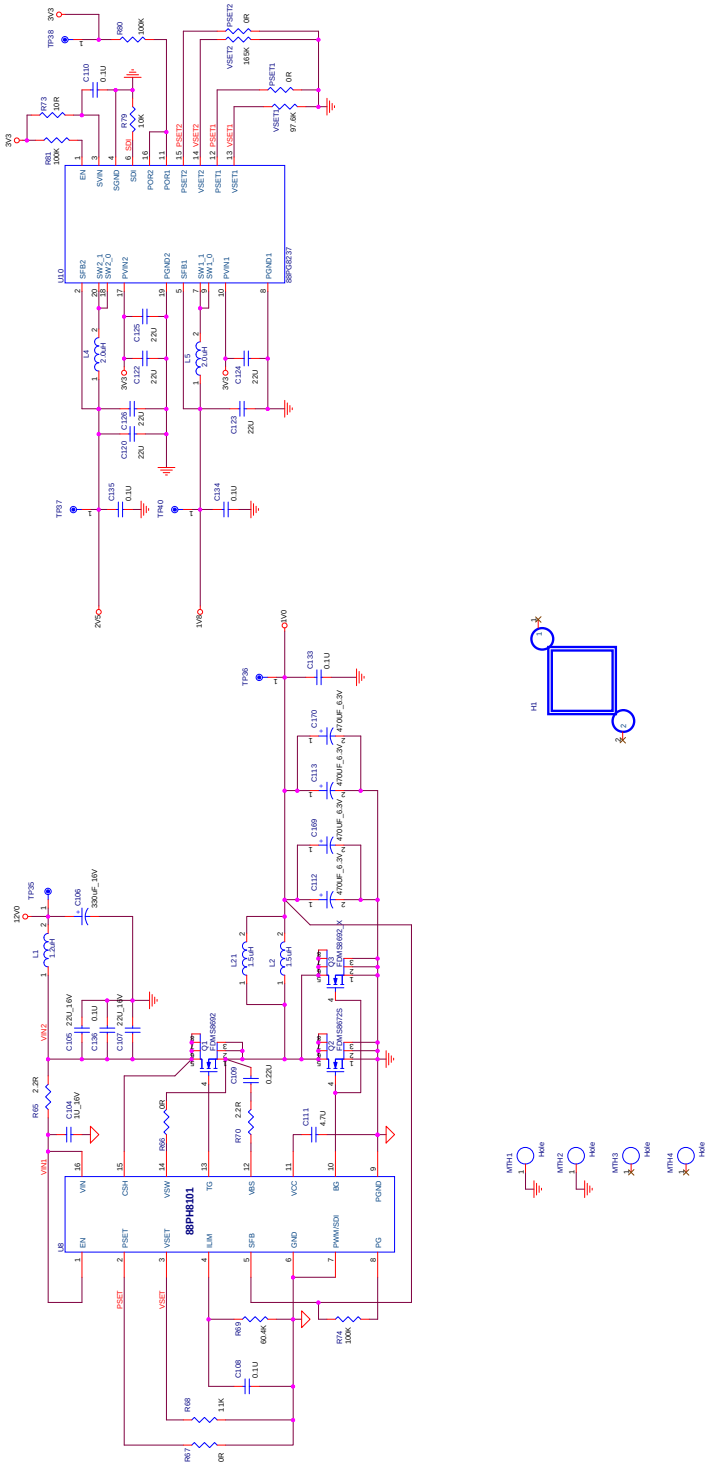
Note: This diagram is for reference only. Contact your Marvell field applications engineer for the latest schematics.

Figure 4-3 88SE9480/88E9485 Power and Ground



Note: This diagram is for reference only. Contact your Marvell field applications engineer for the latest schematics.

Figure 4-4 88SE9480/88SE9485 Power Regulators



Note: This diagram is for reference only. Contact your Marvell field applications engineer for the latest schematics.

4.2 Layer Stack-Up

The following layer stack up is recommended:

- Layer 1–Topside, Parts, Low and High-Speed Signal Routes, and Power Routes
- Layer 2–Solid Ground Plane
- Layer 3–Power Plane and Low Speed Signals
- Layer 4–Power Plane
- Layer 5–Solid Ground Plane
- Layer 6–Bottom Layer, Low and High-Speed Signal Routes, and Power Routes

Note: 5 mil traces and 5 mil spacing are the recommended minimum requirements.

4.2.1 Layer 1–Topside, Parts, Low and High-Speed Signal Routes, and Power Routes

All active parts are to be placed on the topside. Some of the differential pairs for SAS/SATA and PCIe are routed on the top layer, differential 100 ohm impedance needs to be maintained for those high-speed signals.

4.2.2 Layer 2–Solid Ground Plane

A solid ground plane should be located directly below the top layer of the PCB. This layer should be a minimum distance below the top layer in order to reduce the amount of crosstalk and EMI. There should be no cutouts in the ground plane. Use of 1 ounce copper is recommended.

4.2.3 Layer 3–Power Plane and Low Speed Signals

Use solid planes on layer 3 to supply power to the ICs on the PCB. Avoid narrow traces and necks on this plane.

4.2.4 Layer 4–Power Plane

Use solid planes on layer 4 to supply power to the ICs on the PCB. Avoid narrow traces and necks on this plane.

4.2.5 Layer 5–Solid Ground Plane

A solid ground plane should be located directly below the top layer of the PCB. This layer should be a minimum distance below the top layer in order to reduce the amount of crosstalk and EMI. There should be no cutouts in the ground plane. Use of 1 ounce copper is recommended.

4.2.6 Layer 6–Bottom Layer, Low and High-Speed Signal Routes, and Power Routes

Some of the differential pairs for SAS/SATA and PCIe are routed on the top layer, differential 100Ω impedance needs to be maintained for those high speed signals.

4.3 Power Supply

The 88SE9480/88SE9485 operates using the following power supplies:

- VDD Power (1.0V) for the digital core
- PCIe Analog Power Supply (1.8V)
- SAS/SATA Analog Power Supply (2.5V)
- General I/O Power (3.3V)
- Bias Current Resistor (RSET)

4.3.1 VDD Power (1.0V)

All digital power pins (VDD pins) must be connected directly to a VDD plane in the power layer with short and wide traces to minimize digital power-trace inductances.

Use vias close to the VDD pins to connect to this plane and avoid using the traces on the top layer. Marvell recommends placing capacitors around the three sides of the PCB near VDD pins with the following dimensions:

- 0.001 µF (1 capacitor)
- 0.1 µF (2 capacitors)
- 2.2 µF (1 ceramic capacitor)

The combinations of small capacitors are used to suppress switching noise at various frequency ranges. The 2.2 µF ceramic decoupling capacitor is required to filter the lower frequency power-supply noise.

To reduce system noise, place high-frequency surface-mount monolithic ceramic bypass capacitors as close as possible to the channel VDD pins. Place at least one decoupling capacitor on each side of the IC package.

4.3.2 PCIe Analog Power Supply (1.8V)

The analog supply provides power for the PCIe link's high speed serial signals. To ensure high speed link operation, use a series of bypass capacitors for the supplies. A typical capacitor value combination is 1 nF, 0.1µF, and 2.2 µF.

4.3.3 SAS/SATA Analog Power Supply (2.5V)

The analog supply provides power for the SAS/SATA link's high speed serial signals. To ensure high speed link operation, use a series of bypass capacitors for the supplies. A typical capacitor value combination is 1 nF, 0.1µF, and 2.2 µF.

4.3.4 General I/O Power (3.3V)

A general I/O power supply provides power to the GPIO, flash and I2C blocks. A stable and clean power source is desired. Use proper bypass capacitors to provide a clean power source with good stability. A typical capacitor value combination is 0.1µF, and 2.2 µF.

4.3.5 Bias Current Resistor (RSET)

Connect a 6.04KΩ (1%) resistor between the ISET pin and the adjacent top ground plane. This resistor should lie as close as possible to the ISET pin. Avoid routing noisy signals close to the ISET pin.

4.4 PCB Trace Routing

The stack-up parameters for the reference board are shown in Table 4-1.

Table 4-1 PCB Board Stack-up Parameters

Layer	Layer Description	Copper Weight (oz)	Target Impedance (±10%)
1	Signal	0.5	50
2	GND	1	N/A
3	Power and Signal	1	50
4	Power	1	N/A
5	GND	1	N/A
6	Signal	0.5	50

\

4.5 Recommended Layout

High-speed designs must consist of a good board stack-up and careful consideration of the power planes. For the 88SE9480/88SE9485, the following power planes are required:

- VDDIO_C, VDDIO_D, and VDDIO_P power plane (3.3V power source for the digital I/O pins)
- VDD (1.0V power source for the core and digital circuitry)
- VAA (2.5V power source for SAS/SATA analog)
- AVDD (1.8V power source for PCIe analog)

Solid ground planes are recommended. However, special care should be taken when routing VAA, AVDD, and VSS pins.

The following general tips describe what should be considered when determining your stack-up and board routing. These tips are not meant to substitute for consulting with a signal-integrity expert or doing your own simulations.

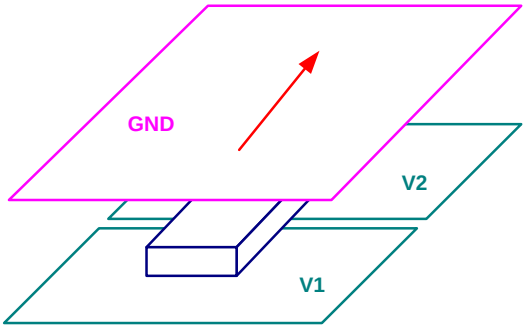
Note: Specific numbers or rules-of-thumb are not used here because they might not be applicable in every situation.

- Do not split ground planes.

  Keep good spacing between possible sensitive analog circuitry on your board and the digital signals to sufficiently isolate noise. A solid ground plane is necessary to provide a good return path for routing layers. Try to provide at least one ground plane adjacent to all routing layers (see Figure 4-5).
- Keep trace layers as close as possible to the adjacent ground or power planes.

  This helps minimize crosstalk and improve noise control on the planes.

Figure 4-5 Trace Has At Least One Solid Plane For Return Path



- When routing adjacent to only a power plane, do not cross splits.

  Route traces only over the power plane that supplies both the driver and the load. Otherwise, provide a decoupling capacitor near the trace at the end that is not supplied by the adjacent power plane.
- Critical signals should avoid running parallel and close to or directly over a gap.

  This would change the impedance of the trace.
- Separate analog powers onto opposing planes.

  This helps minimize the coupling area that an analog plane has with an adjacent digital plane.

- For dual strip-line routing, traces should only cross at 90 degrees.

  Avoid more than two routing layers in a row to minimize tandem crosstalk and to better control impedance.
- Planes should be evenly distributed in order to minimize warping.
- Calculating or modeling impedance should be made prior to routing.

  This helps ensure that a reasonable trace thickness is used and that the desired board thickness is available. Consult with your board fabricator for accurate impedance.
- Allow good separation between fast signals to avoid crosstalk.

  Crosstalk increases as the parallel traces get longer.
- When packages become smaller, route traces over a split power plane

  Smaller packages force vias to become smaller, thereby reducing board thickness and layer counts, which might create the need to route traces over a split power plane. Some alternatives to provide return path for these signals are listed below.

  Caution must be used when applying these techniques. Digital traces should not cross over analog planes, and vice-versa. All of these rules must be followed closely to prevent noise contamination problems that might arise due to routing over the wrong plane.

  By tightly controlling the return path, control noise on the power and ground planes can be controlled.

  - Place a ground layer close enough to the split power plane in order to couple enough to provide buried capacitance, such as SIG-PWR-GND (see Figure 4-6). Return signals that encounter splits in this situation simply jumps to the ground plane, over the split, and back to the other power plane. Buried capacitance provides the benefit of adding low inductance decoupling to your board. Your fabricator may charge for a special license fee and special materials. To determine the amount of capacitance your planes provide, use the following equation:

    $$C = 1.249 \bullet 10^{-13} \bullet E_r \bullet L \bullet W / H$$

    Where E_R is the dielectric coefficient, L • W represents the area of copper, and H is the separation between planes.
  - Provide return-path capacitors that connect to both power planes and jumps the split. Place them close to the traces so that there is one capacitor for every four or five traces. The capacitors would then provide the return path (see Figure 4-7).
  - Allow only static or slow signals on layers where they are adjacent to split planes.

Figure 4-6 shows the ground layer close to the split power plane.

Figure 4-6 Close Power and Ground Planes Provide Coupling For Good Return Path

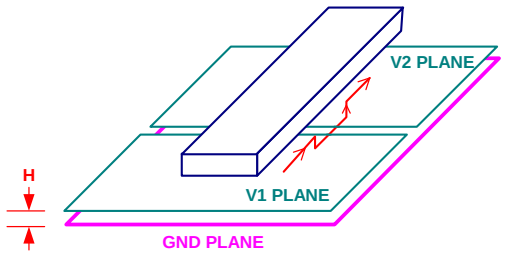
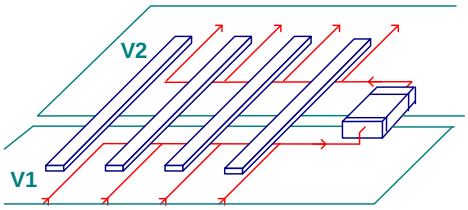


Figure 4-7 shows the thermal ground plane in relation to the return-path capacitor.

Figure 4-7 Suggested Thermal Ground Plane On Opposite Side of Chip



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5 ELECTRICAL SPECIFICATIONS

This chapter contains the following sections:

5.1 Absolute Maximum Ratings

Table 5-1 Absolute Maximum Ratings

Parameter	Symbol	Minimum	Typical	Maximum	Units
Absolute Analog Power for PCIe PHY	AVDD[8:0]	1.62	1.8	1.98	V
Absolute Analog Power for SAS/SATA PHY, Chip PLL	VAA[7:0], VAA_ANA	2.25	2.5	2.75	V
Absolute Power for Digital Core	VDD	0.9	1.0	1.1	V
Absolute Digital I/O Power	VDDO1/VDDO2	3	3.3	3.6	V

CAUTION: Exposure to conditions at or beyond the maximum rating may damage the device. Operation beyond the recommended operating conditions (Table 5-2) is neither recommended nor guaranteed.

Note: Before designing a system, it is recommended that you read application note AN-63: *Thermal Management for Marvell Technology Products*. This application note presents basic concepts of thermal management for integrated circuits (ICs) and includes guidelines to ensure optimal operating conditions for Marvell Technology's products.

5.2 Recommended Operating Conditions

Table 5-2 Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units
Analog Power for PCIe PHY	AVDD[8:0]	1.71	1.8	1.89	V
Analog Power for SAS/SATA PHY, Chip PLL	VAA[7:0], VAA_ANA	2.38	2.5	2.63	V
Digital Core Power	VDD	0.95	1.0	1.05	V
Digital I/O Power	VDDO1/VDDO2	3.14	3.3	3.47	V
Internal Bias Reference	ISET, PIN_ISET	5.74	6.04	6.34	KΩ
Ambient Operating Temperature	T_A	0	N/A	70	°C
Junction Operating Temperature	T_J	0	N/A	125	°C

CAUTION: Operation beyond the recommended operating conditions is neither recommended nor guaranteed.

5.3 DC Electrical Characteristics

Table 5-3 DC Electrical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Units
Analog Power for PCIe PHY 1.8V	I_{AVDD}	N/A	0.78	N/A	A
Analog Power for SAS/SATA PHY 2.5V, Chip PLL	I_{VAA}	N/A	0.78	N/A	A
Digital Core Power	I_{VDD}	N/A	2.0	N/A	A
Digital I/O Power	I_{VDDO}	N/A	50	N/A	mA
Input Low Voltage of Digital I/O	V_{IL}	-0.4	N/A	0.3 × VDDOx	V
Input High Voltage of Digital I/O	V_{IH}	0.7 × VDDOx	N/A	VDDOx + 0.4	V
Output Low Voltage of Digital I/O	V_{OL}	N/A	0.13	N/A	V
Output High Voltage of Digital I/O	V_{OH}	2.0	VDDOx*	N/A	V

* VDDOx: VDDO1/VDDO2.

CAUTION: Operation beyond the recommended operating conditions is neither recommended nor guaranteed.

Table 5-4 shows the internal pull-up and pull-down strength.

Table 5-4 Internal Pull-Up and Pull-Down Strength

Specifications	Condition	Minimum	Nominal	Maximum	Unit
Pull-Up Strength	V(PAD) = 0.5 × VDDO	10	N/A	50	µA
	V(PAD) = 0	10	N/A	65	µA
Pull-Down Strength	V(PAD) = 0.5 × VDDO	10	N/A	50	µA

5.4 Thermal Data

It is recommended to read application note *AN-63 Thermal Management for Selected Marvell® Products* (Document Number MV-S300281-00) and the *ThetaJC, ThetaJA, and Temperature Calculations White Paper*, available from Marvell, before designing a system. These documents describe the basic understanding of thermal management of integrated circuits (ICs) and guidelines to ensure optimal operating conditions for Marvell products.

Table 5-5 provides the thermal data for the 88SE9480/88SE9485. The simulation was performed according to JEDEC standards. The heat sink is 25.4 mm × 25.4 mm × 25 mm.

Table 5-5 shows the values for the package thermal parameters for the484-ball HSBGA mounted on a 4-layer PCB.

Table 5-5 Package Thermal Data, 4-Layer PCB*

Parameter	Definition	Airflow Value			
		0 m/s	1 m/s	2 m/s	3 m/s
θ_{JA}	Thermal resistance: junction to ambient (no heat sink)	16.2 C/W	13.9 C/W	13.0 C/W	12.6 C/W
θ_{JA}	Thermal resistance: junction to ambient (with heat sink)	11.7 C/W	8.4 C/W	7.8 C/W	7.6 C/W
θ_{JC}	Thermal resistance: junction to case	5.30 C/W	N/A	N/A	N/A

* All data is based on parts mounted on a 4” x 4.5” JEDEC 4L PCB.

5.5 AC Timing

This section discusses the following topics:

- SATA
- PCIe
- Parallel Flash and NVSRAM

5.5.1 SATA

This product conforms to AC timing requirements as specified in the *Serial ATA Revision 3.0 Specification* (www.sata-io.org).

5.5.2 PCIe

This product conforms to AC timing requirements as specified in the *PCIe® Base 2.0* specification (www.pcisig.com/).

5.5.3 Parallel Flash and NVSRAM

This section describes the timing for Parallel Flash and NVSRAM.

Figure 5-1 illustrates the Parallel Flash and NVSRAM Read timing, and Table 5-6 provides parameter information for the timing diagram.

Figure 5-1 Parallel Flash / NVSRAM Read Timing

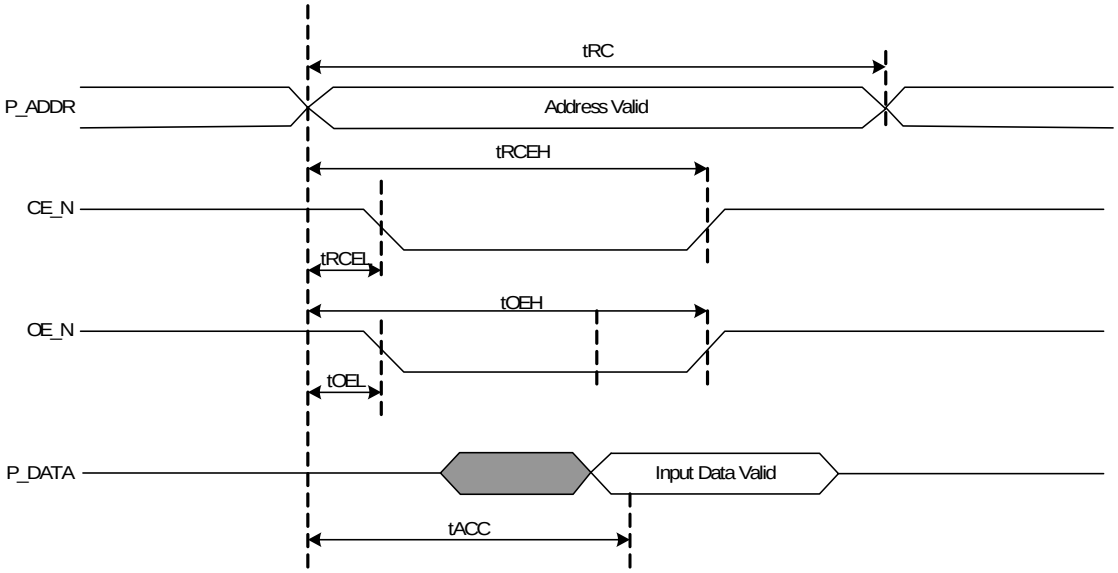

Table 5-6 Timing Parameters for Figure 5-1, Parallel Flash / NVSRAM Read Timing

Parameter	Description	NVSRAM	Parallel Flash	Unit
tRC	Read Cycle Time	(NV_RD_CYCLE_TM (R0C968h [7:0]) + 2) × Tclk	(FLSH_RD_CYCLE_TM (R0C978h [7:0]) + 2) × Tclk	ns
tRCEL	Read CE Assert Time	(NV_RD_CE_ASSRT_TM (R0C96Ch [23:16]) + 1) × Tclk	(FLSH_RD_CE_ASSRT_TM (R0C97Ch [23:16]) + 1) × Tclk	ns
tRCEH	Read CE Deassert Time	(NV_RD_CE_DEASSRT_TM (R0C96Ch [31:24]) + 2) × Tclk	(FLSH_RD_CE_DEASSRT_TM (R0C97Ch [31:24]) + 2) × Tclk	ns
tOEL	Read OE Assert Time	(NV_RD_OE_ASSRT_TM (R0C96Ch [7:0]) + 1) × Tclk	(FLSH_RD_OE_ASSRT_TM (R0C97Ch [7:0]) + 1) × Tclk	ns
tOEH	Read OE Deassert Time	(NV_RD_OE_DEASSRT_TM (R0C96Ch [15:8]) + 2) × Tclk	(FLSH_RD_OE_DEASSRT_TM (R0C97Ch [15:8]) + 2) × Tclk	ns
tACC	Read Data Latch Time	(NV_RD_DATA_LTCH_TM (R0C968h [15:8]) + 1) × Tclk - 20	(FLSH_RD_DATA_LTCH_TM (R0C978h [15:8]) + 1) × Tclk - 20	ns

Note: Tclk—Internal system clock cycle, default value is 3.33ns.

Figure 5-2 illustrates the Parallel Flash and NVSRAM Write timing, and Table 5-7 provides parameter information for the timing diagram.

Figure 5-2 Parallel Flash / NVSRAM Write Timing

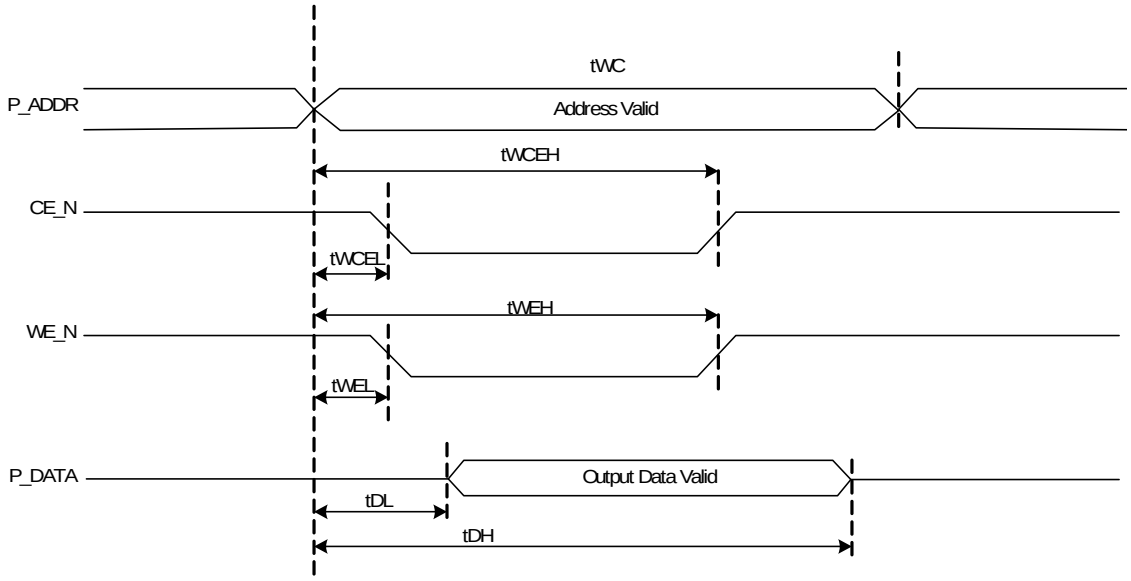

Table 5-7 Timing Parameters for Figure 5-1, Parallel Flash / NVSRAM Read Timing

Parameter	Description	NVSRAM	Parallel Flash	Unit
tWC	Write Cycle Time	(NV_WRT_CYCLE_TM (R0C960h [7:0]) + 2) × Tclk	(FLSH_WRT_CYCLE_TM (R0C970h [7:0]) + 2) × Tclk	ns
tWCEL	Write CE Assert Time	(NV_CE_ASSRT_TM (R0C960h [15:8]) + 1) × Tclk	(FLSH_CE_ASSRT_TM (R0C970h [15:8]) + 1) × Tclk	ns
tWCEH	Write CE Deassert Time	(NV_CE_DEASSRT_TM (R0C960h [23:16]) + 2) × Tclk	(FLSH_CE_DEASSRT_TM (R0C970h [23:16]) + 2) × Tclk	ns
tWEL	Write WE Assert Time	(NV_WRT_WE_ASSRT_TM (R0C964h [7:0]) + 1) × Tclk	(FLSH_WRT_WE_ASSRT_TM (R0C974h [7:0]) + 1) × Tclk	ns
tWEH	Read WE Deassert Time	(NV_WRT_WE_DEASSRT_TM (R0C964h [15:8]) + 2) × Tclk	(FLSH_WRT_WE_DEASSRT_TM (R0C974h [15:8]) + 2) × Tclk	ns
tDL	Write Data IO Enable Time	(NV_WRT_DATA_IO_EN_TM (R0C964h [23:16]) + 1) × Tclk	(FLSH_WRT_DATA_IO_EN_TM (R0C974h [23:16]) + 1) × Tclk	ns
tDH	Write Data IO Disable Time	(NV_WRT_DATA_IO_DSBL_TM (R0C964h [31:24]) + 2) × Tclk	(FLSH_WRT_DATA_IO_DSBL_TM (R0C974h [31:24]) + 2) × Tclk	ns

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