



# 88SE9171 R1.2

One-Lane PCIe 2.0 to One-Port 6  
Gbps SATA I/O Controller

**Preliminary Datasheet**

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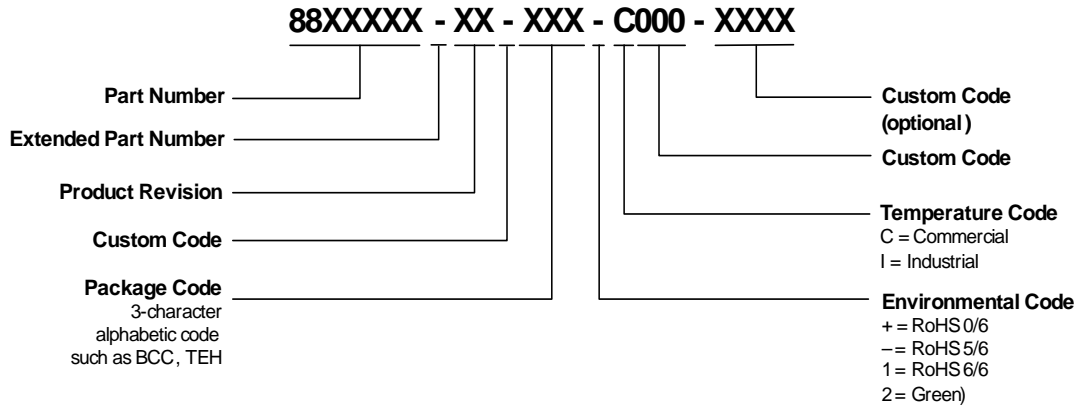
Patent(s) Pending—Products identified in this document may be covered by one or more Marvell patents and/or patent applications.

## ORDERING INFORMATION

### Ordering Part Numbers and Package Markings

The following figure shows the ordering part numbering scheme for the 88SE9171 part. For complete ordering information, contact your Marvell FAE or sales representative.

#### Sample Ordering Part Number



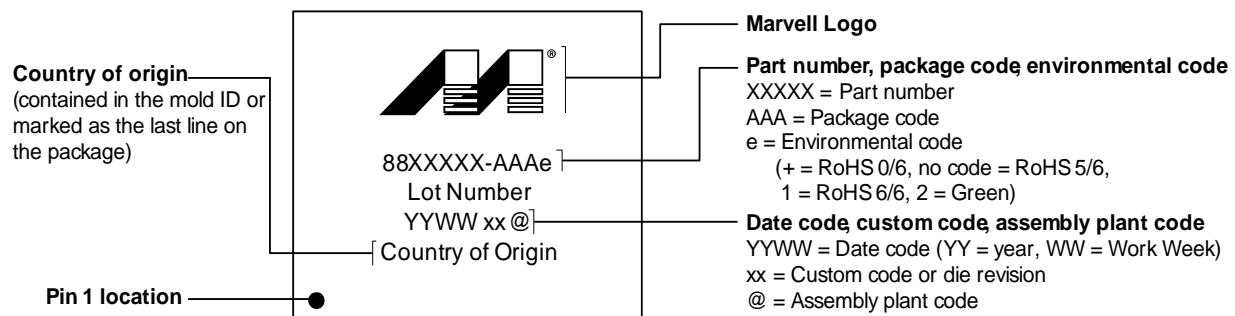
The standard ordering part numbers for the respective solutions are indicated in the following table.

#### Ordering Part Numbers

Part Number	Description
88SE9171A2-NNX2C000	56-Pin QFN 7 mm x 7 mm, PCIe 2.0 x1 to one 6 Gbps SATA I/O Controller
88SE9171A2-NNX2I000	56-Pin Industrial Grade QFN 7 mm x 7 mm, PCIe 2.0 x1 to one 6 Gbps SATA I/O Controller
88SE9171A2-NNX2A000	56-Pin Automotive Grade QFN 7 mm x 7 mm, PCIe 2.0 x1 to one 6 Gbps SATA I/O Controller *
88SE9171A2-NNX2C000-P115	56-Pin QFN 7 mm x 7 mm, PCIe 2.0 x1 to one 6 Gbps SATA I/O Controller
88SE9171A2-NNX2C000TP115	56-Pin QFN 7 mm x 7 mm, PCIe 2.0 x1 to one 6 Gbps SATA I/O Controller

The next figure shows a typical Marvell package marking.

#### 88SE9171 Package Marking and Pin 1 Location





**Note:** The above drawing is not drawn to scale. The location of markings is approximate. Add-on marks are not represented. Flip chips vary widely in their markings and flip chip examples are not shown here. For flip chips, the markings may be omitted per customer requirement.

# CHANGE HISTORY

## Document Changes \*

Location	Type	Description	Date
Global	Update	Changed all instances of "Processor" to "Controller."	March 7, 2014
Global	Update	Removed all instances of "3 Gbps" from various chapters and the heading and title of book.	March 7, 2014
Global	Update	Removed the note "This field is writable through the Mbus."	March 11, 2014
N/A	Update	Removed Read Sequence Example.	August 20, 2014
N/A	Update	Removed Write Sequence Example.	August 20, 2014
Page 3-6	Update	Removed "when input" from the descriptions of the PU and PD pin types in Table 3-1, <a href="#">Pin Type Definitions</a> .	March 7, 2014
Page 3-9	Update	Updated the "1%" to +/- 1%" in the ISET description in Table 3-5, <a href="#">Reference Signals</a> .	March 7, 2014
Page 3-9	Update	Removed the following note from Table 3-6, <a href="#">General Purpose I/O Signals</a> : <b>Note:</b> For normal operation GPIO1 and GPIO1 should not be pulled down. The GPIO[3] pin is used as sample-at-reset bootstrap pins	March 7, 2014
Page 3-9	Update	Merged the GPIO4 pin in Table 3-6, <a href="#">General Purpose I/O Signals</a> to the same group-line as GPIO0 through GPIO3.	March 7, 2014
Page 5-3	Update	Removed the Alternate Digital I/O Power (2.5V) parameter from Table 5-2, <a href="#">Recommended Operating Conditions</a> .	March 11, 2014

\* The type of change is categorized as: Parameter, Revision, or Update. A Parameter change is a change to a spec value, a Revision change is one that originates from the chip Revision Notice, and an Update change includes all other document updates.



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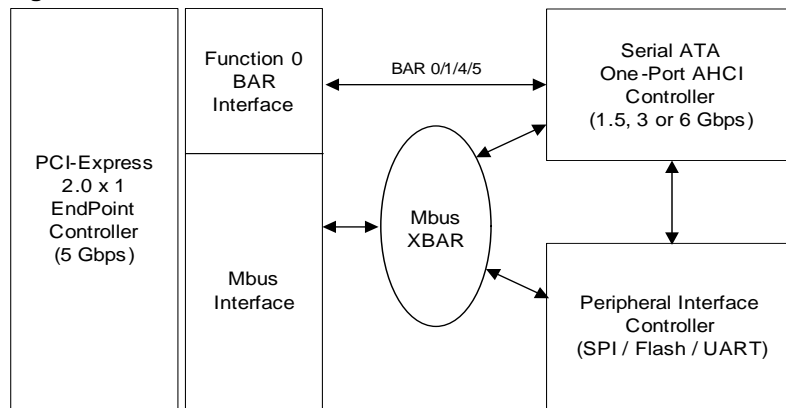


# 1 OVERVIEW

The 88SE9171 is a one-port, 6 Gbps SATA I/O controller with a one-lane PCIe 2.0 interface. The 88SE9171 supports devices compliant with the Serial ATA International Organization: Serial ATA Revision 3.0 specification.

Figure 1-1 shows the system block diagram for the 88SE9171.

**Figure 1-1 88SE9171 Block**





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# 2 FEATURES

This chapter contains the following sections:

- General
- PCIe
- SATA Controller
- SPI Interface Controller
- Peripheral Interface Controller



## 2.1 General

- 55 nm CMOS process, 1.0V digital core, 1.8V analog, and 3.3V I/O power supplies.
- An optional on-die regulator can be used with an external PNP bipolar device to generate a 1.0V supply to the chip from an 1.8V power source.
- Reference clock frequency of 25 MHz, provided by an external clock source or generated by an external crystal oscillator.

## 2.2 PCIe

- PCIe 2.0 endpoint device.
- Supports one lane.
- Compliant with PCIe 2.0 specifications.
- Supports communication speeds of 2.5 Gbps and 5.0 Gbps.
- Supports IDE programming interface registers for the SATA controller.
- Supports AHCI programming interface registers for the SATA controller.
- Supports aggressive power management.
- Supports error reporting, recovery, and correction.
- Supports Message Signaled Interrupt (MSI).

## 2.3 SATA Controller

- Compliant with Serial ATA Specification 3.0.
- Supports communication speeds of 6.0 Gbps, 3.0 Gbps, and 1.5 Gbps.
- Supports programmable transmitter signal levels.
- Supports Gen 1i, Gen 1x, Gen 2i, Gen 2m, Gen 2x, and Gen 3i.
- Supports one SATA port.
- Supports AHCI 1.0 and IDE programming interface.
- Supports Native Command Queuing (NCQ).
- Supports Port Multiplier FIS-based switching or command-based switching.
- Supports Partial and Slumber Power Management states.
- Supports Staggered Spin-up.

## 2.4 SPI Interface Controller

- A four-pin interface provides read and write access to an external SPI flash or SPI ROM device.
- Vendor-specific information stored in the external device is read by the controller during the chip power-up.
- PCI BootROM can be stored in the external SPI device and read through the Expansion ROM BAR and the SPI interface controller.



## 2.5 Peripheral Interface Controller

- Six General Purpose I/O (GPIO) ports.
  - Each of the six GPIO pins can be assigned to act as a general input or output pin.
  - Each of the GPIO inputs can be programmed to generate an edge-sensitive or a level-sensitive maskable interrupt.
  - Each of the GPIO outputs can be programmed for a connected LED to blink at a user-defined fixed rate. The default rate is 100 ms.



# 3 PACKAGE

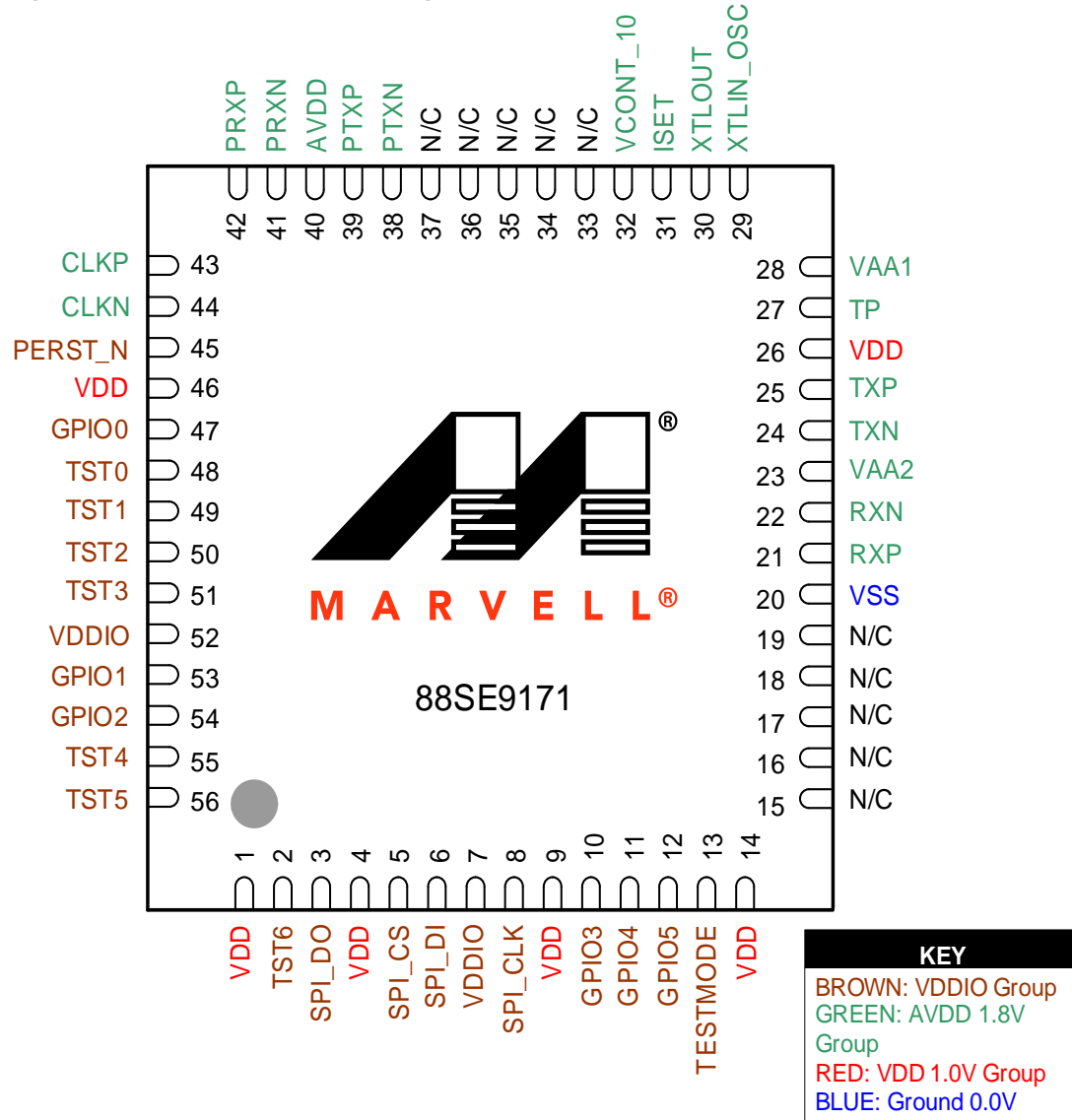
This chapter contains the following sections:

- Pin Diagram
- Mechanical Dimensions
- Signal Descriptions

### 3.1 Pin Diagram

The 56-pin QFN pin diagram is illustrated in Figure 3-1.

Figure 3-1 88SE9171 56-Pin QFN Diagram

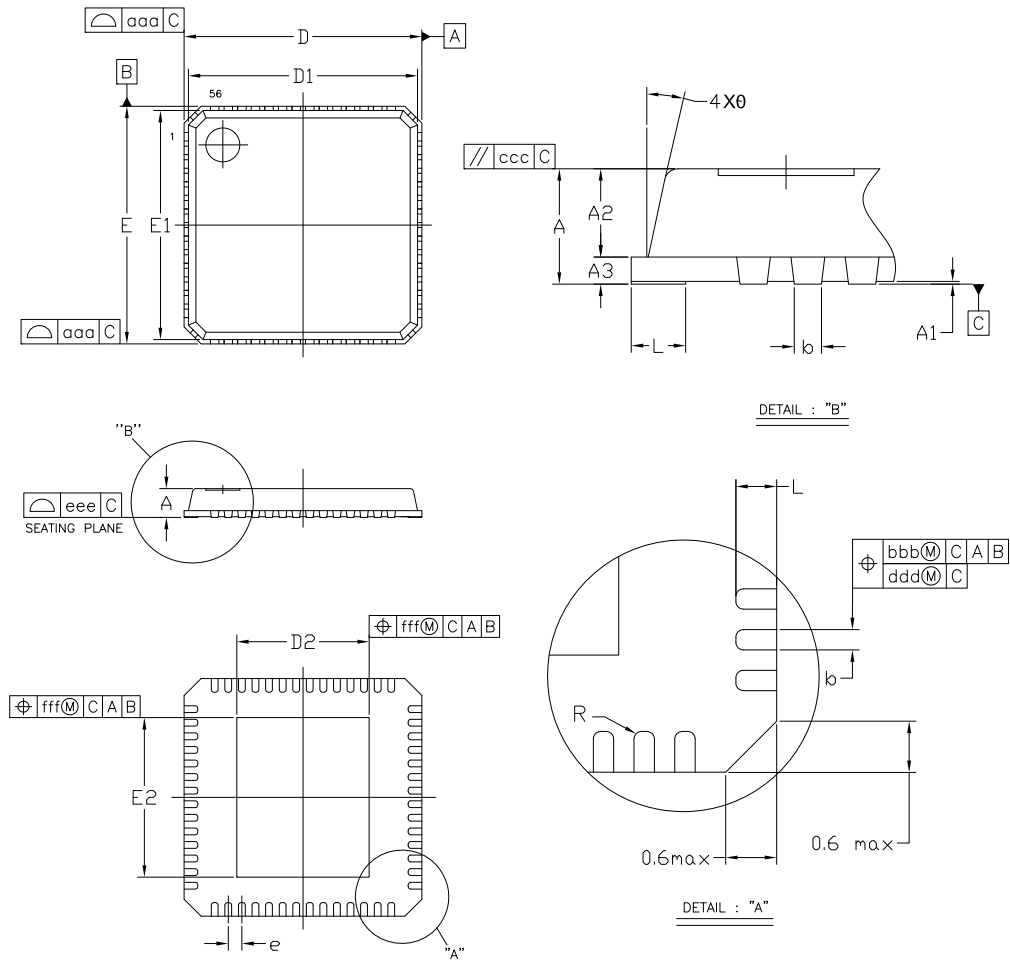


**Note:** The center area beneath the chip is the Exposed Die Pad (Epad). When designing the PCB, create a solder pad for the Epad and connect the Epad to ground.

### 3.2 Mechanical Dimensions

The package mechanical drawing is shown in Figure 3-2.

Figure 3-2 Package Mechanical Diagram



The package mechanical dimensions are shown in Figure 3-3.

**Figure 3-3 Package Mechanical Dimensions**

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	0.60	0.65	0.70	0.024	0.026	0.028
A3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	7.00 BSC			0.276 BSC		
D1/E1	6.75 BSC			0.266 BSC		
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
θ	0°	---	14°	0°	---	14°
R	0.075	---	---	0.003	---	---
aaa	---	---	0.10	---	---	0.004
bbb	---	---	0.07	---	---	0.003
ccc	---	---	0.10	---	---	0.004
ddd	---	---	0.05	---	---	0.002
eee	---	---	0.08	---	---	0.003
fff	---	---	0.10	---	---	0.004

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT : JEDEC MO-220.

Option	Symbol	Die Pad Size Options		Shape Option
		Dimension in mm	Dimension in inch	
	D <sub>2</sub>	3.50 ± 0.20	0.138 ± 0.008	Rectangular
	E <sub>2</sub>	3.80 ± 0.20	0.150 ± 0.008	

### 3.3 Signal Descriptions

This section contains the pin types and signal descriptions for the 88SE9171 package.

#### 3.3.1 Pin Type Definitions

Pin type definitions are shown in Table 3-1.

**Table 3-1 Pin Type Definitions**

Pin Type	Definition
I/O	Input and output
I	Input only
O	Output only
mA	DC sink capability (All GPIO and TST pins are 12 mA)
5	5V tolerance (All GPIO and TST pins are 5V tolerance)
A	Analog
PU	Internal pull-up
PD	Internal pull-down
OD	Open-drain pad

#### 3.3.2 Signal Descriptions

This section outlines the 88SE9171 pin descriptions. All signals ending with the letter N indicate an active-low signal.

**Table 3-2 PCIe Interface Signals**

Signal Name	Signal Number	Type	Description
PERST_N	45	5, I, PU	PCI Platform Reset. Active low, indicates when the applied power is within the specified tolerance and stable.
CLKP	43	I, A	Reference Clock.
CLKN	44		Low voltage differential signals. The clock frequency has to be 100 MHz.
PRXP	42	I, A	PCIe differential signals to the controller's receiver.
PRXN	41		
PTXP	39	O, A	PCIe differential signals from the controller's transmitter.
PTXN	38		

**Table 3-3 Serial ATA Interface Signals**

Signal Name	Signal Number	Type	Description
TXN	24	O, A	Serial ATA Transmitter Differential Outputs.
TXP	25		
RXP	21	I, A	Serial ATA Receiver Differential Inputs.
RXN	22		

**Table 3-4 Reference Signals**

Signal Name	Signal Number	Type	Description
ISET	31	I/O, A	Reference Current for Crystal Oscillator and PLL. This pin has to be connected to an external 6.04 kΩ 1% resistor to Ground.
XTLOUT	30	O, A	Crystal Output.
XTLIN_OSC	29	I, A	Reference Clock Input. This signal can be from an oscillator, or connected to a crystal with the XTLOUT pin. The clock frequency must be 25 MHz ± 80 ppm.

**Table 3-5 General Purpose I/O Signals**

Signal Name	Signal Number	Type	Description
GPIO0	47	5, I/O, 12 mA, PU	General Purpose I/O.
GPIO1	53		
GPIO2	54		
GPIO3	10		
GPIO4	11		
GPIO5	12		

**Table 3-6 SPI Flash Interface Signals**

Signal Name	Signal Number	Type	Description
SPI_CLK	8	5, O, 12 mA	SPI Interface Clock.
SPI_DI	6	5, I, PU	Serial Data In. Connect to the serial flash device's serial data output (DO).

**Table 3-6 SPI Flash Interface Signals** (continued)

Signal Name	Signal Number	Type	Description
SPI_CS	5	5, O, 12 mA	SPI Interface Chip Select.
SPI_DO	3	5, O, 12 mA	Serial Data Out. Connect to the serial flash device's serial data input (DI).

**Table 3-7 Test Pins**

Signal Name	Signal Number	Type	Description
TST0	48	5, I/O, 12 mA, PU	Digital Test Pins. This pin works as UART input (UAI) in normal function mode.
TST1	49		Digital Test Pin. This pin works as UART output (UAO) in normal function mode.
TST2	50		Digital Test Pins.
TST3	51		
TST4	55		
TST5	56		
TST6	2		

**Table 3-8 Test Mode Interface Signals**

Signal Name	Signal Number	Type	Description
TP	27	I/O, A	Analog Test Point for PCIe PHY, SATA PHY, crystal oscillator, and PLL.
TESTMODE	13	5, I, PD	Test Mode. Enables chip test modes.

**Table 3-9 Power and Ground Pins**

Signal Name	Signal Number	Type	Description
VCONT_10	32	O, A	Voltage Control. Output signal which is connected to the base of an external BJT component to generate a 1.0V supply from 1.8V.
VAA2	23	Power	Analog power. 1.8V analog power supply for SATA PHY.

**Table 3-9 Power and Ground Pins** (continued)

Signal Name	Signal Number	Type	Description
VAA1	28	Power	Analog power 1.8V analog power for crystal oscillator, reference current generator, PLL, and internal voltage regulator.
AVDD	40	Power	Analog power. 1.8V analog power supply for PCIe PHY.
VDDIO	7 52	Power	I/O Power. 3.3V analog power supply for digital I/Os.
VDD	1, 4, 9, 14, 26, 46	Power	1.0V Core Digital Power.
VSS	20	Power	Ground. The main ground is the exposed die-pad (ePad) on the bottom side of the package.

**Table 3-10 Not Connected**

Signal Name	Signal Number	Type	Description
N/C	15, 16, 17, 18, 19, 33, 34, 35, 36, 37	N/A	Not connected.

**Note:** At-Speed PLL and PHY Test entries marked containing “/4” indicate 1/4 rates.



# 4 LAYOUT GUIDELINES

This chapter describes the system recommendations from the Marvell Semiconductor design and application engineers who work with the 88SE9171. It is written for those who are designing schematics and printed circuit boards for an 88SE9171-based system. Whenever possible, the PCB designer must try to follow the suggestions provided in this chapter.

The information in this chapter is preliminary. Please consult with Marvell Semiconductor design and application engineers before starting your PCB design.

The chapter contains the following sections:

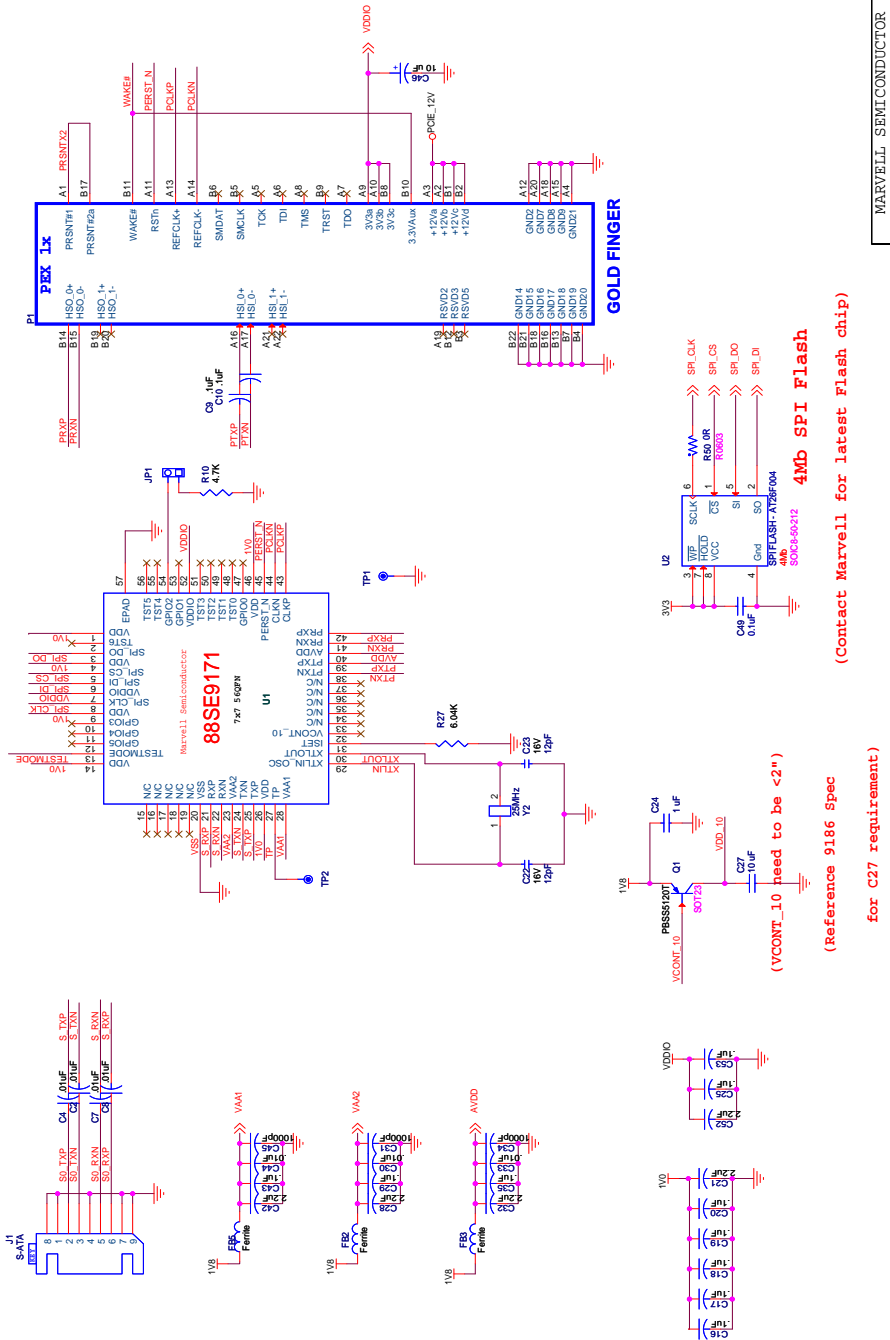
- [Board Schematic Example](#)
- [External Voltage Regulator](#)
- [Layer Stack-up](#)
- [Power Supply](#)
- [PCB Trace Routing](#)
- [Recommended Layout](#)

Refer to Chapter 3, [Package](#), for package information.

## 4.1 Board Schematic Example

The board schematic consists of the major interfaces of the 88SE9171 including SATA and PCIe. Figure 4-1 shows an example board schematic.

Figure 4-1 88SE9171 Example Board Schematic

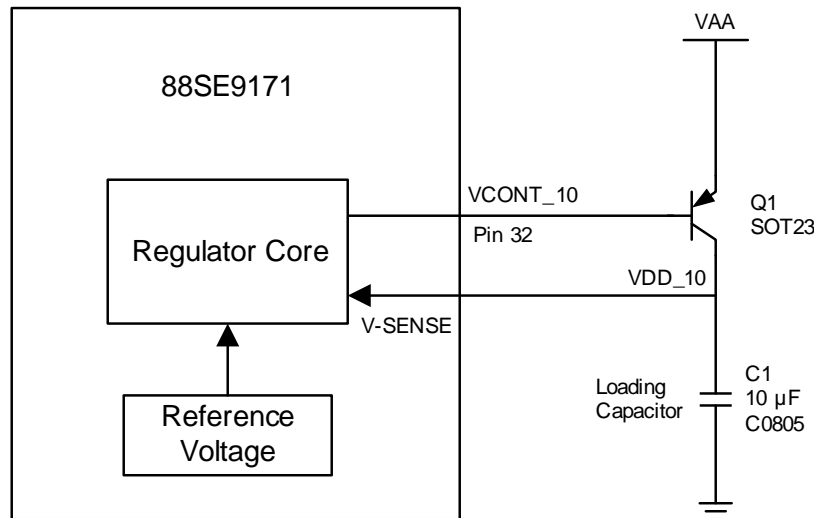


**Note:** Please contact your Marvell field applications engineer for the latest schematics.

## 4.2 External Voltage Regulator

The external voltage regulator consists of an external Bipolar Junction Transistor (BJT). The voltage level is on the **VCONT\_10** voltage control pin and it supplies **VDD\_10** to the core power. The collector of the BJT provides a stable voltage source and sufficient current to drive the 88SE9171. Figure 4-2 shows a block diagram of the voltage regulator loop.

Figure 4-2 88SE9171 Voltage Regulator Loop Block Diagram



The BJT's supply voltage, **VAA**, can use the same source as the 88SE9171's **VAA1** or **VAA2**. The BJT and the internal regulator core forms a closed feedback loop to provide a stable voltage for **VDD\_10**.

### 4.2.1 Recommended Components

For stability reasons, the loading capacitor on the collector output has a low Effective Series Resistance (ESR). The ESR is inversely proportional to the zero location. Table 4-1 describes the recommended components for the reference design.

Table 4-1 Component List

Symbol	Manufacturer	Part Number	Description
C1	Johansen Dialectrics	6R3R15X106KV4E	10 µF Tanceram Capacitor. <ul style="list-style-type: none"> <li>ESR of 20–50 mΩ at 1 MHz UGBW</li> <li>High DC breakdown</li> <li>Low DC leakage</li> </ul> <p><b>Note:</b> The second pole must be kept away from the UGBW because of parasitic RC inside the BJT.</p>
Q1	Phillips Semiconductor	PBSS5120T	Low $V_{CESAT}$ PNP transistor.

#### 4.2.2 External BJT Requirements

An  $h_{FE}$  of 200–400 is required when the BJT output current ( $I_C$ ) reaches its maximum, and low  $V_{CESAT}$  (about 200 mV at  $I_{Cmax}$ ). The trace length between the BJT and the **VCONT\_10** pin of the 88SE9171 must be less than 0.5 in. The control signal **VCONT\_10** connects to the base of the BJT. The PCB trace for the BJT and the load capacitor must be about 10 mils wide.

Regarding thermal characteristics, the mounting pad for the collector must be at least 1 cm<sup>2</sup> tin plated with single-sided copper. The typical power dissipation is approximately 0.5W for this BJT. Electrical requirements for the BJT are listed in Table 5-4, [External BJT Requirements](#).

## 4.3 Layer Stack-up

The following layer stack up is recommended:

- Layer 1–Topside, Parts, Slow and High Speed Signal Routes, and Power Routes
- Layer 2–Solid Ground Plane
- Layer 3–Power Plane
- Layer 4–Bottom Layer, Slow and High-Speed Signal Routes, and Power Routes

5 mil traces and 5 mil spacing are the recommended minimum requirements.

### 4.3.1 Layer 1–Topside, Parts, Slow and High Speed Signal Routes, and Power Routes

All active parts are to be placed on the topside. Some of the differential pairs for SATA and PCIe are routed on the top layer, differential 100 ohm impedance needs to be maintained for those high speed signals.

### 4.3.2 Layer 2–Solid Ground Plane

A solid ground plane must be located directly below the top layer of the PCB. This layer must be a minimum distance below the top layer in order to reduce the amount of crosstalk and EMI. No cutouts must exist in the ground plane. Use of 1 ounce copper is recommended.

### 4.3.3 Layer 3–Power Plane

Use solid planes on layer 3 to supply power to the ICs on the PCB. Avoid narrow traces and necks on this plane.

### 4.3.4 Layer 4–Bottom Layer, Slow and High-Speed Signal Routes, and Power Routes

Some of the differential pairs for SATA and PCIe are routed on the top layer, differential 100Ω impedance needs to be maintained for those high speed signals. The high speed signals have the return current on the third layer, which is the power plane. Make sure there is no cut-out under the signal path.

## 4.4 Power Supply

The 88SE9171 operates using the following power supplies:

- VDD Power (1.0V) for the digital core
- Analog Power Supply (1.8V)

### 4.4.1 VDD Power (1.0V)

All digital power pins (VDD pins) must be connected directly to a VDD plane in the power layer with short and wide traces to minimize digital power-trace inductances.

Use vias close to the VDD pins to connect to this plane and avoid using the traces on the top layer. Marvell recommends placing capacitors around the three sides of the PCB near VDD pins with the following dimensions:

- 1 nF (1 capacitor)
- 0.1  $\mu$ F (2 capacitors)
- 2.2  $\mu$ F (1 ceramic capacitor)

The 2.2  $\mu$ F ceramic decoupling capacitor is needed to filter the lower frequency power-supply noise.

To reduce system noise, the use of high-frequency surface-mount monolithic ceramic bypass capacitors must be placed as close as possible to the channel VDD pins. At least one decoupling capacitor must be placed on each side of the IC package.

Short and wide copper traces must be used to minimize parasitic inductances. Low-value capacitors (1,000–10,000 pF) are preferable over higher values because they are more effective at higher frequencies.

### 4.4.2 Analog Power Supply (1.8V)

The PCIe analog supply provides power for the PCIe link's high speed serial signals. To ensure high speed link operation, use a series of bypass capacitors for the supplies. A typical capacitor value combination is 1 nF, 0.1 $\mu$ F, and 2.2  $\mu$ F.

### 4.4.3 Bias Current Resistor (RSET)

Connect a 6.04K $\Omega$  (1%) resistor between the ISET pin and the adjacent top ground plane. This resistor must lie as close as possible to the ISET pin.

## 4.5 PCB Trace Routing

The stack-up parameters for the reference board are shown in Table 4-2.

**Table 4-2 PCB Board Stack-up Parameters**

Layer	Layer Description	Copper Weight (oz)	Target Impedance ( $\pm 10\%$ )
1	Signal	0.5	50
2	GND	1	N/A
3	Power	1	N/A
4	Signal	0.5	50

## 4.6 Recommended Layout

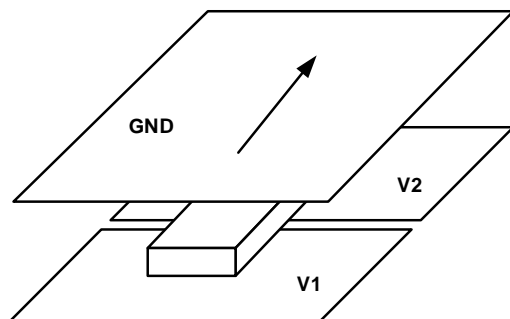
Solid ground planes are recommended. However, special care must be taken when routing VAA and VSS pins.

The following general tips describe what must be considered when determining your stack-up and board routing. These tips are not meant to substitute for consulting with a signal-integrity expert or doing your own simulations.

**Note:** Specific numbers or rules-of-thumb are not used here because they might not be applicable in every situation.

- Do not split ground planes.  
Keep good spacing between possible sensitive analog circuitry on your board and the digital signals to sufficiently isolate noise. A solid ground plane is necessary to provide a good return path for routing layers. Try to provide at least one ground plane adjacent to all routing layers (see Figure 4-3).
- Keep trace layers as close as possible to the adjacent ground or power planes.  
This helps minimize crosstalk and improve noise control on the planes.

**Figure 4-3 Trace Has At Least One Solid Plane For Return Path**



- When routing adjacent to only a power plane, do not cross splits.  
Route traces only over the power plane that supplies both the driver and the load. Otherwise, provide a decoupling capacitor near the trace at the end that is not supplied by the adjacent power plane.
- Critical signals must avoid running parallel and close to or directly over a gap.  
This would change the impedance of the trace.
- Separate analog powers onto opposing planes.  
This helps minimize the coupling area that an analog plane has with an adjacent digital plane.
- For dual strip-line routing, traces must only cross at 90 degrees.  
Avoid more than two routing layers in a row to minimize tandem crosstalk and to better control impedance.
- Planes must be evenly distributed in order to minimize warping.
- Calculating or modeling impedance must be made prior to routing.  
This helps ensure that a reasonable trace thickness is used and that the desired board thickness is available. Consult with your board fabricator for accurate impedance.



- Allow good separation between fast signals to avoid crosstalk. Crosstalk increases as the parallel traces get longer.
- When packages become smaller, route traces over a split power plane  
Smaller packages force vias to become smaller, thereby reducing board thickness and layer counts, which might create the need to route traces over a split power plane. Some alternatives to provide return path for these signals are listed below.

Caution must be used when applying these techniques. Digital traces must not cross over analog planes, and vice-versa. All of these rules must be followed closely to prevent noise contamination problems that might arise due to routing over the wrong plane.

By tightly controlling the return path, control noise on the power and ground planes can be controlled.

- Place a ground layer close enough to the split power plane in order to couple enough to provide buried capacitance, such as SIG-PWR-GND (see Figure 4-4). Return signals that encounter splits in this situation simply jumps to the ground plane, over the split, and back to the other power plane. Buried capacitance provides the benefit of adding low inductance decoupling to your board. Your fabricator may charge for a special license fee and special materials. To determine the amount of capacitance your planes provide, use the following equation:

$$C = 1.249 \cdot 10^{-13} \cdot E_r \cdot L \cdot W / H$$

Where  $E_r$  is the dielectric coefficient,  $L \cdot W$  represents the area of copper, and  $H$  is the separation between planes.

- Provide return-path capacitors that connect to both power planes and jumps the split. Place them close to the traces so that there is one capacitor for every four or five traces. The capacitors would then provide the return path (see Figure 4-5).
- Allow only static or slow signals on layers where they are adjacent to split planes.

Figure 4-4 shows the ground layer close to the split power plane.

**Figure 4-4 Close Power and Ground Planes Provide Coupling For Good Return Path**

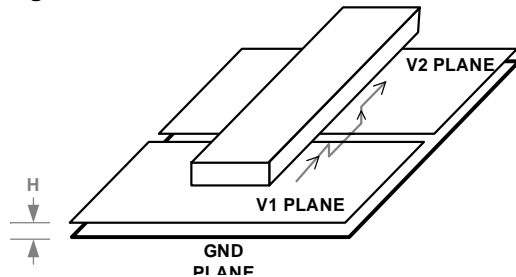
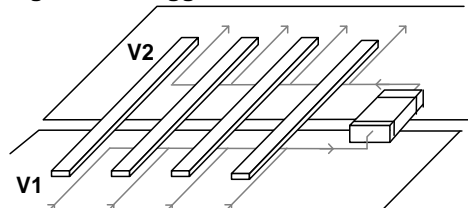


Figure 4-5 shows the thermal ground plane in relation to the return-path capacitor.

**Figure 4-5 Suggested Thermal Ground Plane On Opposite Side of Chip**





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# 5 ELECTRICAL SPECIFICATIONS

This chapter contains the following sections:

- [Absolute Maximum Ratings](#)
- [Recommended Operating Conditions](#)
- [Power Requirements](#)
- [Voltage Regulator Requirements](#)
- [DC Electrical Characteristics](#)
- [Thermal Data](#)

## 5.1 Absolute Maximum Ratings

Table 5-1 defines the absolute maximum ratings for the 88SE9171.

**Table 5-1 Absolute Maximum Ratings\***

Parameter	Symbol	Minimum	Typical	Maximum	Units
Absolute Analog Power for PCIe PHY	AVDD <sub>abs</sub>	-0.5	N/A	1.98	V
Absolute Analog Power for Crystal Oscillator and PLL	VAA1 <sub>abs</sub>	-0.5	N/A	1.98	V
Absolute Analog Power for SATA PHY	VAA2 <sub>abs</sub>	-0.5	N/A	1.98	V
Absolute Digital Core Power	VDD <sub>abs</sub>	-0.5	N/A	1.21	V
Absolute Digital I/O Power	VDDIO <sub>abs</sub>	-0.5	N/A	3.63	V
Alternate Digital I/O Power (1.8V)	VDDIO <sub>abs</sub>	-0.5	N/A	1.98	V

\* Estimated values are provided until characterization is complete.

## 5.2 Recommended Operating Conditions

Table 5-2 defines the recommended operating conditions for the 88SE9171.

**Table 5-2 Recommended Operating Conditions\***

Parameter	Symbol	Minimum	Typical	Maximum	Units
Analog Power for PCIe PHY	AVDD <sub>op</sub>	1.71	1.8	1.98	V
Analog Power for Crystal Oscillator and PLL	VAA1 <sub>op</sub>	1.71	1.8	1.98	V
Analog Power for SATA PHY	VAA2 <sub>op</sub>	1.71	1.8	1.98	V
Digital Core Power	VDD <sub>op</sub>	0.95	1.0	1.21	V
Digital I/O Power (3.3V)	VDDIO <sub>op</sub>	3.135	3.3	3.63	V
Digital I/O Power (1.8V)	VDDIO <sub>op</sub>	1.71	1.8	1.98	V
Internal Bias Reference	ISET <sub>op</sub>	5.98	6.04	6.10	KΩ
Ambient Operating Temperature, Advanced Commercial	N/A	0	N/A	85	°C
Ambient Operating Temperature, Industrial†	N/A	-40	N/A	85	°C
Junction Operating Temperature, Advanced Commercial	N/A	0	N/A	125	°C
Junction Operating Temperature, Industrial†	N/A	-20	N/A	125	°C

\* Estimated values are provided until characterization is complete.

† Engineering samples only. Estimated value provided until characterization is complete. Marvell does not have automotive or military qualification for industrial temperature versions of 88SE9171.

## 5.3 Power Requirements

Table 5-3 defines the power requirements for the 88SE9171.

**Table 5-3 Power Requirements\***

Parameter	Symbol	Maximum	Units
Analog Power for PCIe PHY Transmitter	$I_{AVDD}$	55	mA
Analog Power for Crystal Oscillator and PLL	$I_{VAA1}$	10	mA
Analog Power for SATA PHY	$I_{VAA2}$	55	mA
Digital Core Power	$I_{VDD}$ (300MHz SYSCLK)	600	mA
	$I_{VDD}$ (200MHz SYSCLK)	360	mA
Digital I/O Power (3.3V)†	$I_{VDDIO}$	50	mA

\* Estimated values are provided until characterization is complete.

† The digital I/O power supply can be either 3.3V or 1.8V.

## 5.4 Voltage Regulator Requirements

Table 5-4 defines the requirements for the external Bipolar Junction Transistor (BJT) used with the regulator core.

**Table 5-4 External BJT Requirements\***

Parameter	Symbol	Minimum	Typical	Maximum	Units
DC Current Gain of the BJT	$h_{FE}$	200	N/A	N/A	mA/mA
Collector-Emitter Saturation Voltage	$V_{CEsat}$	N/A	N/A	-200	mV
Power Dissipation of the BJT	P	N/A	N/A	500	mW
Equivalent series resistance of the capacitor	ESR	20	N/A	50	mΩ
Decoupling capacitor (ceramic)	C	10	N/A	N/A	μF

\* Estimated values are provided until characterization is complete.

## 5.5 DC Electrical Characteristics

Table 5-5 defines the DC electrical characteristics for the 88SE9171.

**Table 5-5 DC Electrical Characteristics\***

Parameter	Symbol	Test Condition	Minimum	Typical	Maximum	Units
Input Low Level Voltage	$V_{IL}$	N/A	-0.4	N/A	$0.25 \times V_{DDIO}$	V
Input High Level Voltage	$V_{IH}$	N/A	$0.8 \times V_{DDIO}$	N/A	5.5	V
Output Low Level Current	$I_{OL}$	$V_{PAD} = 0.4V$	5	N/A	N/A	mA
Output High Level Current	$I_{OH}$	$V_{PAD} = V_{DDIO} - 0.4V$	5	N/A	N/A	mA
Pull Up Strength	$I_{PU}$	$V_{PAD} = 0.5 \times V_{DDIO}$	10	N/A	N/A	$\mu A$
Pull Down Strength	$I_{PD}$	$V_{PAD} = 0.5 \times V_{DDIO}$	10	N/A	N/A	$\mu A$
Input Leakage Current	$I_{LK}$	$0 < V_{PAD} < V_{DDIO}$	N/A	N/A	10	$\mu A$
Input Capacitance	$C_{IN}$	$0 < V_{PAD} < 5.5V$	N/A	N/A	5	pF

\* Estimated values are provided until characterization is complete.



## 5.6 Thermal Data

It is recommended to read the application note *AN-63 Thermal Management for Selected Marvell® Products* (Document Number MV-S300281-00) and the *ThetaJC, ThetaJA, and Temperature Calculations White Paper*, available from Marvell, before designing a system. These documents describe the basic understanding of thermal management of integrated circuits (ICs) and guidelines to ensure optimal operating conditions for Marvell products.

Table 5-6 provides the estimated thermal data for the 88SE9171. Actual values may vary depending on the PCB board design and the size of PCB.

Table 5-6 shows the values for the package thermal parameters for the -lead Quad Flat Non-Lead package (QFN) mounted on a four-layer PCB.

**Table 5-6 Package Thermal Data**

Parameter	Definition	Airflow Value			
		0 m/s	1 m/s	2 m/s	3 m/s
$\theta_{JA}$	Thermal resistance: junction to ambient	29.9 C/W	26.6 C/W	25.5 C/W	24.8 C/W
$\Psi_{JT}$	Thermal characterization parameter: junction to top center	0.63 C/W	N/A	N/A	N/A



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