Marvell. Moving Forward Faster

PRODUCT OVERVIEW

The Marvell® 88W8686 is a low-cost, low-power highly-integrated IEEE 802.11a/g/b MAC/Baseband/RF WLAN system-on-chip (SoC), designed to support IEEE 802.11a or 802.11g payload data rates of 6, 9, 12, 18, 24, 36, 48, and 54 Mbps, as well as 802.11b data rates of 1, 2, 5.5, and 11 Mbps.

The device provides the combined functions of the IEEE Standard 802.11/802.11b Direct Sequence Spread Spectrum (DSSS), 802.11a/g Orthogonal Frequency Division Multiplexing (OFDM) baseband modulation, Medium Access Controller (MAC), CPU, memory, host interfaces, and direct conversion WLAN RF radio on a single integrated chip.

The core functional units of the 88W8686 are connected with a high throughput interconnect system, as shown in Figure 1.

The 88W8686 is equipped with a fully integrated RF to baseband transceiver that operates in both the 2.4 GHz ISM radio band for 802.11g/b WLAN applications and 5 GHz UNII radio band for 802.11a WLAN applications. It contains all the circuitry to support both transmit and receive operations.

The transceiver architecture includes a Marvell second-generation radio, designed specifically for co-existence with cellular phones. Cellular band transmit spurious tone, noise, and receive jammer considerations have been designed for into the device.

Due to very low spectral emissions in the cellular phone receive band, the device does not interfere with cellular phone reception and is immune to high power cellular phone transmission signals.

For optimum performance, the gain adjustment of the integrated LNA and AGC on the receive path is seamlessly controlled by baseband functions. The entire receive path has over 90 dB of voltage gain and gain control range.

Integrated transmitters up-convert the quadrature baseband signal, and then deliver the RF signals to external power amplifiers for 2.4 GHz and 5 GHz radio band transmission.

Local oscillator frequencies are generated by a fully integrated programmable frequency synthesizer without any external components. The loop bandwidth is optimized for phase noise and dynamic performance and quadrature signals are generated on-chip.

For security, the 88W8686 supports the IEEE 802.11i security standard through implementation of the Advanced Encryption Standard (AES)/Counter Mode CBC-MAC Protocol (CCMP), and Wired Equivalent Privacy (WEP) with Temporal Key Integrity Protocol (TKIP) security mechanisms.

For video, voice, and multimedia applications, the 88W8686 supports 802.11e Quality of Service (QoS). A Bluetooth coexistence interface is also supported.

The 88W8686 supports both a generic SPI (G-SPI) and SDIO host interface and is available in QFN and flip chip packages.

Figure 1:   Top Block Diagram[1]
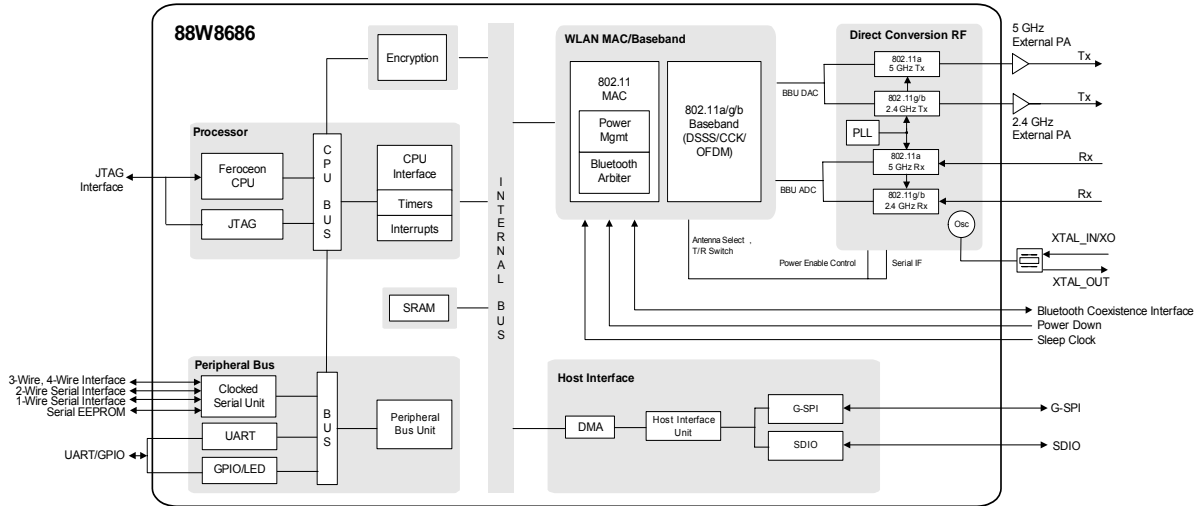
1. Antenna used as an option to enhance performance.

Reference Designs

Marvell reference designs are highly-integrated low cost, production quality designs that provide a quick time-to-market solution for customers developing single chip IEEE 802.11a/g/b WLAN solutions.

For further information, contact Marvell representatives.

Applications

- Cellular handsets
- Consumer electronic devices that require low power consumption

General Features

- Ultra low-power dissipation
- Single-chip integration of 802.11a/g/b wireless RF and baseband, MAC, CPU, memory, and host interfaces
- Integrates all RF to baseband transmit and receive operations, with support for external PAs
- Fully integrated frequency synthesizers with optimized phase noise performance for OFDM applications
- Integrated direct conversion WLAN RF radio
- Supports 19.2, 20, 24, 26, 38.4, and 40 MHz oscillator clock sources
- Software backward compatible with 88W8385 and 88W8015 devices

Payload Data Rates

- IEEE 802.11 data rates of 1 and 2 Mbps
- IEEE 802.11b data rates of 5.5 and 11 Mbps
- IEEE 802.11a/g data rates of 6, 9, 12, 18, 24, 36, 48, and 54 Mbps for multimedia content transmission

Packaging

- 68-pin QFN package
- 280 μm pitch flip chip
- 500 μm pitch flip chip[1]

---

1. 500 μm flip chip option supports 802.11g/b only.

Processor

CPU

- Integrated Marvell Feroceon® CPU (ARMv5TE-compliant)
- Offloads wireless protocol stack processing from host CPU
- 128 MHz operating frequency

DMA

- Independent 2-channel Direct Memory Access (DMA)

Networking Functions

WLAN MAC

- Ad-Hoc and Infrastructure modes
- Request-to-Send (RTS)/Clear-to-Send (CTS) for operation under Distributed Coordination Function (DCF)
- Hardware filtering of 64 multicast and 96 unicast addresses and additional firmware options
- On-chip Tx and Rx FIFOs for maximum throughput
- Open System and Shared Key Authentication services
- Managed information base counters
- 802.11e Quality of Service (QoS)
- 802.11h DFS statistics processing
- Power management
- External sleep clock control
- Transmit rate adaptation
- Long and short preamble generation on a frame-by-frame basis for 802.11b frames

WLAN Baseband

- DSSS and OFDM modulation
- Advanced Equalizer for Complementary Code Keying (CCK) modes
- Differential Binary Phase Shift Keying (DBPSK), Differential Quadrature Phase Shift Keying (DQPSK), and CCK modulation modes
- 16-QAM and 64-QAM modulation
- On-chip A/D and D/A converters for Inphase/Quadrature (I/Q) channels
- Targeted for multi-path delay spreads up to 680 ns in 11 Mbps mode and 150 ns in 54 Mbps mode
- Supports 802.11h (DFS and TPC) statistics gathering
- Supports 802.11j channels (Japan)

WLAN RF

Rx Path

- On-chip gain selectable LNA with optimized noise figure and power consumption
- Highly integrated architecture eliminates need for external SAW filter
- High dynamic range AGC function in receive mode
- Immune to high power cellular phone transmission signals

Tx Path

- Image-reject transmitter to reduce external RF filter count for 2.4 GHz radio transmit
- Supports external PA with power control for both 2.4 GHz and 5 GHz operation
- Supports closed and open loop power control in increments of 0.5 dB
- Very low spectral emissions in the cellular phone receive band

WLAN Encryption

- WEP 64- and 128-bit encryption with hardware TKIP processing
- WPA (Wi-Fi Protected Access)
- CCMP hardware implementation as part of 802.11i security standard

Networking Coexistence

- Supports Marvell 2-Wire Bluetooth Coexistence Arbitration (2WBCA) scheme
- Supports Marvell 3-Wire Bluetooth Coexistence Arbitration (3WBCA) scheme
- Supports Marvell 4-Wire Bluetooth Coexistence Arbitration (4WBCA) scheme

Host Interfaces

- G-SPI device interface
- SDIO device interface

Memory

Frame Buffer

- Internal SRAM for Tx frame queues and Rx data buffers

Boot ROM

- Boot ROM

Peripheral Bus Interfaces

- Clocked Serial Unit
  - 3-Wire, 4-Wire (3W4W) Interface
  - 2-Wire Serial Interface (TWSI)
  - 1-Wire Serial Interface
  - SPI Serial (EEPROM)
- Universal Asynchronous Receiver/Transmitter (UART)
- General Purpose Input Output (GPIO)
- Flexible GPIO interface with Light Emitting Diode (LED) driver to indicate Tx/Rx activities

Test

- On-chip diagnostic registers

THIS PAGE INTENTIONALLY LEFT BLANK

For further information about Marvell® products, see the Marvell website: http://www.marvell.com