

# S1 EP29 - 3nm Advancing Cloud-Optimized Silicon Solutions

Wednesday, December 7, 2022 · 7:24

Join Hugh Durdan, Vice President of Marketing in the ASIC Business Unit and podcast host Chris Banuelos on this week's episode, discussing all things 3nm. Learn more about how 3nm is advancing cloud-optimized silicon solutions, the driver behind the evolution, more on Marvell's recent announcement on the 3nm silicon platform and much more. Read the press release: <https://bit.ly/3P68F24>

## Speakers

### **Hugh Durdan**

Vice President of Marketing in the ASIC Business Unit

## Host

### **Christopher Banuelos**

Senior Manager of Global Social Media Marketing

#### **C Christopher Banuelos 00:04**

Welcome to the Marvell Essential Technology Podcast. I'm your host, Chris Banuelos. On today's episode, join in on a conversation between me and Hugh Durdan, Vice President of Marketing in the ASIC business unit. And today, we're discussing all things three nanometer (3nm). Learn more about how 3nm is advancing cloud optimized silicon solutions. What's driving the evolution to 3nm Marvell's recent announcement on the 3nm silicon platform, industry partnerships, use cases, and much more. To stay up to date on future episodes, please be sure to subscribe to the Marvell Essential Technology Podcast. Hugh, thank you so much for being on today's episode is great to have you. One of my first questions for you is how is 3nm advancing cloud optimized silicon solutions? And what is driving the evolution to 3nm?

#### **H Hugh Durdan 01:00**

Yeah, good question, Chris. So there's been a lot of debate in the press about Moore's law, and is Moore's Law dead or not? And I kind of in some ways, you that is almost a religious kind of argument, where there, there is no right answer. There's lots of opinions. But from our customers perspective, moving to the most advanced process, nodes still provide significant benefits to their applications. And those benefits come in 3 different dimensions. It comes through the power that the device consumes, the performance they can achieve, and the density and what I mean by density is, how much can they fit on a chip, a number of the applications that we service are very high end applications. And they're actually limited by how much content you can fit on the largest die that's possible to manufacture. And so with each successive process node, as a process shrinks, they can fit more on that single die and get more capability. And these are the types of things that make 3nm very attracted to them. And so we were the first that 5nm, we've had tremendous success there with a wide range of our products. And now it's time to move on to the next node, which is 3nm.

**C Christopher Banuelos 02:24**

Marvell recently announced its 3nm silicon platform. Can you tell me more about the platform? And what, what is the impact on the industry?

**H Hugh Durdan 02:33**

So the platform is comprised of a number of different elements. One of the key things that's part of the platform is the intellectual property. So my intellectual property, what I mean is the, mainly what's called Hard IP. So those are the physical interfaces that go on to a die that support things like PCI Express (PCIe), or UCI, ie the new day to day interconnect or high speed SERDES for Ethernet in applications like that. And so these IP elements are building blocks that go into a wide range of Marvell's products that goes into our ASICs that we do for customers, it goes into our switch chips, the PHYs that we do for the optical space goes into our storage products. And so it's a portfolio of IP, which is primarily targeted to cloud applications, and again, gets used across the whole product portfolio within Marvell. So the IP is one aspect of it and other aspects is our design methodology. So we have a complete design flow, again, used across all the products that Marvell does, focused on three nanometer. And then the packaging capability is also another key element to that many of the applications that we're servicing are, are moving to either very large complex packages with a single device, or in many cases, those large complex packages have multiple die within the package. And so part of the design methodology and part of the IP is the ability to put those die in a package, connect them all together, make sure that they work together, do the thermal analysis, and so on, to make sure that the product is manufacturable and reliable. And so all those different elements come together to form this design platform that we utilize to leverage both for our standard products and the ASICs that we do in conjunction with our customers.

**C Christopher Banuelos 04:31**

Can you tell me more about Marvell's partnership with TSMC?

**H Hugh Durdan 04:36**

So Marvell has had a long relationship with with TSMC. For many generations, the previous one was at 5nm. And so that whole design platform that I talked about, what was also in placed in 5nm , and now we've moved it to 3 [nm], both with TSMC. And so from a manufacturing point of view, TSMC is a very important part. And, again, our customers demand the latest technology the most advanced in terms of power, performance and density. And TSMC provides that. But another very important aspect of our relationship with TSMC is on the packaging side. So those complex multi chip packages that I talked about, in many cases who are partnering with TSMC. To do that, we also use the TSMC technology called ko OS, which stands for chip on wafer on substrate. And so they're a very important partner, not only for the silicon technology, but also the packaging technology for those large complex packages.

**C Christopher Banuelos 05:39**

What are some of the use cases for 3nm?

**H Hugh Durdan 05:42**

So 3nm has a wide range of use cases across our products, some move to the latest technology sooner than others. But over time, pretty much everything that we do is going to move to 3nm. So the types of applications that move there first are mainly processor related applications, whether it's an ARM processor, like our OCTEON product line, or an artificial intelligence (AI) machine learning (ML) processor that we do for our customers. And the reason why they move there first is that they tend to be very large devices that benefit from the density. So again, they can fit more on the device because the scalability of three nanometer versus five nanometer, they also benefit from the power reduction, and they get a performance improvement. So that's probably the first class of parts that we moving there, other applications will move there very quickly. After that, we are currently looking at devices for things like 5G infrastructure, which are very power sensitive and benefit from the power scalability of three nanometer. And then our optical fibers, both coherent and data center, etcetera, will move to 3nm over time. So it's going to be a very, very important technology for Marvell.

**C Christopher Banelos 06:59**

Hugh, thank you for joining today's episode. I wanted to say thought we had a great conversation. Really appreciate you being on today's podcast.

**H Hugh Durdan 07:06**

Thank you, Chris. It was great to be here. I appreciate the opportunity.

**C Christopher Banelos 07:11**

Thank you for listening to the Marvell Essential Technology Podcast. As always, please feel free to visit our website to learn more, and we'll see you on the next episode.



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