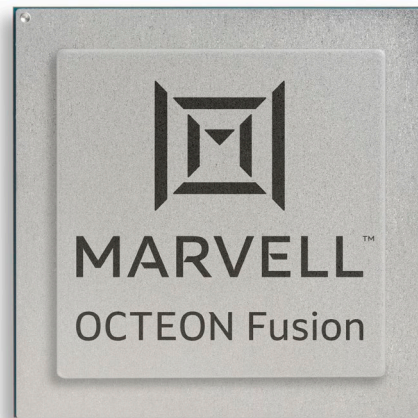# OCTEON TX2
Infrastructure Processor Family

Announcement of Next Generation Infrastructure Processors

OCTEON® TX2
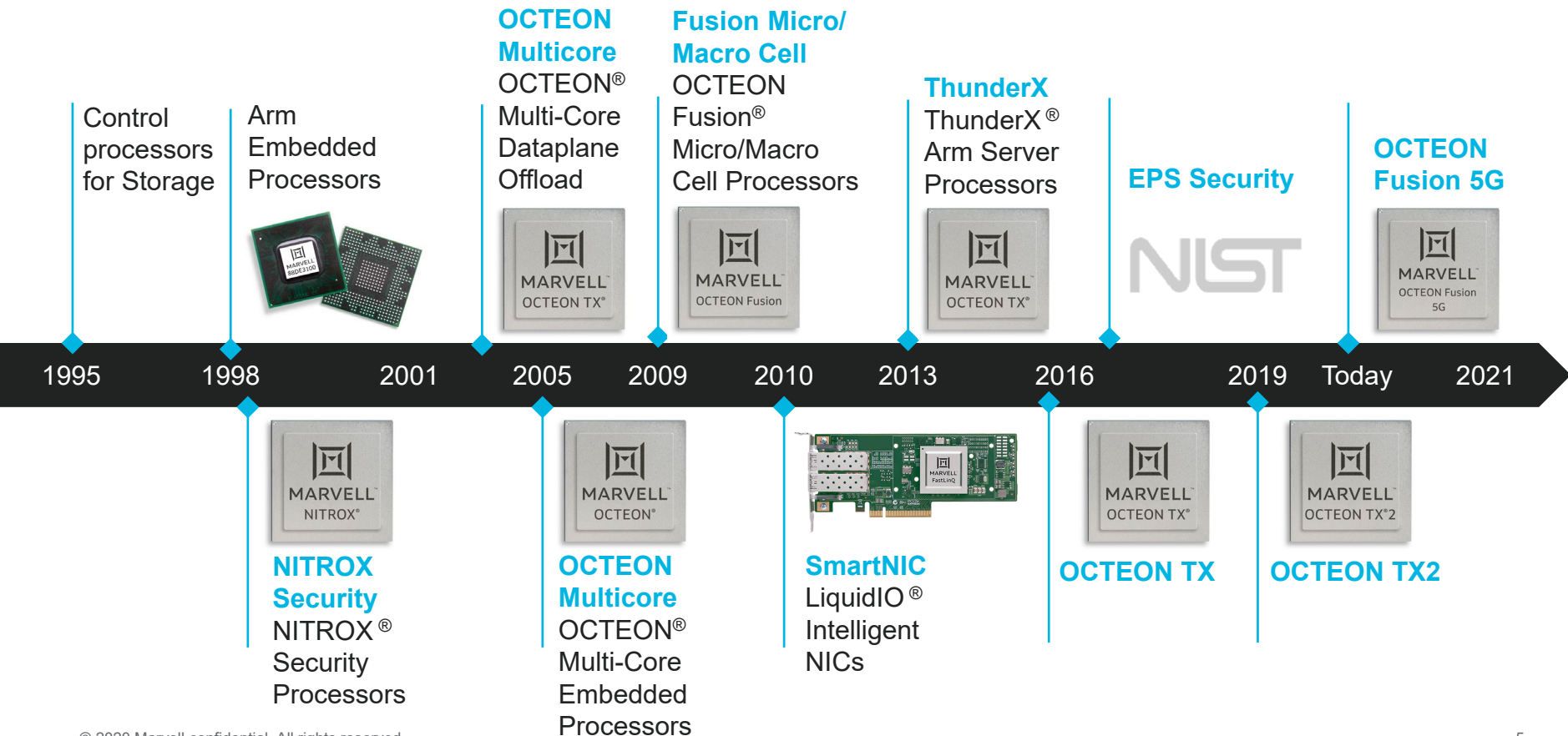
OCTEON Fusion®

OCTEON TX2 Announcement

- Industry-leading data path performance up to 200Gbps for networking and security applications

- Up to 5 100G MACs integrated in the OCTEON TX2 infrastructure processor leading to significant TCO advantage

- OCTEON TX2 Infrastructure Processor family combines 4 to 36 Armv8-based architecture cores with configurable, programmable hardware accelerator blocks

- Fully virtualized SoC architecture Second line of text example
  – Cores, I/O and all data-plane acceleration engines are fully virtualized

OCTEON TX2 Announcement

- Target Markets:
  - Enterprise Networking / security
  - 5G wireless infrastructure
  - Service provider / multi-access Edge compute
  - Cloud / Data Center

Highest Performance Infrastructure Processor Family

A Long History of Compute Innovation

OCTEON Multicore
OCTEON®
Multi-Core
Dataplane
Offload

Fusion Micro/ Macro Cell
OCTEON
Fusion®
Micro/Macro
Cell Processors

ThunderX
ThunderX®
Arm Server
Processors

OCTEON Fusion 5G

Control processors for Storage

Arm Embedded Processors

EPS Security

1995   1998   2001   2005   2009   2010   2013   2016   2019   Today   2021

NITROX Security
NITROX®
Security
Processors

OCTEON Multicore
OCTEON®
Multi-Core
Embedded
Processors

SmartNIC
LiquidIO®
Intelligent
NICs

OCTEON TX

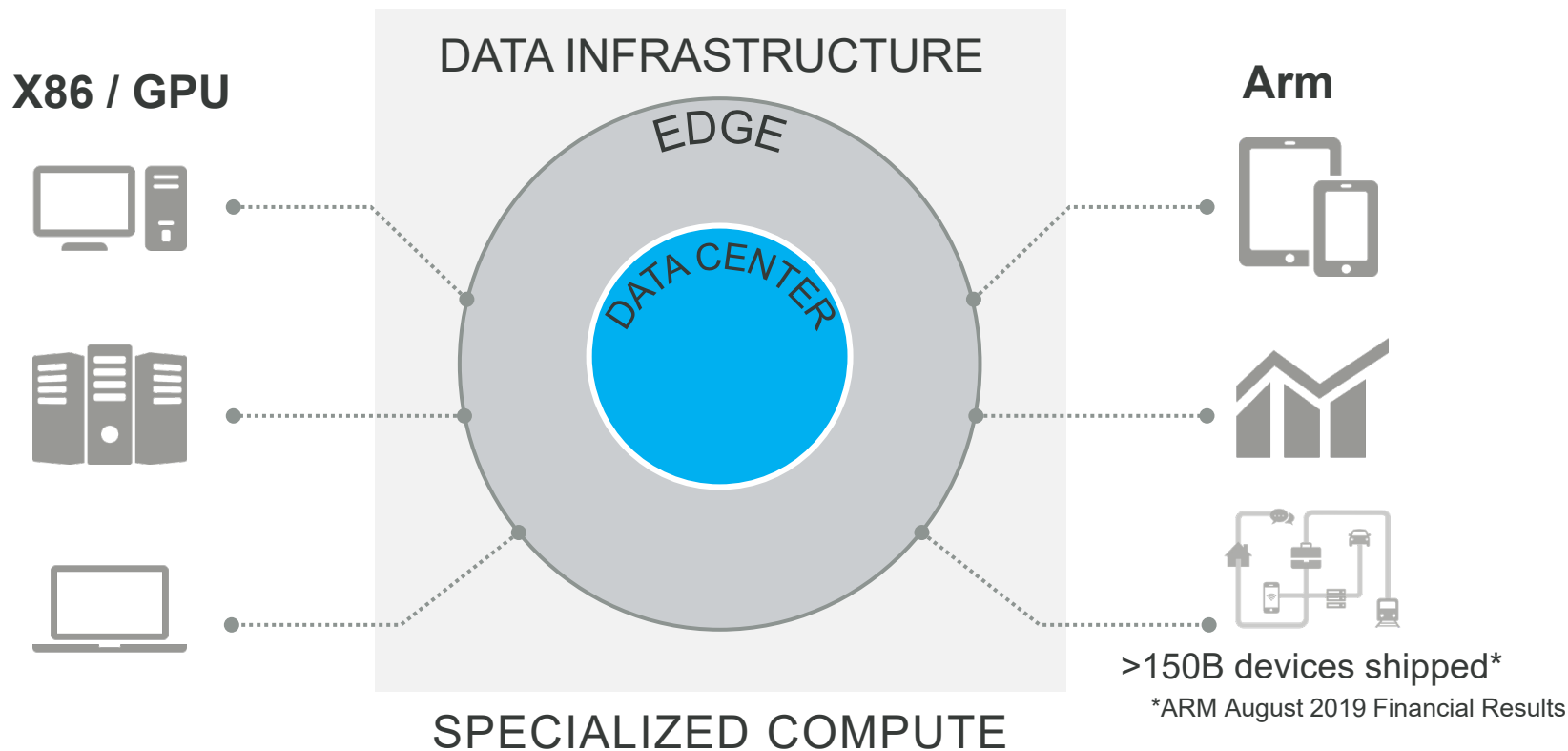**OCTEON TX2**

5

Announcement of Next Generation Infrastructure Processors

- This is the standard bullet slide

- Keep bullet points brief

- Use line spacing to clearly separate each point
  - Second line of text example

New Horizons – New Solutions

X86 / GPU

DATA INFRASTRUCTURE

EDGE

DATA CENTER

Arm

SPECIALIZED COMPUTE

>150B devices shipped*

*ARM August 2019 Financial Results

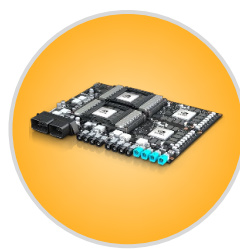# From the Core to the Edge – Technology Leadership

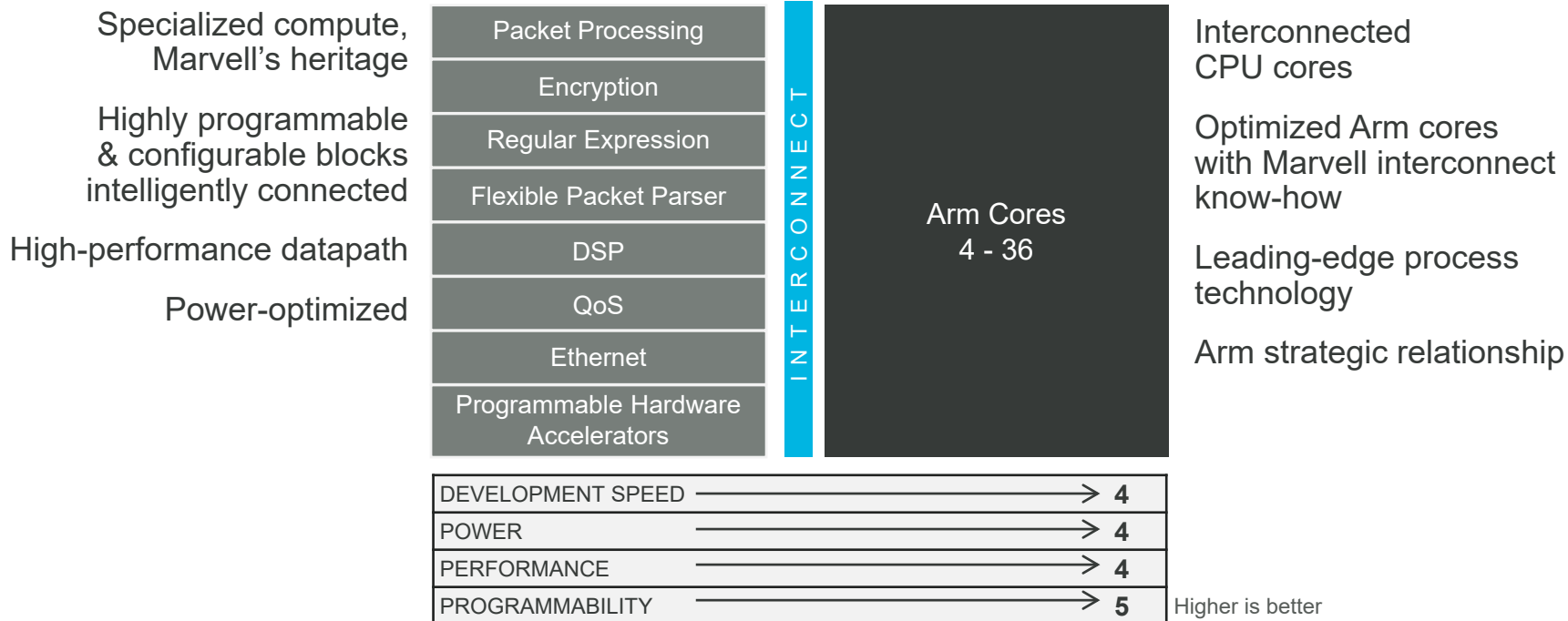| DATA CENTER | CARRIER | ENTERPRISE | EDGE | THINGS |

End-to-end SECURITY

Packet Processing

Compute

Signal Processing

What is a Marvell Infrastructure Processor?

MARVELL™

Specialized compute, Marvell's heritage

Highly programmable & configurable blocks intelligently connected

High-performance datapath

Power-optimized

| Packet Processing |
| Encryption |
| Regular Expression |
| Flexible Packet Parser |
| DSP |
| QoS |
| Ethernet |
| Programmable Hardware Accelerators |

INTERCONNECT

Arm Cores
4 - 36

Interconnected CPU cores

Optimized Arm cores with Marvell interconnect know-how

Leading-edge process technology

Arm strategic relationship

DEVELOPMENT SPEED	→ 4
POWER	→ 4
PERFORMANCE	→ 4
PROGRAMMABILITY	→ 5

Higher is better

Infrastructure Processor: Leading Compute and Data Plane

High-end firewall
Crypto offload

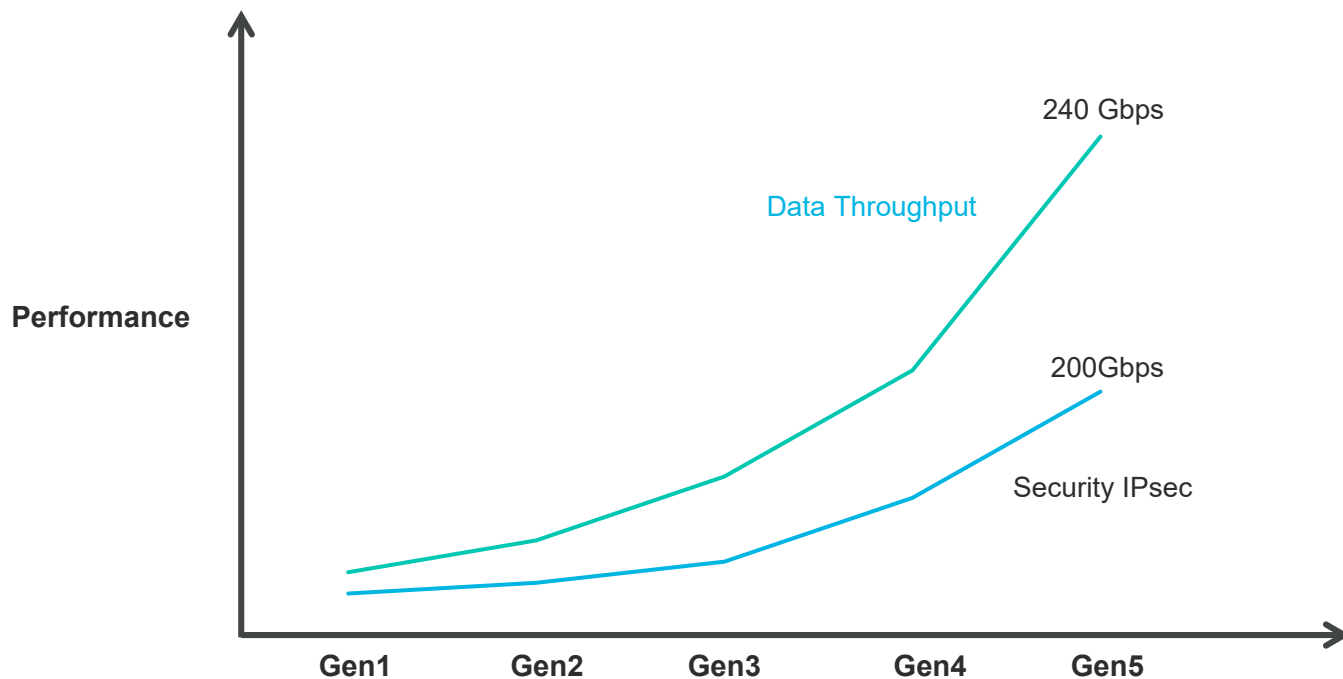**Routers and switches**
Control / data, crypto offload

Macro / micro BTS
Transport layer and crypto

MARVELL CN98xx

MARVELL CN96xx

SMB firewall /
Security gateway
Control plane processor

MARVELL CN9130

MARVELL CN96xx

MARVELL CN92xx

MARVELL CN9130

MARVELL CN92xx

MARVELL CN96xx

Marvell Infrastructure Processor Timeline

Performance

Data Throughput

240 Gbps

200Gbps

Security IPsec

Gen1   Gen2   Gen3   Gen4   Gen5

OCTEON TX2 Infrastructure Processor: CN98/96xx
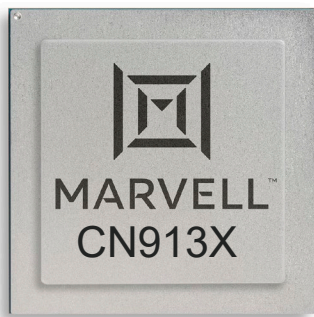
|			
MARVELL™ CN913X	**MARVELL™** CN92XX	**MARVELL™** CN96XX	**MARVELL™** CN98XX
4C A72 20 Gbps NOW	12-18C ARMv8.2 50 Gbps NOW	18-24C ARMv8.2 100 Gbps NOW	24-36C ARMv8.2 200 Gbps Q2'2020

Unified software development environment supporting standard Linux, DPDK, containers & virtualization

OCTEON TX2 Infrastructure Processor: CN98/96xx

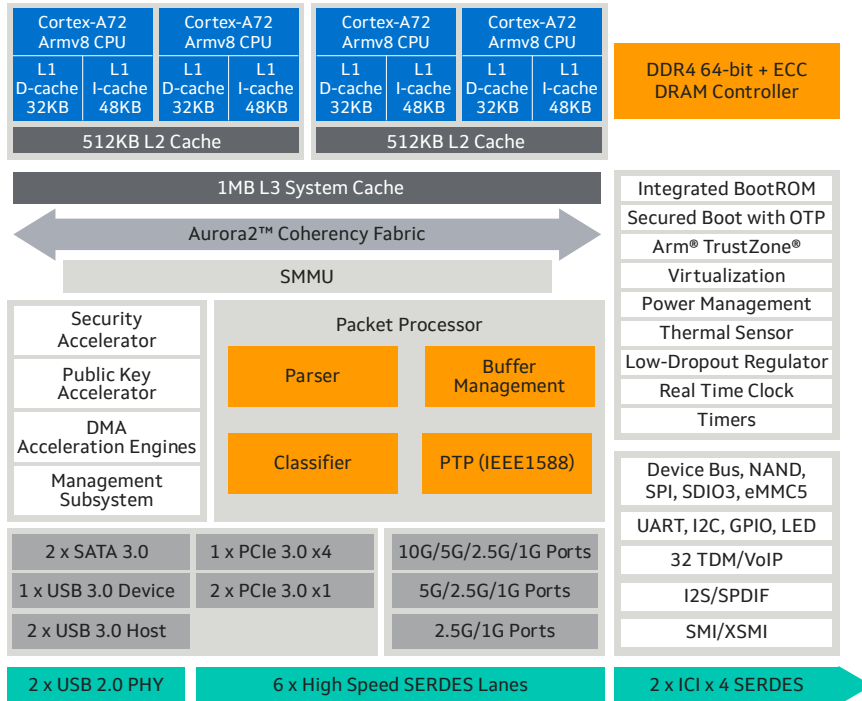Introducing the industry's highest performing Infrastructure Processor family
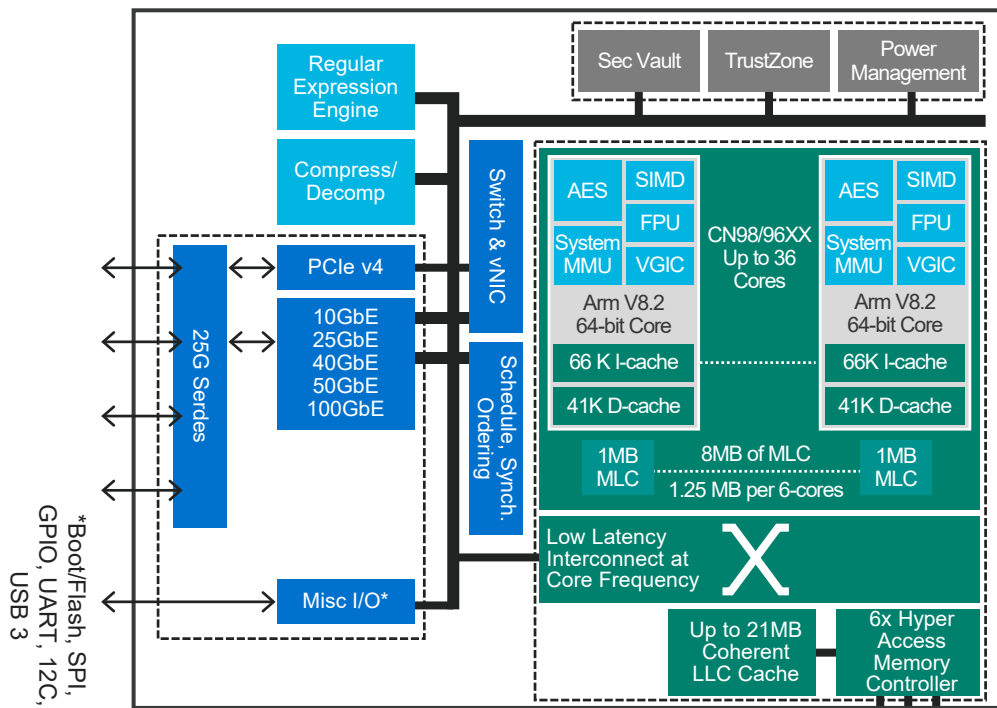
- Highest Compute (SPECINTRate) SOC in its class
- Multi-core scaling w/ low latency interconnect
- Rich I/O
- HW acceleration for packet processing, encryption

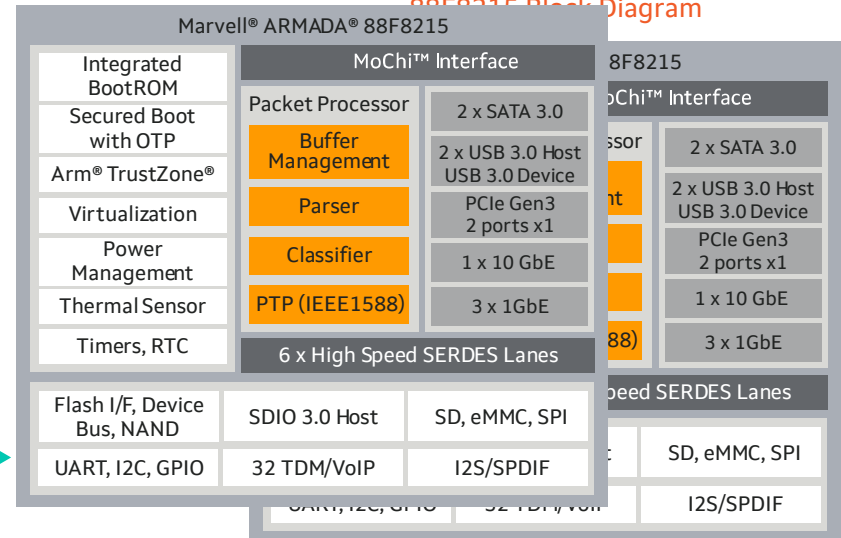# CN9130 – Best Performance/Watt Processor Targeting SOHO/SMB

CN9130 block diagram

Cortex-A72 Armv8 CPU	Cortex-A72 Armv8 CPU	Cortex-A72 Armv8 CPU	Cortex-A72 Armv8 CPU
L1 D-cache 32KB / L1 I-cache 48KB	L1 D-cache 32KB / L1 I-cache 48KB	L1 D-cache 32KB / L1 I-cache 48KB	L1 D-cache 32KB / L1 I-cache 48KB
512KB L2 Cache		512KB L2 Cache	

DDR4 64-bit + ECC DRAM Controller

1MB L3 System Cache

Aurora2™ Coherency Fabric

SMMU

Security Accelerator
Public Key Accelerator
DMA Acceleration Engines
Management Subsystem

Packet Processor
- Parser
- Buffer Management
- Classifier
- PTP (IEEE1588)

Integrated BootROM
Secured Boot with OTP
Arm® TrustZone®
Virtualization
Power Management
Thermal Sensor
Low-Dropout Regulator
Real Time Clock
Timers

Device Bus, NAND, SPI, SDIO3, eMMC5
UART, I2C, GPIO, LED
32 TDM/VoIP
I2S/SPDIF
SMI/XSMI

2 x SATA 3.0	1 x PCIe 3.0 x4	10G/5G/2.5G/1G Ports
1 x USB 3.0 Device	2 x PCIe 3.0 x1	5G/2.5G/1G Ports
2 x USB 3.0 Host		2.5G/1G Ports

2 x USB 2.0 PHY | 6 x High Speed SERDES Lanes | 2 x ICI x 4 SERDES

- CN913X – Up to 4 cores (20 Gbps)
- Supports up to 18 SERDES lanes
- <10W power consumption

88F8215 Block Diagram

Marvell® ARMADA® 88F8215

MoChi™ Interface

Integrated BootROM
Secured Boot with OTP
Arm® TrustZone®
Virtualization
Power Management
Thermal Sensor
Timers, RTC

Packet Processor
- Buffer Management
- Parser
- Classifier
- PTP (IEEE1588)

| 2 x SATA 3.0 |
| 2 x USB 3.0 Host USB 3.0 Device |
| PCIe Gen3 2 ports x1 |
| 1 x 10 GbE |
| 3 x 1GbE |

6 x High Speed SERDES Lanes

| Flash I/F, Device Bus, NAND | SDIO 3.0 Host | SD, eMMC, SPI |
| UART, I2C, GPIO | 32 TDM/VoIP | I2S/SPDIF |

14

OCTEON TX/TX2: Portfolio

Metric	CN913X	CN83XX	CN92XX	CN96XX	CN98XX
Cores	4	8-24	12-18	18-24	30-36
Max Freq	2.2G	2.0G	2.0G	2.4G	2.4G
Cache (MLC, LLC)	2MB	8MB	5MB, 8MB	5MB, 14MB	8MB, 21MB
DDR4	1@2400MTS	2@2100MTS	2@3200MTS	3@3200MTS	6@3200MTS
Ethernet	Up to 3 x10G+6x1/2.5G	12x10G	4x25G, 8x10G	3 x100G/12x25G	5 x100G/20x25G
Max PPS	15Mpps	60Mpps	Up to 50Mpps	Up to 120Mpps	Up to 220Mpps
IP FWDing	Up to 25G	Up to 60G	Up to 80G	120G-140G	200G-240G
IPSEC (Gbps)	Up to 15G	30Gbps	50Gbps	100Gbps	200Gbps
Serdes	Up to 18x 10G	22x 10G	32x 16G/25G	32x 16G/25G	48-56 16G/25G
PCI-e Physical Interface/VF	Up-to 18x v3/8	24 lanes v3/64	24 lanes v4/256	24 lanes v4/256	32 lanes v4/512-1K
Estimated TDP	9W-14W	30W-55W	45W-65W	55W-80W	80W-120W
AVAILABLE	NOW	NOW	NOW	NOW	Q2'2020

Unified Software Development Environment

VPP

OpenSSL

Arm V8 Crypto ISA

DPDK ENGINE

DPDK DATA PLANE DEVELOPMENT KIT

IPSEC

L2/L3

Hyperscan

Standard Linux Apps

SDK

OpenWrt Wireless Freedom

Secure Storage

Linux Kernel

TCP/IP
Routing/Bridging/iptables

IPSEC

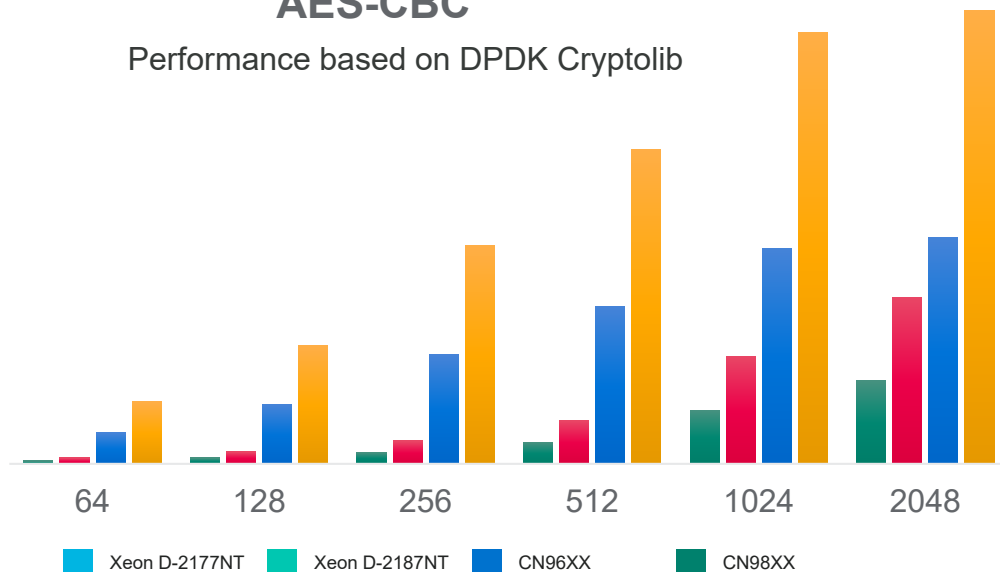BuildRoot Making Embedded Linux Easy

Secure Boot

Boot Loader
U-Boot/UEFI
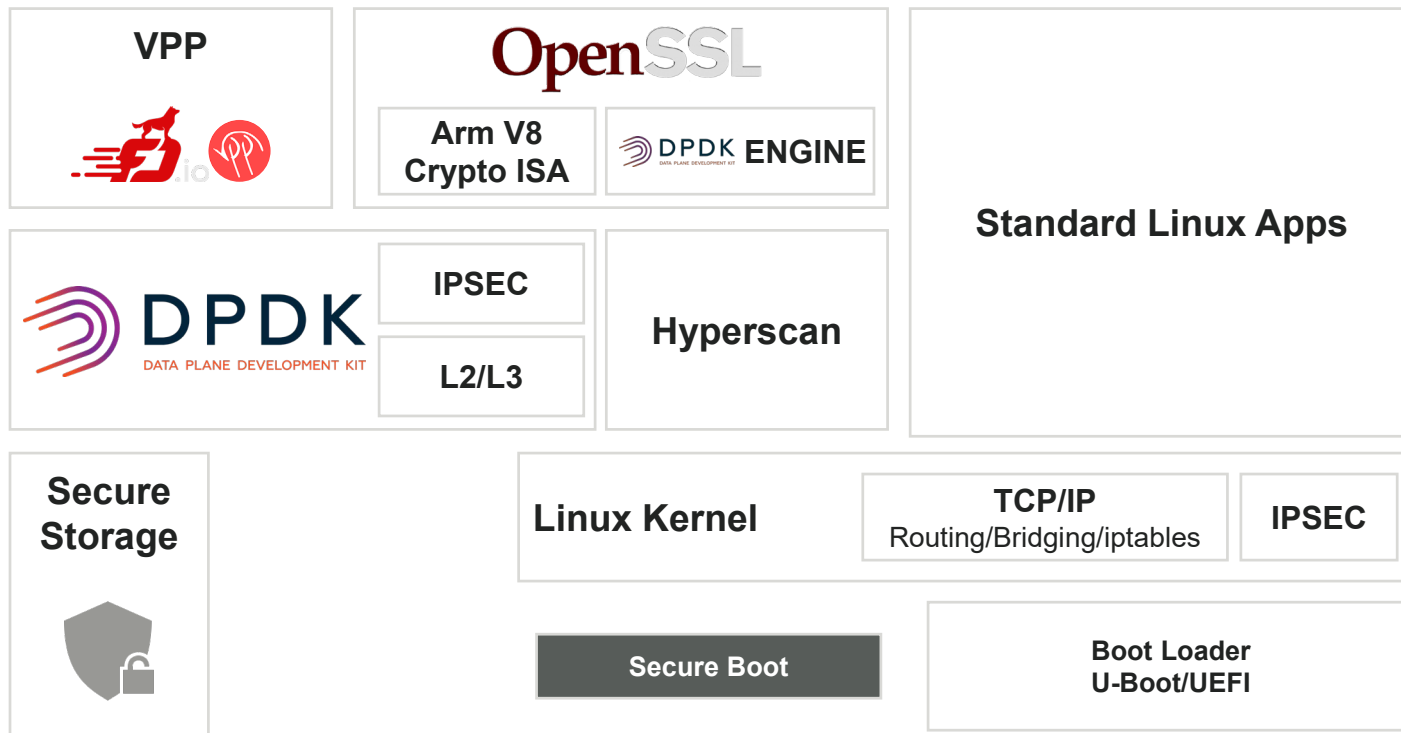
Marvell Security Acceleration Performance Advantage

Infrastructure Processor with Crypto accelerator
Performance vs. software implementation with QAT

AES-CBC

Performance based on DPDK Cryptolib

Legend: Xeon D-2177NT, Xeon D-2187NT, CN96XX, CN98XX
X-axis: 64, 128, 256, 512, 1024, 2048

Crypto Requirement (1KB Packet)	Intel Xeon	Marvell Infrastructure Processor
50G	*128W	50W
100G	**155W	75W
200G	***300W	135W

Packet size

***Marvell Estimate

Proof Point: Security Appliance Example

Intrusion Protection | Firewall | IPSEC

32 Core x86

Marvell
CN98XX

4x10/40G

8x25G

Higher Performance

Intrusion Prevention	12G	50G
Firewall	50G	200G
IPSEC	6G	100G

Proof Point: Network Visibility and Analysis Appliance

CPU with FPGA	Infrastructure Processor

CPU with FPGA side:

Xeon – 2187NT

FPGA

⇅⇅⇅⇅

Ethernet

Power: 235W
Price: 3X+

Infrastructure Processor side:

Marvell
CN96XX: 24 Core

⇅⇅⇅⇅

Ethernet

Power: <75W
Price: 1X

Proof Point: 5G Macro Base Station

OCTEON TX2 Arm V8.2 SoC
5G gNodeB design
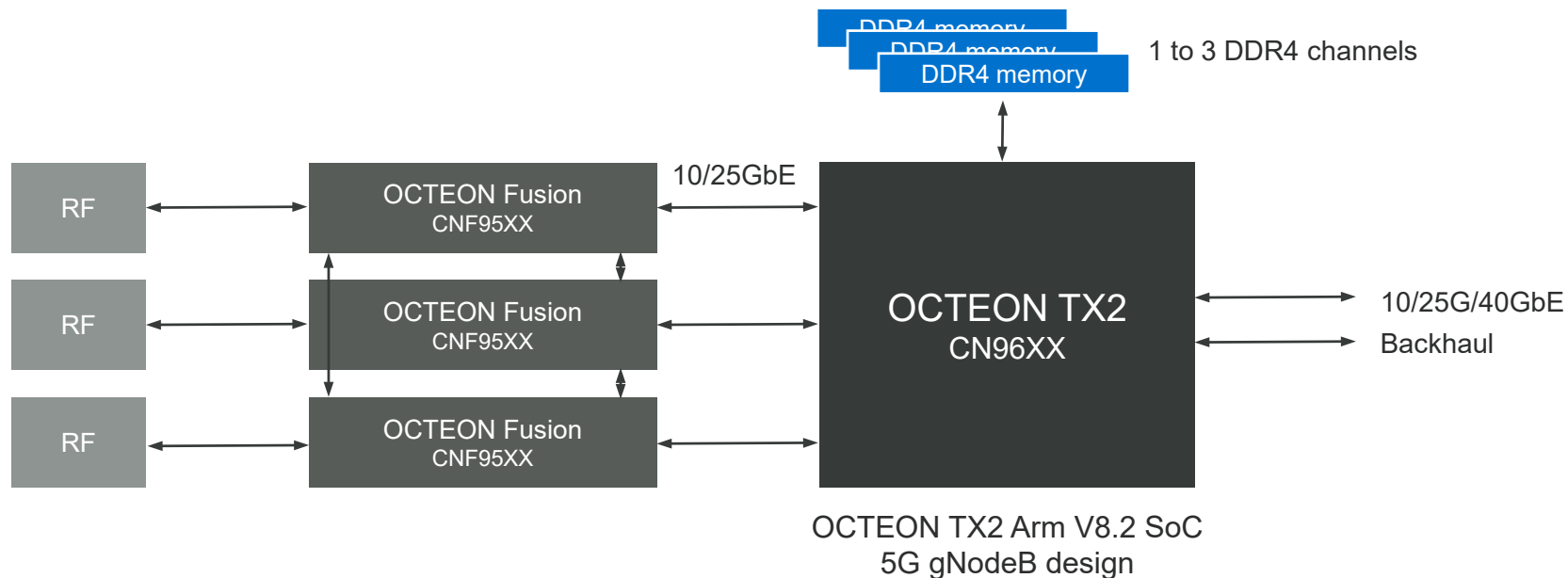
Summary

- Industry-leading data path performance up to 200Gbps for networking and security applications

- Up to 5 100G MACs integrated in the OCTEON TX2 infrastructure processor leading to significant TCO advantage

- OCTEON TX2 Infrastructure Processor family scales 4 to 36 Arm v8-based architecture cores with configurable, programmable hardware accelerator blocks

Highest Performance Infrastructure Processor Family

Traditional Data Infrastructure Compute Options

CPU only

Arm / X86 Compute

DEVELOPMENT SPEED	→ 5
POWER	→ 2
PERFORMANCE	→ 2
PROGRAMMABILITY	→ 5

FPGA

Arm

LUT and Interconnect

DEVELOPMENT SPEED	→ 3
POWER	→ 2
PERFORMANCE	→ 3
PROGRAMMABILITY	→ 5

Custom ASIC

Fixed ASIC Gates

Arm

DEVELOPMENT SPEED	→ 1
POWER	→ 5
PERFORMANCE	→ 5
PROGRAMMABILITY	→ 1

OCTEON TX2 Value Proposition: The Best of Both Worlds

3 I/O bridges (each 1+Tbps) for 200Gbps of Data-plane processing
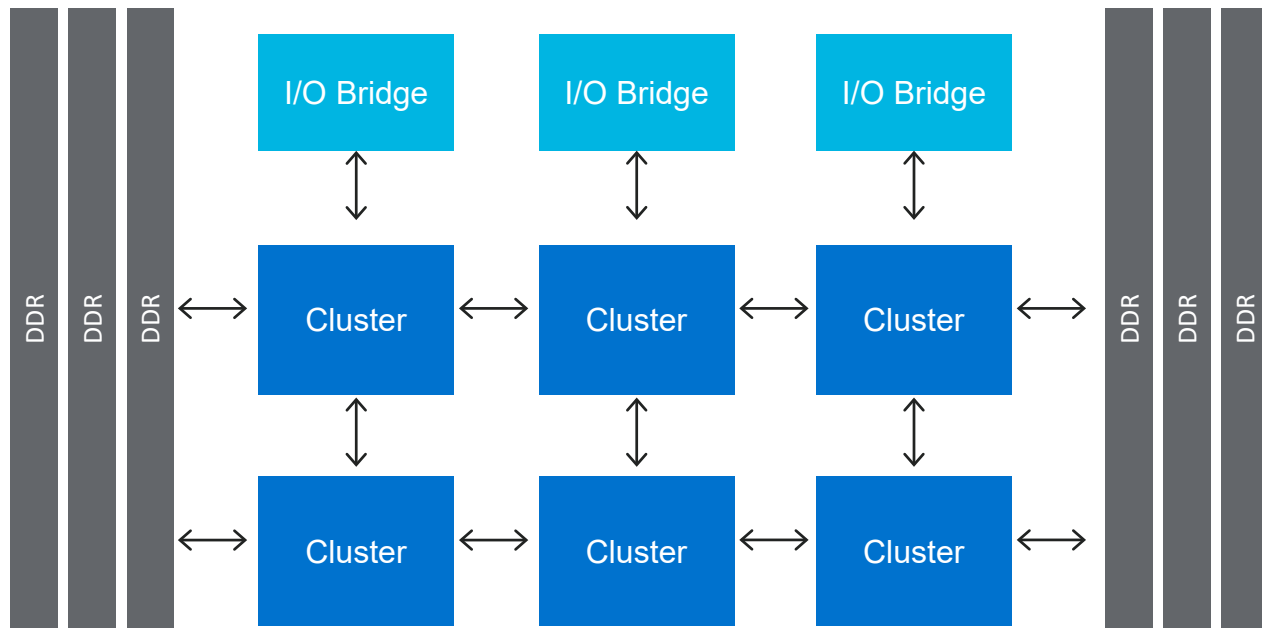
CN98xx architecture

MARVELL™

Essential technology, done right™