OCTEON TX2
Infrastructure Processor Family
Announcement of Next Generation Infrastructure Processors

OCTEON® TX2

OCTEON Fusion®
OCTEON TX2 Announcement

- Industry-leading data path performance up to 200Gbps for networking and security applications
- Up to 5 100G MACs integrated in the OCTEON TX2 infrastructure processor leading to significant TCO advantage
- OCTEON TX2 Infrastructure Processor family combines 4 to 36 Armv8-based architecture cores with configurable, programmable hardware accelerator blocks
- Fully virtualized SoC architecture
  - Cores, I/O and all data-plane acceleration engines are fully virtualized
OCTEON TX2 Announcement

- Target Markets:
  - Enterprise Networking / security
  - 5G wireless infrastructure
  - Service provider / multi-access Edge compute
  - Cloud / Data Center
A Long History of Compute Innovation


- Control processors for Storage
- Arm Embedded Processors
- OCTEON Multicore OCTEON® Multi-Core Data Plane Offload
- Fusion Micro/Macro Cell OCTEON Fusion® Micro/Macro Cell Processors
- ThunderX ThunderX® Arm Server Processors
- EPS Security
- OCTEON Fusion 5G

- NITROX Security
- NITROX® Security Processors
- OCTEON Multicore OCTEON® Multi-Core Embedded Processors
- SmartNIC LiquidIO® Intelligent NICs
- OCTEON TX
- OCTEON TX2
Announcement of Next Generation Infrastructure Processors

- This is the standard bullet slide
- Keep bullet points brief
- Use line spacing to clearly separate each point
  - Second line of text example
New Horizons – New Solutions

DATA INFRASTRUCTURE

EDGE

SPECIALIZED COMPUTE

X86 / GPU

Arm

>150B devices shipped*

*ARM August 2019 Financial Results
From the Core to the Edge – Technology Leadership

<table>
<thead>
<tr>
<th>DATA CENTER</th>
<th>CARRIER</th>
<th>ENTERPRISE</th>
<th>EDGE</th>
<th>THINGS</th>
</tr>
</thead>
<tbody>
<tr>
<td>End-to-end SECURITY</td>
<td>Packet Processing</td>
<td>Compute</td>
<td>Signal Processing</td>
<td></td>
</tr>
</tbody>
</table>
What is a Marvell Infrastructure Processor?

Specialized compute, Marvell’s heritage
Highly programmable & configurable blocks intelligently connected
High-performance datapath
Power-optimized

Interconnected CPU cores
Optimized Arm cores with Marvell interconnect know-how
Leading-edge process technology
Arm strategic relationship

InterCONNECT

Arm Cores 4 - 36

Packet Processing
Encryption
Regular Expression
Flexible Packet Parser
DSP
QoS
Ethernet
Programmable Hardware Accelerators

DEVELOPMENT SPEED ➔ 4
POWER ➔ 4
PERFORMANCE ➔ 4
PROGRAMMABILITY ➔ 5

Higher is better
Infrastructure Processor: Leading Compute and Data Plane

- High-end firewall
  - Crypto offload

- SMB firewall / Security gateway
  - Control plane processor

- Routers and switches
  - Control / data, crypto offload

- Macro / micro BTS
  - Transport layer and crypto
Marvell Infrastructure Processor Timeline

Data Throughput

Performance

Gen1 Gen2 Gen3 Gen4 Gen5

240 Gbps

Security IPsec

200 Gbps
OCTEON TX2 Infrastructure Processor: CN98/96xx

4C A72
20 Gbps
NOW

12-18C ARMv8.2
50 Gbps
NOW

18-24C ARMv8.2
100 Gbps
NOW

24-36C ARMv8.2
200 Gbps
Q2’2020

Unified software development environment supporting standard Linux, DPDK, containers & virtualization
Introducing the industry’s highest performing Infrastructure Processor family

- Highest Compute (SPECINTRate) SOC in its class
- Multi-core scaling w/ low latency interconnect
- Rich I/O
- HW acceleration for packet processing, encryption
CN9130 – Best Performance/Watt Processor Targeting SOHO/SMB

- CN913X – Up to 4 cores (20 Gbps)
- Supports up to 18 SERDES lanes
- <10W power consumption

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### OCTEON TX/TX2: Portfolio

<table>
<thead>
<tr>
<th>Metric</th>
<th>CN913X</th>
<th>CN83XX</th>
<th>CN92XX</th>
<th>CN96XX</th>
<th>CN98XX</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cores</td>
<td>4</td>
<td>8-24</td>
<td>12-18</td>
<td>18-24</td>
<td>30-36</td>
</tr>
<tr>
<td>Max Freq</td>
<td>2.2G</td>
<td>2.0G</td>
<td>2.0G</td>
<td>2.4G</td>
<td>2.4G</td>
</tr>
<tr>
<td>Cache (MLC, LLC)</td>
<td>2MB</td>
<td>8MB</td>
<td>5MB, 8MB</td>
<td>5MB, 14MB</td>
<td>8MB, 21MB</td>
</tr>
<tr>
<td>DDR4</td>
<td>1@2400MTS</td>
<td>2@2100MTS</td>
<td>2@3200MTS</td>
<td>3@3200MTS</td>
<td>6@3200MTS</td>
</tr>
<tr>
<td>Ethernet</td>
<td>Up to 3 x10G+6x1/2.5G</td>
<td>12x10G</td>
<td>4x25G, 8x10G</td>
<td>3x100G/12x25G</td>
<td>5x100G/20x25G</td>
</tr>
<tr>
<td>Max PPS</td>
<td>15Mpps</td>
<td>60Mpps</td>
<td>Up to 50Mpps</td>
<td>Up to 120Mpps</td>
<td>Up to 220Mpps</td>
</tr>
<tr>
<td>IP FWDing</td>
<td>Up to 25G</td>
<td>Up to 60G</td>
<td>Up to 80G</td>
<td>120G-140G</td>
<td>200G-240G</td>
</tr>
<tr>
<td>IPSEC (Gbps)</td>
<td>Up to 15G</td>
<td>30Gbps</td>
<td>50Gbps</td>
<td>100Gbps</td>
<td>200Gbps</td>
</tr>
<tr>
<td>Serdes</td>
<td>Up to 18x 10G</td>
<td>22x 10G</td>
<td>32x 16G/25G</td>
<td>32x 16G/25G</td>
<td>48-56 16G/25G</td>
</tr>
<tr>
<td>Estimated TDP</td>
<td>9W-14W</td>
<td>30W-55W</td>
<td>45W-65W</td>
<td>55W-80W</td>
<td>80W-120W</td>
</tr>
<tr>
<td>AVAILABLE</td>
<td>NOW</td>
<td>NOW</td>
<td>NOW</td>
<td>NOW</td>
<td>Q2’2020</td>
</tr>
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Unified Software Development Environment

- VPP
- OpenSSL
- Arm V8 Crypto ISA
- DPDK ENGINE
- IPSEC
- L2/L3
- Hyperscan
- Secure Storage
- Linux Kernel
- TCP/IP Routing/Bridging/iptables
- IPSEC
- Secure Boot
- Boot Loader U-Boot/UEFI

Standard Linux Apps

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Marvell Security Acceleration Performance Advantage

Infrastructure Processor with Crypto accelerator
Performance vs. software implementation with QAT

AES-CBC
Performance based on DPDK Cryptolib

<table>
<thead>
<tr>
<th>Packet size</th>
<th>Xeon D-2177NT</th>
<th>Xeon D-2187NT</th>
<th>CN96XX</th>
<th>CN98XX</th>
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</thead>
<tbody>
<tr>
<td>64</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>128</td>
<td></td>
<td></td>
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<tr>
<td>256</td>
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</tr>
<tr>
<td>512</td>
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</tr>
<tr>
<td>1024</td>
<td></td>
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<tr>
<td>2048</td>
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</table>

<table>
<thead>
<tr>
<th>Crypto Requirement (1KB Packet)</th>
<th>Intel Xeon</th>
<th>Marvell Infrastructure Processor</th>
</tr>
</thead>
<tbody>
<tr>
<td>50G</td>
<td>*128W</td>
<td>50W</td>
</tr>
<tr>
<td>100G</td>
<td>**155W</td>
<td>75W</td>
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<tr>
<td>200G</td>
<td>***300W</td>
<td>135W</td>
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</table>

Proof Point: Security Appliance Example

Intrusion Protection  |  Firewall  |  IPSEC

<table>
<thead>
<tr>
<th></th>
<th>Intrusion Prevention</th>
<th>Firewall</th>
<th>IPSEC</th>
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</thead>
<tbody>
<tr>
<td></td>
<td>12G</td>
<td>50G</td>
<td>50G</td>
</tr>
<tr>
<td></td>
<td>50G</td>
<td>200G</td>
<td></td>
</tr>
<tr>
<td></td>
<td>6G</td>
<td>100G</td>
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Higher Performance

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Proof Point: Network Visibility and Analysis Appliance

- **CPU with FPGA**
  - Xeon – 2187NT
  - FPGA
  - Power: 235W
  - Price: 3X+

- **Infrastructure Processor**
  - Marvell CN96XX: 24 Core
  - Power: <75W
  - Price: 1X
Proof Point: 5G Macro Base Station

- OCTEON Fusion CNF95XX
- OCTEON TX2 CN96XX

10/25GbE

1 to 3 DDR4 channels

RF

10/25G/40GbE Backhaul

OCTEON TX2 Arm V8.2 SoC
5G gNodeB design

DDS memory

DDS memory

DDS memory

1 to 3 DDR4 channels
Summary

- Industry-leading data path performance up to 200Gbps for networking and security applications

- Up to 5 100G MACs integrated in the OCTEON TX2 infrastructure processor leading to significant TCO advantage

- OCTEON TX2 Infrastructure Processor family scales 4 to 36 Arm v8-based architecture cores with configurable, programmable hardware accelerator blocks

Highest Performance Infrastructure Processor Family
Traditional Data Infrastructure Compute Options

CPU only

Arm / X86 Compute

<table>
<thead>
<tr>
<th>DEVELOPMENT SPEED</th>
<th>5</th>
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<tbody>
<tr>
<td>POWER</td>
<td>2</td>
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<tr>
<td>PERFORMANCE</td>
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<tr>
<td>PROGRAMMABILITY</td>
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</tbody>
</table>

FPGA

LUT and Interconnect

<table>
<thead>
<tr>
<th>DEVELOPMENT SPEED</th>
<th>3</th>
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</thead>
<tbody>
<tr>
<td>POWER</td>
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</tr>
<tr>
<td>PERFORMANCE</td>
<td>3</td>
</tr>
<tr>
<td>PROGRAMMABILITY</td>
<td>5</td>
</tr>
</tbody>
</table>

Custom ASIC

Fixed ASIC Gates

<table>
<thead>
<tr>
<th>DEVELOPMENT SPEED</th>
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<tbody>
<tr>
<td>POWER</td>
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<tr>
<td>PERFORMANCE</td>
<td>5</td>
</tr>
<tr>
<td>PROGRAMMABILITY</td>
<td>1</td>
</tr>
</tbody>
</table>
OCTEON TX2 Value Proposition: The Best of Both Worlds

3 I/O bridges (each 1+Tbps) for 200Gbps of Data-plane processing

CN98xx architecture
Essential technology, done right™