Structera™ X 2504 Memory-Expansion Controller
CXL 2.0 DDR5 4-channel expander
P/N MV-SLX25041-A0-HF350AA-C000

Overview
The Marvell® Structera™ X 2504 (P/N MV-SLX24051-A0-HF350AA-C000) device is a CXL memory-expansion controller designed to enhance memory scalability and performance in data center environments. The Structera X 2504 supports DDR5 with two DIMMs per channel, enabling a total of eight DDR5 DIMMs per controller to maximize memory capacity. Tailored for mission-critical applications like AI, it maximizes memory capacity effectively, optimizing performance for modern cloud and data center.

Products in the Structera X memory-expansion controller family are CXL 2.0 compliant and support 16 PCIe/CXL lanes for a single host or bifurcation to eight PCIe/CXL lanes for dual-host configurations.

The Structera X 2504 offers four inline LZ4 compression engines that support four channels of DDR5-3200 at full bandwidth. The compression engines support both 4KB and 1KB page sizes.

Structera X devices support inline AES-XTS 256-bit encryption and decryption, ensuring robust data security with high-performance encryption algorithms for sensitive data.

Structera X devices integrate an embedded hardware security module (eHSM) for system-level security. The eHSM securely manages cryptographic keys and provides hardware-based authentication. Coupled with secure boot capabilities, the eHSM ensures that only trusted firmware and software are loaded during system startup, safeguarding against unauthorized access and potential threats.

Block Diagram

![Block Diagram Image](image-url)
### Key Features

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| Standards and interfaces     | • PCIe 5.0 (2.5/5.0/8.0/16.0/32.0 GT/s)  
  • CXL 2.0 (8.0/16.0/32.0 GT/sec)  
  • PCIe/CXL host interfaces  
  • 16-lane physical interface (PHY) |
| CXL modes                    | • CXL 1.1 Exclusive Restricted CXL Device (eRCD) mode  
  - Power-saving modes  
  - Lane-reversal  
  - Spread-spectrum clocking for common reference-clock links  
  - QoS telemetry |
| Memory                       | • Support for DDR5:  
  - Up to 6400 MT/s data rate  
  - Subdivided into two 40-bit subchannels (32 data bits, eight ECC bits)  
  - Up to four physical ranks per subchannel  
  • U/R/LRDIMM and soldered DRAM  
  • DRAM interfaces with enhanced RAS capabilities.  
  • MPAM support for bandwidth partitioning and monitoring  
  • DRAM crypto with AES-XTS 256 on data with optional address scrambling |
| Control and management       | • Miscellaneous I/O interfaces: SPI/QSPI/xSPI, GPIO, UART, I3C, TWSI, I2C/SMBus  
  • Multiple embedded Arm Cortex M7 processors  
  - System-control processor (SCP)  
  - Management-control processor (MCP)  
  - Cryptographic-control processor (CCP)  
  - PCIe configuration-offload processor (PCP)  
  • Embedded hardware security module (eHSM) using Arm Cortex M3 processor  
  • Extensive power and thermal management capabilities  
  • Compatible with Arm Server Base System Architecture (SBSA) |
| Compression                   | • Support for 4K or 1K page sizes  
  • LZ4 algorithm support  
  • Data integrity protection, including poison and decompress-after-compress |
| Package characteristics      | • 35mm x 35mm package with 0.8 mm ball pitch |

### Target Applications
- In-memory databases
- Design simulation
- Deep learning