Product Brief

MARVELL® 7nm CUSTOM ASIC

Overview

Marvell 7nm ASIC offers a comprehensive semiconductor solution for wired, wireless, storage, and datacenter applications. Marvell 7nm ASICs are designed to deliver more significantly better power and performance with significant area savings vs previous technology nodes. This combination of performance, power and area advantages can help chip designers stay ahead of system-level demands driven by the evolving network, data center and 5G solutions.

Future-Ready IP

Marvell ASIC 7nm IP portfolio features the full range of Arm™ cores, leading-edge high-speed SERDES, and embedded SRAMs. Cutting edge 64-bit Arm™ cores enable designers to optimize their chips for performance in the most demanding communications applications. In addition to turnkey SoC capability, Marvell ASIC can leverage our extensive array of custom processors for server and infrastructure applications. Marvell ASIC also has significant experience with implementation and optimization of advanced signal processing and machine learning cores.

Optimized 112Gbps and 56Gbps SERDES designs extend the Marvell HSS roadmap in 7nm. Marvell SERDES cores provide outstanding jitter performance and equalization over a wide range of interface standards. Marvell ASIC also delivers proven advanced packaging capability supporting the latest memory technologies including HBM2E.

7nm Marvell ASICs leverage customized high performance SRAM IP to enable customers to scale up their on chip performance without sacrificing area and power. High performance dense single port, two port, multiport, and TCAM capabilities allow customers to build area efficient solutions without having to partition to multiple frequency domains.

Highlights

- Industry-leading 112G SerDes for next generation systems
- High-density SRAM optimized for Machine Learning and Network Applications
- Fully integrated Adaptive Voltage Scaling (AVS) ASIC flow
- Comprehensive portfolio of advanced packaging solutions, including MCM, chiplets, multiple HBM integration technologies

Key Features

Features		Benefits
Power Optimized ASIC	Integrated AVS	· Significant power benefit, integrated throughout the flow
	Low Voltage	· Significant reduction in active power for DSP and compute
	Vt Optimization	· Reduced leakage power
Standard Cell Differentiation	Custom Cell	· Optimized standard cells to enable high perfor¬mance design, density and power optimized MAC for machine learning
arm™ Partnership	Turnkey SOC	· Optimized SOC tuned to customer requirements - from the most advanced 64bit cores available to low power microcontroller solutions
	Custom Processor	· Ability to leverage Marvell optimized custom processors with flexible integration schemes
SERDES Leadership	Long Reach	· Power-performance optimized 112G, 56G solutions
	Chiplet Solutions	· Industry's highest bandwidth density solution for chiplet integration
Memory Solutions	Dense SRAM	· Highest bandwidth and capacity dense memory solutions optimized to packet buffer and machine learning applications
	Multiport	· Custom, high performance multiport solutions for shared memory
	Embedded TCAM	· High performance, low power TCAM solutions for demanding networking applications
Advanced Packaging	Multi Chip Module	· Chiplet and CSP integration, industry's most complex advanced packages in production today
	2.5D/Fanout	· Proven HBM integration capability for massive scale or cost optimized integration

MARVELL

Marvell first revolutionized the digital storage industry by moving information at speeds never thought possible. Today, that same breakthrough innovation remains at the heart of the company's storage, networking and connectivity solutions. With leading intellectual property and deep system-level knowledge, Marvell semiconductor solutions continue to transform the enterprise, cloud, automotive, industrial, and consumer markets. For more information, visit www.marvell.com.

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