MV78230

ARMADA® XP Highly Integrated Multi-Core ARMv7 Based System-on-Chip Processors

Hardware Specifications

Doc. No. MV-S106687-00, Rev. H
July 29, 2014, Preliminary

Document Classification: Proprietary Information

Document Conventions

	**Note:** Provides related information or information of special importance.
	**Caution:** Indicates potential damage to hardware or software, or loss of data.
	**Warning:** Indicates a risk of personal injury.

Document Status

Doc Status: Preliminary	Technical Publication: 0.xx

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Revision History

Table 1: Revision History

Revision	Date	Comments
Rev. H	July 29, 2014	Revised Release
1. Added a note in the following locations about contacting a Marvell® FAE if implementing a design integrating the LCD or FPD interfaces. • Preface on page 19 • Section 2.2.5, Flat Panel Display (FPD) Interface, on page 36 • Section 2.2.9, Liquid Crystal Display (LCD) Interface, on page 40 • Section 9.7.2, Flat Panel Display (FPD) Interface AC Timing, on page 112 • Section 9.7.3, Liquid Crystal Display Interface AC Timing, on page 114 2. In section Features on page 7, added the following bullet: - Programmable thermal sensor controller with ±5°C accuracy and overheat detection. 3. In Section 7.1, Power Up/Down Sequence, on page 76, updated Figure 6, Power Up Sequence Example, on page 77 to combine the CPU and Core voltages to a single line on the graph.. 4. In Section 7.2.1, Global System Reset (SYSRSTn), on page 77, updated the first 2 cases in which SYSRST_OUTn is asserted for a duration of 100 ms. 5. Updated Figure 69, 732-Pin FCBGA Package and Dimensions, on page 172 to remove the ball inline pitch dimension and to revise the dimension accuracy.		
Rev. G	August 4, 2013	Revised Release
Rev. F	December 4, 2012	Revised Release
Rev. E	May 28, 2012	Revised Release
Rev. D	October 9, 2011	Revised Release
Rev. C	August 15, 2011	Revised Release
Rev. B	December 15, 2010	Revised Release
Rev. A	August 24, 2010	Initial Release

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PRODUCT OVERVIEW

ARMADA® XP Family

The MV78230 is a complete system-on-chip (SoC) solution based on the Marvell® Core Processor embedded CPU technology. By leveraging the successful Marvell system controllers and extensive expertise in ARM instruction-set-compliant CPUs, the ARMADA XP Family of SoCs present a new level of performance, integration, and efficiency to raise the performance/power and performance/cost bar.

The ARMADA® XP Highly Integrated Multi-Core ARMv7 Based System-on-Chip Processors include the following devices:

- MV78230
- MV78232
- MV78260
- MV78460

With full pin and software compatibility between the different devices, the ARMADA® XP Highly Integrated Multi-Core ARMv7 Based System-on-Chip Processors enables full performance scalability to best fit the requirements of any specific application.

This specification refers to the MV78230 only. For more information about other members of the ARMADA® XP Highly Integrated Multi-Core ARMv7 Based System-on-Chip Processors, refer to the *ARMADA® XP Highly Integrated Multi-Core ARMv7 Based System-on-Chip Processors Functional Specifications*.

MV78230 Device

The Marvell ARMADA XP device presents a new level of performance, integration and efficiency to make the system design simple and cost efficient.

The MV78230 integrates Dual Superscalar CPUs with:

- ARMv7-compliant CPU cores with the latest Marvell micro-architecture enhancements, with a double precision IEEE-compliant Floating Point Unit (FPU) per core
- Shared Level 2 (L2) 1MB cache
- Low-latency, high-bandwidth, tightly coupled DDR3/DDR3L memory controller

The advanced I/O peripherals include PCI Express (PCIe) Gen1.1/2, USB2.0 with integrated PHYs, SATA ports, Ethernet, LCD, and TDM interfaces.

To allow enhanced handshake and data flow, a full hardware I/O cache coherency scheme is implemented between the I/Os and the CPU.

Optimized for low-power operation and providing advanced power management capabilities, the 40 nm process based MV78230 is ideally suited for a wide range of applications that require both high-performance and minimal power consumption. The rich and diversified interface mix of the MV78230 allows it to be the perfect solution for different types of applications and systems in various fields such as:

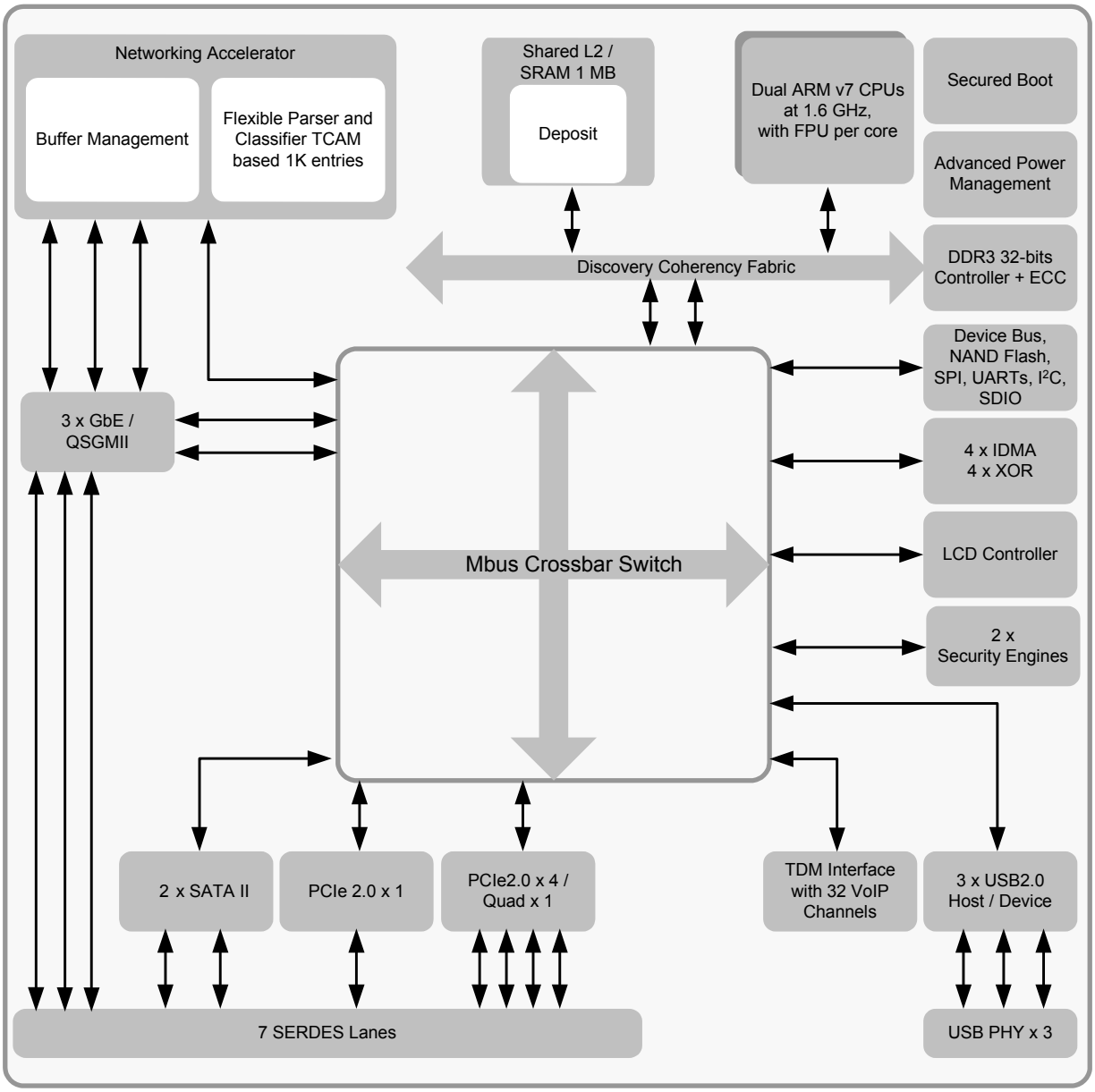
- Wireless infrastructure: Cellular, WiMax and WiFi
- Low-Mid range integrated routers
- Enterprise Network Storage (NAS, RAID, iSCSI) products
- Mid-High end consumer and Enterprise appliances (such as laser printers)
- Networking and Telecom Line cards
- Unified Threat Management boxes
- VoIP media gateways

The innovative Coherency Fabric architecture provides a coherent interconnect between the CPUs themselves and between the CPUs and the I/O masters. This enables the system to operate either in Symmetrical Multi Processing (SMP) mode or Asymmetric Multi Processing (AMP) mode, with I/O cache coherency. In addition, the efficiency of the bus enables a high-frequency, high-bandwidth, and low-latency access time throughout the CPU memory subsystem.

The on-chip Mbus architecture, a Marvell® proprietary crossbar interconnect for non-blocking any-to-any connectivity, enables concurrent transactions among multiple units. This design results in high system throughput, allowing system designers to create high-performance products.

The pin and software compatibility with the other ARMADA XP devices, offers full performance scalability to best fit the requirements of any specific applications.

MV78230 Block Diagram



FEATURES

- **The MV78230 Includes:**
  - Two high-performance, dual-issue CPU with Floating Point Unit
  - SMP/AMP operation modes
  - Supports I/O cache coherency
  - 1 MB L2 cache
  - Three 10/100/1000 Ethernet MAC controllers
  - High-bandwidth DDR3-1600 memory interface (32-bit SDRAM with ECC option)
  - Seven SERDES lanes with versatile muxing options for SGMII, QSGMII, PCIe, ETM, and SATA ports
  - PCI Express 2.0 x4 port; can also function as four x1 ports
  - Additional x1 PCI Express 2.0 port
  - Three USB Host/Device ports with integrated PHYs
  - Two integrated security cryptographic engines
  - Four IDMA engines
  - Integrated Storage Accelerator engine (four XOR DMA or iSCSI CRC engines)
  - TDM interface supporting up to 32 VoIP channels
  - 16-bit Device Bus with up to five chip selects, including NAND Flash support
  - Two SPI interfaces
  - SD/SDIO/MMC Host interface
  - LCD controller with both parallel and LVDS transmitter interfaces
  - Four 16750 compatible UART ports
  - Two I^2C interfaces
  - Programmable Timers and Watchdogs
  - Real Time Clock (RTC)
  - Adaptive Voltage Scaling (AVS)
  - Interrupt controller with priority scheme
  - Secured boot
  - Advanced power management
- **Internal Architecture**
  - High-bandwidth, low-latency Coherency Fabric interconnect between the Marvell® Core Processor CPU and CPU memory subsystem
  - Advanced Mbus (crossbar extension) architecture with any-to-any concurrent I/O connectivity
  - Full I/O cache coherency
- **Two Dual-Issue ARMv7-Compliant CPU**
  - Up to 1.6 GHz
  - Superscalar RISC CPU with Harvard architecture issues two instructions per cycle
  - Single/double precision Floating Point Unit (VFP3-16) IEEE 754 compliant per core
  - Symmetrical Multi Processing (SMP) and Asymmetric Multi Processing (AMP) modes
  - Compliant with ARMv7 architecture, published in the *ARM Architecture Reference Manual*, Second Edition
  - Supports 32-bit instruction set for performance and flexibility
  - Large Physical Address Expansion support—up to 40-bit address space
  - Thumb-2 and Thumb-EE instruction set for code density
  - Supports DSP instructions to boost performance for signal processing applications
  - MMU-ARMv7 compliant VMSA MMU
  - Management unit 4-KB L0 Instruction and data cache, direct mapping
  - 32-KB L1 Instruction cache four-way, set-associative, physically indexed physically tagged, parity protected
  - 32-KB L1 Data cache, eight-way, set-associative, physically indexed, physically tagged, parity protected
  - MESI cache coherency scheme
  - Hit-under-miss and multiple outstanding requests
  - Advanced write coalescing support
  - Variable stages pipeline—six to ten stages
  - Out-of-order execution for increased performance
  - In-order retire via a Reordering Buffer (ROB)
  - Advanced branch prediction—32 Branch Target Buffer (BTB) and 1K entries Branch Prediction Unit (BPU) with GShare algorithm
  - Branch Return Stack Point for subroutine call
  - 64-bit internal data bus with 64-bit load/store instructions
  - Endianness options—Little, Big, and Mixed Endianness
  - JTAG/ARM-compatible ICE, and Embedded Trace Module (ETM) for enhanced real time debug capabilities
- **1-MB Unified L2/SRAM**
  - Eight-way, write-back and write-through cache
  - Physically addressed
  - Non-blocking pipeline supports multiple outstanding requests and Hit Under Miss (HUM) operation
  - Per-way configured byte addressable SRAM or L2 cache

- I/O direct access to/from L2 cache/SRAM for all Mbus masters, allowing data storing directly into the L2/SRAM
- ECC protected
- Multi Gigabit Ethernet packet pre-loading, via a single CPU activation write transaction

■ **Three Gigabit Ethernet MACs**
- Supports 10/100/1000/2500 Mbps
- Full wire speed receive and transmit of short packets
- Layer 2/3/4 flexible packet modification and hardware forwarding engine
- RGMII / MII / GMII / SGMII/ DRSGMII / QSGMII
- Priority queueing on receive based on DA, VLAN-Tag, IP-TOS
- Per queue egress rate shaping
- Supports queuing based on Marvell® DSA Tag
- Layer2/3/4 frame encapsulation detection
- Supports long frames (up to 10K) on both receive and transmit
- TCP/IP acceleration
- IEEE 1588v2 support
- EEE (Energy Efficient Ethernet) support
- Hardware buffer management for off loading the software-intensive tasks of buffer memory allocation and release

■ **DDR3 SDRAM Controller**
- 32-bit interface with an ECC option
- DDR3 up to 800 MHz (DDR3-1600)
- Clock ratio of 1:N and 2:N between the DDR SDRAM and the CPU core, respectively
- SSTL 1.8/1.5V/1.35 I/Os
- Auto calibration of I/Os output impedance
- Supports four SDRAM ranks
- Supports all DDR devices densities up to 4 Gb
- Supports all DIMM configurations (registered and unbuffered, x8, or x16 SDRAM devices)
- DDR3 write and read leveling DIMM support
- DDR3 address mirroring support
- Supports DDR3 BL8
- Supports 2T and 3T modes to enable high-frequency operation even under heavy load configuration
- Supports SDRAM bank interleaving
- Supports up to 32 open pages
- Supports up to 128-byte burst per single memory access

■ **High-Speed Integrated SERDES Lanes**
- Integrated seven low-power, high-speed SERDES PHYs, based on proven Marvell SERDES technology
- Diverse muxing options of PCIe, SATA, SGMII, QSGMII, and ETM interfaces

■ **PCI Express Interfaces (x4, quad x1)**
- PCI Express Gen 1.1 at 2.5 Gbps / Gen 2.0 at 5 Gbps signaling
- May be configured as either Root Complex or Endpoint
- x1/x4 link width
- Lane polarity reversal support
- Maximum payload size of 128 bytes
- Single Virtual Channel (VC-0)
- Replay buffer support
- Extended PCI Express configuration space
- Power management: L0s and L1 ASPM active power state support; software L1 and L2 support
- MSI/MSI-x support
- Error message support

■ **Configured PCI Express x4 or Quad x1 Port**
- The PCI Express x4 port can be configured to function as four independent x1 ports, useful for interfacing multiple off-the-shelf PCI Express devices
- Each of the quad x1 ports is PCI Express Base 2.0 compliant, has its own register file, and supports the same full feature set as the x4 port

■ **Additional identical PCI-Express Gen2.0 interface (x1)**

■ **PCI Express Master Specific Features**
- Host to PCI Express bridge—translates CPU cycles to PCI Express memory or configuration cycles
- Supports DMA bursts between memory and PCI Express
- Supports up to four outstanding read transactions
- Maximum read request of up to 128 bytes
- Maximum write request of up to 128 bytes

■ **PCI Express Target Specific Features**
- Supports reception of up to four read requests
- Maximum read request of up to 4 KB
- Maximum write request of up to 128 bytes
- Supports PCI Express access to all of the device's internal registers

■ **Three USB Ports**
- USB 2.0 compliant with integrated PHY
- Each port can act as a USB Host or Device (peripheral)
- Enhanced Host Controller Interface (EHCI) compatible as a host

- As a host, supports direct connection to all peripheral types (LS, FS, HS)
- As a peripheral, connects to all host types (HS, FS) and hubs
- Up to six independent endpoints, supporting control, interrupt, bulk, and isochronous data transfers
- Dedicated DMA for data movement between memory and port

■ **Two Marvell® 3 Gbps (Gen2i) SATA Interfaces**
- Compliant with SATA II Phase 1 specifications
  - Supports SATA II Native Command Queuing (NCQ), up to 128 outstanding commands
  - First party DMA (FPDMA) full support
  - Backwards compatible with SATA I devices
- Supports SATA II Phase 2 advanced features
  - 3 Gbps (Gen2i) SATA II speed
  - Port Multiplier (PM)—Performs FIS-based switching as defined in SATA working group port multiplier definition
  - Port Selector (PS)—Issues the protocol-based Out-Of-Band (OOB) sequence to select the active host port
- Supports external SATA (eSATA)
- Supports device 48-bit addressing
- Supports ATA Tag Command Queuing
- Enhanced-DMA (EDMA) for the SATA port
  - Automatic command execution without host intervention
  - Command queuing support, for up to 128 outstanding commands
  - Separate SATA request/response queues
  - 64-bit addressing support for descriptors and data buffers in system memory
- Read ahead
- Advanced interrupt coalescing
- Advanced drive diagnostics via the ATA SMART command

■ **Two Cryptographic Engines**
- Hardware implementation on encryption and authentication engines to boost packet processing speed
- Dedicated DMA to feed the hardware engines with data from the internal SRAM memory or from the DDR memory
- Implements AES, DES, and 3DES encryption algorithms
- Implements SHA2, SHA1 and MD5 authentication algorithms

■ **Four-Channel Independent DMA Controller**
- Chaining via linked-lists of descriptors
- Moves data from any interface to any interface
- Supports increment or hold on both the source and destination address

■ **Four XOR DMA Channels**
- Useful for RAID application
- Supports XOR operation on up to eight source blocks
- Supports iSCSI CRC-32 calculation
- Supports normal DMA transfer as well

■ **TDM Interface**
- Supports up to 32 independent VoIP channels
- Generic interface to standard SLIC/SLAC/DAA/codec devices
- Compatible with standard PCM highway formats
- Dedicated DMA engine per each RX and TX channel with flexible buffer allocation and size per channel
- Fully flexible and configurable slot allocation up to 128 full duplex slots
- Each TDM channel can be used either in High-Level Data Link Control (HDLC) Bit Oriented protocol mode or in Transparent Protocol mode

■ **Device Bus Controller**
- 16-bit multiplexed address/data bus
- Supports different types of standard memory devices such as flash and ROM
- Supports NAND Flash
- Five chip selects with programmable timing
- Optional external wait-state support
- 8/16-bit width device support
- Up to 128B burst per a single device bus access

■ **Two SPI Ports**
- General purpose SPI interface
- Up to 8 chip selects
- Supports boot from SPI Flash

■ **SD/SDIO/MMC Host Interface**
- 1-bit/4-bit SDmem, SDIO, and MMC cards
- Up to 50 MHz
- Hardware generate/check CRC on all command and data transaction on the card bus

■ **Four UART Interfaces**
- 16750 UART compatible
- Each port has two pins for transmit and receive operations, and two pins for modem control functions
- One channel also supports an integrated DMA, capable of up to 64-KB transfer

■ **Integrated programmable 32-bit timers/counters and watchdog timers**

- **Interrupt Controller**
  - Advanced interrupt controller with interrupt prioritization mechanism
- **Two I^2C Interfaces**
  - General purpose I^2C master/slave
  - EEPROM Serial initialization support
- **LCD Controller**
  - Either parallel or serialized LVDS interface for connecting with remote panels
  - Up to 24 bits per pixel (bpp) RGB
  - Three overlay layers (video, graphics, and cursor)
  - YC_bC_r to RGB conversion
  - YC_bC_r 4:4:4, 4:2:2 or 4:2:0 input support
  - Color management (brightness, contrast, and hue)
  - Up-scaling and down-scaling support
  - Linear horizontal and vertical up-scaling
  - Color platter: Three 256 entries (2/4/8 bpp) for video and graphic overlay channels
  - Alpha blending support for color panels
  - Dedicated DMA for data movements between memory and port
  - Pulse Width Modulation control
  - Dedicated display PLL for maximum precision in interface clock ratio
- **Real Time Clock**
- **Integrated BootROM with secured boot flow option**
- **Multi-purpose Pins dedicated for peripheral functions and General Purpose I/O**
  - Each pin can be configured independently
  - GPIO inputs can be used to register interrupts from external devices, and generate maskable interrupts
- **Clock Generation Support**
  - Internal generation of CPU core clock, SDRAM clock, Core clock, PCIe clock, GbE clock, USB clock, and SATA clock from a single 25-MHz reference clock
  - Supports internal generation of spread spectrum clocking on the CPU and SDRAM clocks
- **Advanced Power Saving Modes**
  - Dynamic CPU frequency scaling for each of the cores
  - CPU wait for interrupt mode
  - Dynamic power down options
  - Selectable clock gating of different interfaces
  - SDRAM Self Refresh and Power Down modes
  - PCI Express, SGMII, USB, and SATA SERDES shutdown
  - Programmable thermal sensor controller with ±5°C accuracy and overheat detection.
  - Various wake up options
- **FCBGA 23 x 23 mm package, pin compatible with the MV78460 and MV78260 devices**

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Preface

About this Document

This document provides the hardware specifications for the Marvell® MV78230 device. The hardware specifications include detailed pin information, configuration settings, electrical characteristics and physical specifications.

This document is intended to be the basic source of information for designers of new systems.

In this document, the MV78230 is often referred to as the “device”.

Note Before designing a system implementing the Liquid Crystal Display (LCD) interface or the Flat Panel Display (FPD) interface, contact a Marvell® Field Applications Engineer (FAE).

Related Documentation

The following documents contain additional information related to the MV78230. For the latest revision, contact a Marvell representative.

Title	Document Number
ARMADA® XP Family of Highly Integrated Multi-Core ARMv7 Based SoC Processors Functional Specifications	MV-S107021-00
MV78230/78x60 Design Guide	MV-S301878-00
ARMADA® XP MP Core Highly Integrated Marvell ARMv7 SoC Processors Datasheet	MV-S108492-00
MV78230/78x60 ARMADA® XP Family of Highly Integrated Multi-Core ARMv7 Based SoC Processors Functional Errata	MV-S501280-00
MV78230/78x60 ARMADA® XP Family of Highly Integrated Multi-Core ARMv7 Based SoC Processors CPU Core Errata	MV-S501281-00

See the Marvell Extranet website for the latest product documentation.

Document Conventions

The following conventions are used in this document:

Signal Range	A signal name followed by a range enclosed in brackets represents a range of logically related signals. The first number in the range indicates the most significant bit (MSb) and the last number indicates the least significant bit (LSb). Example: DB_Addr[12:0]
Active Low Signals #	An n letter at the end of a signal name indicates that the signal's active state occurs when voltage is low. Example: INTn
State Names	State names are indicated in *italic* font. Example: *linkfail*
Register Naming Conventions	Register field names are indicated by angle brackets. Example: <RegInit> Register field bits are enclosed in brackets. Example: Field [1:0] Register addresses are represented in hexadecimal format. Example: 0x0 Reserved: The contents of the register are reserved for internal use only or for future use. A lowercase <n> in angle brackets in a register indicates that there are multiple registers with this name. Example: Multicast Configuration Register<n>
Reset Values	Reset values have the following meanings: 0 = Bit clear 1 = Bit set
Abbreviations	Kb: kilobit KB: kilobyte Mb: megabit MB: megabyte Gb: gigabit GB: gigabyte
Numbering Conventions	Unless otherwise indicated, all numbers in this document are decimal (base 10). An 0x prefix indicates a hexadecimal number. An 0b prefix indicates a binary number.

1 Typical Applications and System Configurations

The MV78230 can be used in a variety of applications. Examples of these applications are provided in the following sections.

1.1 NVR/DVR/Hybrid Video Surveillance Application

Video surveillance applications, Network Video Recorders (NVR), and Digital Video Recorders (DVR) can also take advantage of the MV78230 SoC.

The high-integration of the MV78230 that resides within the NVR box, with the high-performance core processor CPU, drives H.264 or MPEG-2 data streams from multiple camera banks that are connected over the GbE ports to various I/Os. These I/Os include storage (disks over PCIe or SATA interfaces) or remote host monitoring (over Ethernet interface). The TCP acceleration features offered by the device, and the ability to balance the work load on the CPUs handling the incoming TCP streams, enables the platform to support dozens of the high definition IP cameras.

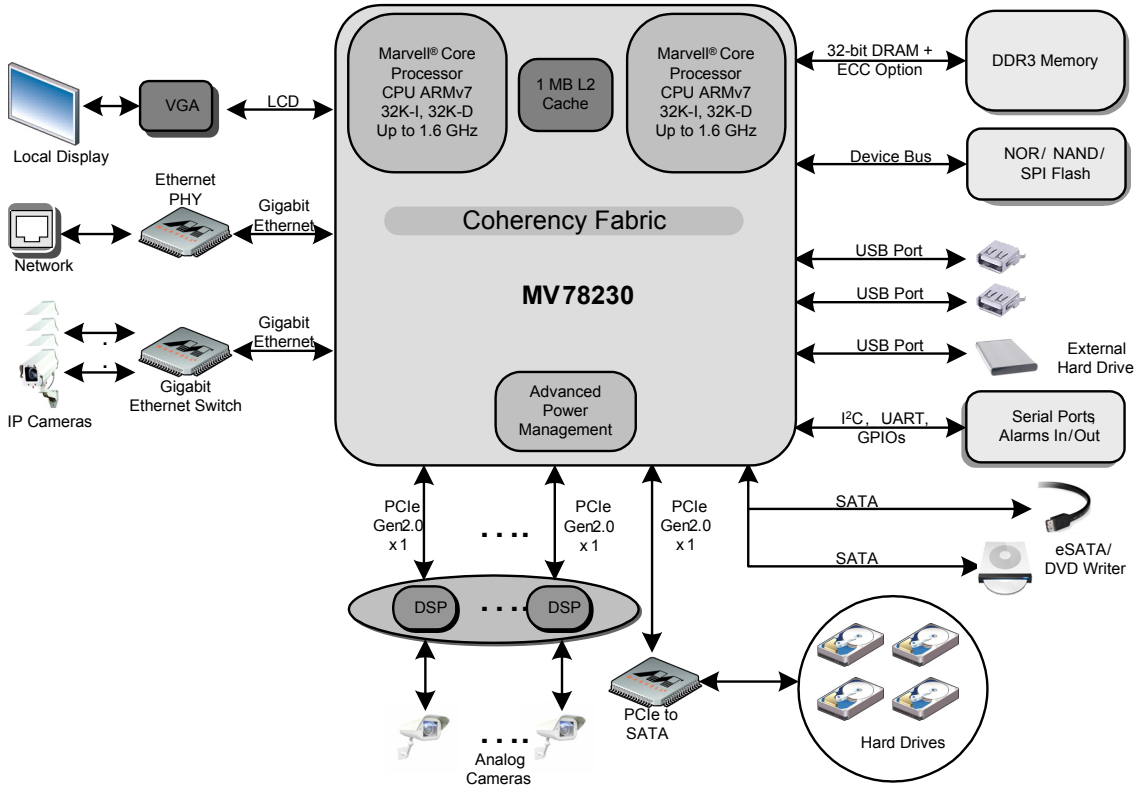
High-performance writes and reads to mass storage are an essential centerpiece for these applications, and the device offers outstanding performance in this arena.

There are several storage expansion options with the two PCIe ports, offering five to eight high-speed, 5 Gbps PCIe lanes, and enabling connectivity to mass storage or DSP banks to interface analog cameras. The fluent PCIe-to-Memory and Memory-to-PCIe operations of the MV78230, the effective disk access, and the core processor CPU capability to successfully handle the high frame rate and resolution from a large number of sources, enables the device to support the application's target number of analog cameras.

The three USB ports with integrated PHYs, the SATA ports that can be used for eSATA extensions or a DVD write backup interface, with the LCD interface that can be used for a local view via VGA, and the integrated clock generation and security engine offer a complete SoC integrated solution at low power to make this SoC the ideal choice for such applications.

Figure 1 shows an example of MV78230 in a hybrid surveillance box application.

Figure 1: MV78230 in a Hybrid Surveillance Box Application



1.2 Enterprise Laser Printer Application

The MV78230 I/O integration, low power, strong core processor CPUs, and an on-chip Floating Point Unit (FPU) makes the device an ideal solution for high-performance enterprise printer applications. The device integrates several I/O peripherals that result in a smaller, simpler board design with lower manufacturing cost.

The device's advanced power save modes enable a power-saving, environmentally friendly, green printer design that meets the restrictive power consumption requirements of worldwide energy regulations, such as Energy Star, EuP, and Top Runners.

In addition to system level power save modes such as DRAM power save modes, Energy Efficient Ethernet, PCIe, and USB power save modes, the MV78230 offers chip level power save options that include power down modes, standby modes, clock throttling modes.

To complete this device's efficient operation, it offers diverse waking options from power save modes, such as:

- Diversified Wake On LAN (WOL) options
- Wake On USB
- Wake On GPIO

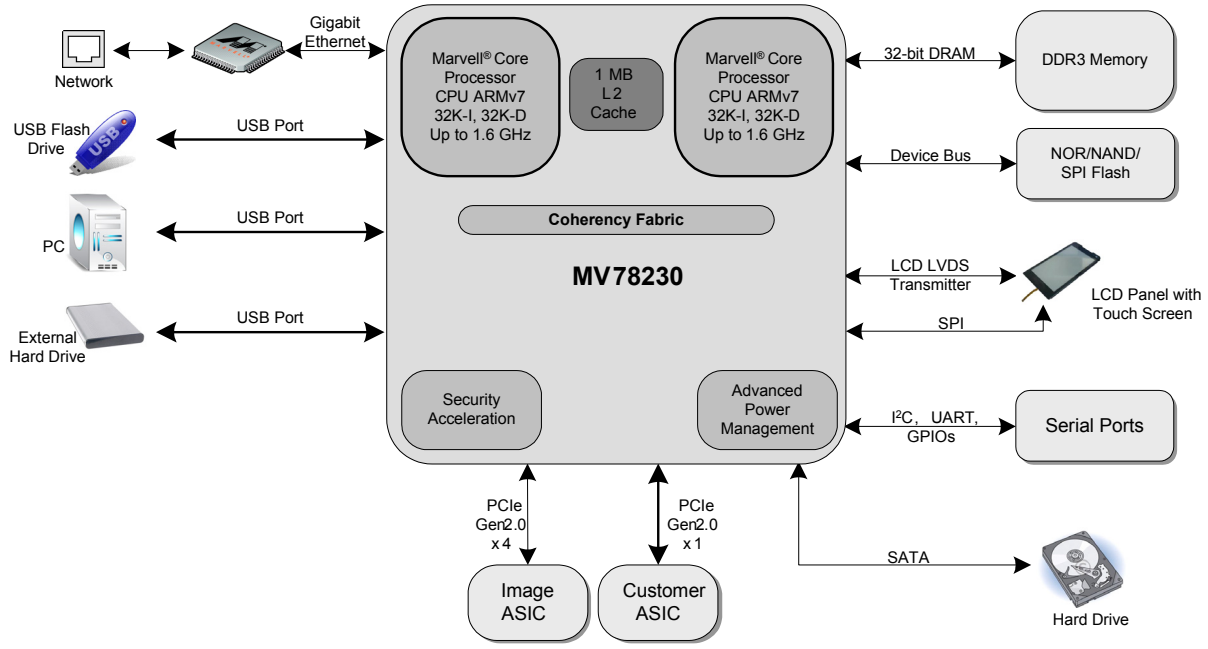
It also guarantees zero packet loss during the wake-up period until the CPU is powered up and ready to process the incoming packets.

The multiple PCIe lanes allow printer designers to connect imaging ASICs to the x4 PCIe interfaces, and use the x1 configurations for other PCIe peripherals. The three on-chip USB ports can connect to PCs, scanners, fax machines, USB flash drives, or wireless connectivity devices. The integrated SATA interface eliminates the need for an external SATA controller for the printer's spooling hard drive.

The integrated LCD controller is capable of supporting up to 24 bpp, with high resolution. It can be used to interface with the printer's LCD panel. The integrated SPI controller provides the option to interface with an LCD screen, if it is used as a touch screen. As in most printers, the LCD panel is located relatively far from the CPU, the device provides LVDS transmitters for the clock and data to connect between the device's LCD logic and the remote LCD panel.

Figure 2 shows a MV78230 SoC in an enterprise laser printer application.

Figure 2: MV78230 in an Enterprise Laser Printer Application



1.3 Enterprise Wireless Access Point

The MV78230 is a perfect fit for Enterprise class wireless access point.

The two CPUs may be used either in AMP mode, where one core is handling the traffic and the other core handles the application layer, or in SMP mode where both cores are running symmetrically as a single ultra-powerful CPU core that can handle both tasks.

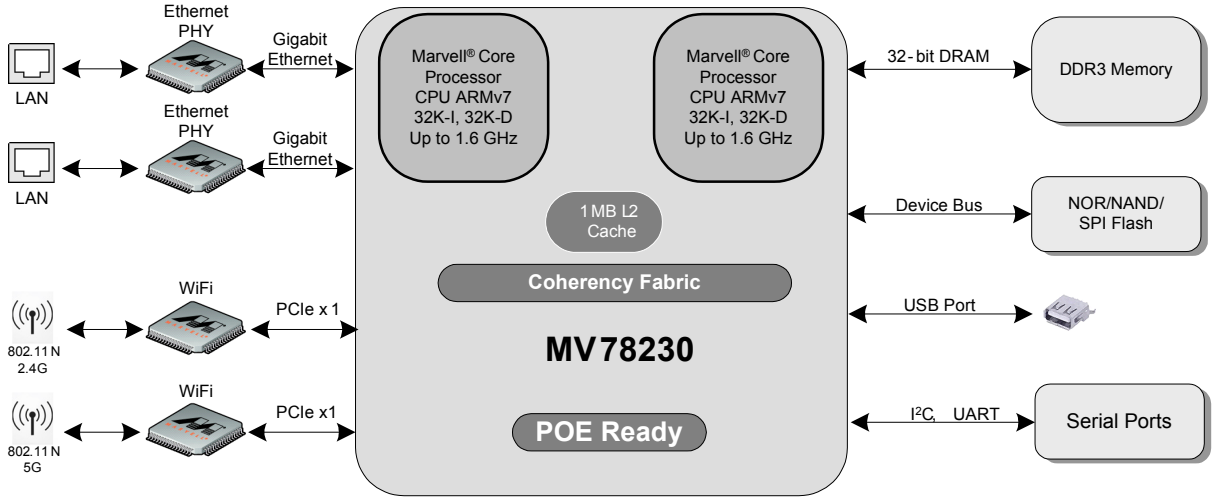
The high-bandwidth PCIe ports (Gen2.0, 5 Gbps) provide the needed connectivity to the WiFi modules, while the internal proprietary MBus interconnect accelerates the data flow to and from the memory.

The integrated security accelerator can be used for secured traffic exchange with the LAN, while the USB/SDIO ports can be used for software upgrade access.

The low power consumption of the device enables the access point solution to be powered by Ethernet (POE) ready.

Figure 3 shows the MV78230 in a typical wireless access point application.

Figure 3: MV78230 Enterprise Wireless Access Point



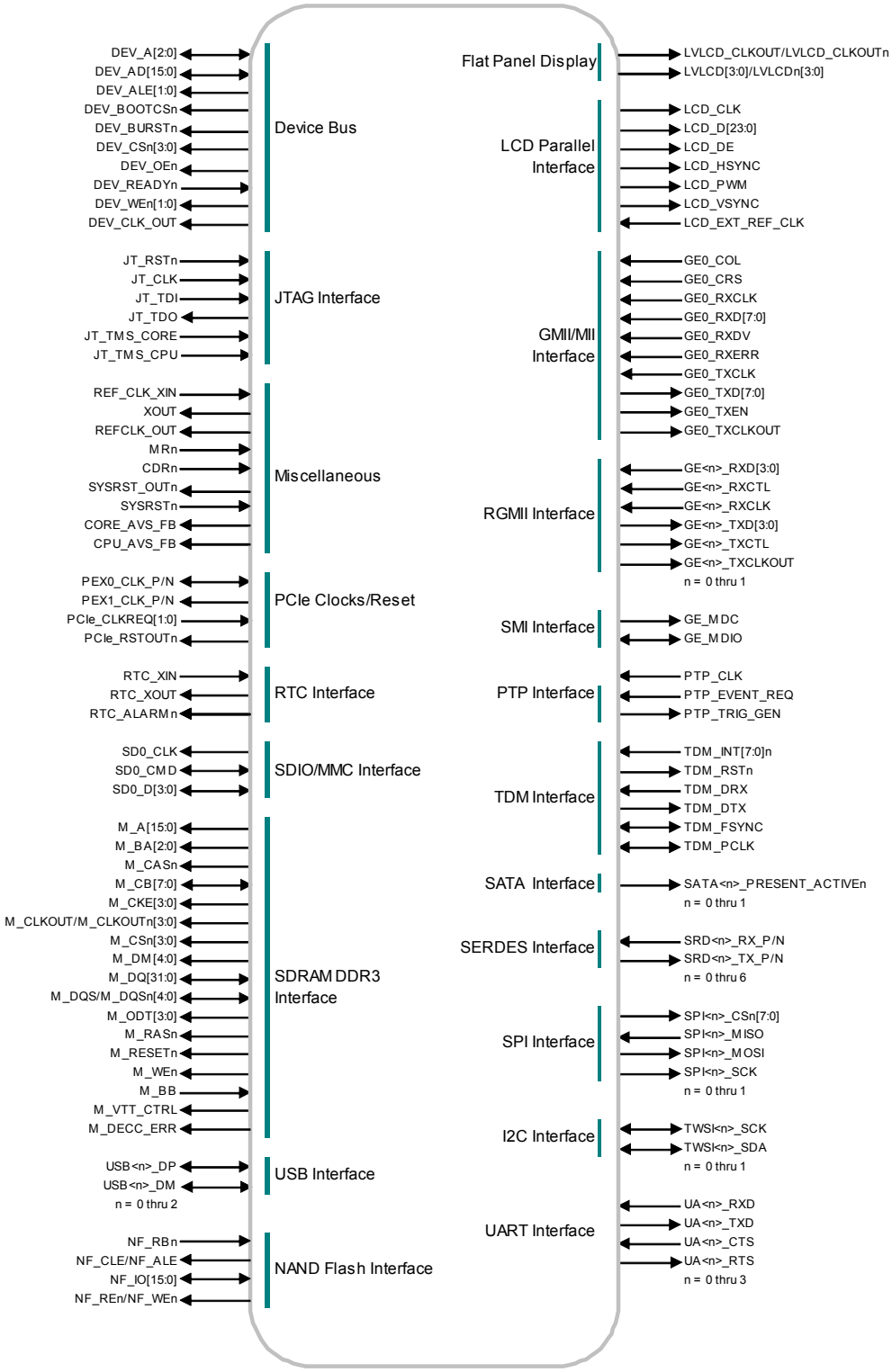
2 Pin Information

This section provides the pin logic diagram for each device and a detailed description of the pin assignments and their functionality.

2.1 Pin Logic

This section provides the pin logic diagram for the MV78230.

Figure 4: MV78230 Pin Logic Diagram



2.2 Pin Descriptions

This section details all the pins for the different interfaces providing a functional description of each pin and pin attributes.

Table 2 defines the abbreviations and acronyms used in the pin description tables.

Table 2: Pin Functions and Assignments Table Key

Term	Definition
<n>	Represents port number when there are more than one ports
Analog	Analog Driver/Receiver or Power Supply
Calib	Calibration pad type
CML	Current Mode Logic
CMOS	Complementary Metal-Oxide-Semiconductor
DDR	Double Data Rate
GND	Ground Supply
HCSL	High-speed Current Steering Logic
I	Input
I/O	Input/Output
LVDS	Low-Voltage Differential Signaling
O	Output
OD	Open Drain pin
Power	Power Supply
SDR	Single Data Rate
SSTL	Stub Series Terminated Logic
t/s	Tri-State pin
TS	Tri-State Value
XXXn	n - Suffix represents an Active Low Signal

Table 3: Interface Pin Prefixes

Interface	Prefix
Gigabit Ethernet	GE_
JTAG	JT_
Liquid Crystal Display	LCD_
LCD Flat Panel Display (LVDS)	LVLCD_
SDRAM	M_
Misc	N/A

Table 3: Interface Pin Prefixes (Continued)

Interface	Prefix
MPP	N/A
NAND Flash	NF_
PCI Express	PEX_ PCIe_
Precise Time Protocol	PTP_
Real Time Clock	RTC_
Secure Digital Input/Output	SDIO_
SERDES	SRD_
SPI	SPI_
TDM	TDM_
I^2C	TWSI_
UART	UA_
USB	USB_

2.2.1 Gigabit Ethernet Port Interface Pin Assignments

Note

The GE0/GE1 signals are implemented on the Multi Purpose Pin Interface. See Section 6, Pin Multiplexing, on page 67.

Table 4: Gigabit Ethernet Port Interface Pin Assignments

Pin Name	I/O	Pin Type	Power Rail	Description
GbE Port0				
GE0_ TXCLKOUT	O	CMOS	VDDO_A	RGMII Transmit Clock Provides 125 MHz for 1000 Mbps, 25 MHz for 100 Mbps, and 2.5 MHz for 10 Mbps. All RGMII output pins are referenced to GE0_TXCLKOUT
				GMII Transmit Clock All GMII output pins are referenced to GE0_TXCLKOUT.
GE0_TXCLK	I	CMOS	VDDO_B	MII Transmit Reference Clock This clock is provided by an external PHY device connected to the MAC. All MII output pins are referenced to GE0_TXCLK.
GE0_TXD[3:0]	O	CMOS DDR	VDDO_A	RGMII Transmit Data Contains the transmit data nibble outputs that run at double data rate. Bits [3:0] are presented on the rising edge of GE0_TXCLKOUT.
		CMOS SDR		MII Transmit Data This bus is referenced to GE0_TXCLK.
				GMII Transmit Data This bus is referenced to GE0_TXCLKOUT
GE0_TXD[7:4]	O	CMOS SDR	VDDO_A	GMII Transmit Data This bus is referenced to GE0_TXCLKOUT.
GE0_TXCTL/ GE0_TXEN	O	CMOS DDR	VDDO_A	RGMII Transmit Control A logical derivative of transmit data enable (TXEN) on GE0_TXCLKOUT rising edge, and data error (TXERR) on GE0_TXCLKOUT falling edge.
		CMOS SDR		MII Transmit Enable Indicates that the packet is being transmitted on the data lines. This pin is referenced to GE0_TXCLK.
				GMII Transmit Enable Indicates that the packet is being transmitted on the data lines. This pin is referenced to GE0_TXCLKOUT.

Table 4: Gigabit Ethernet Port Interface Pin Assignments (Continued)

Pin Name	I/O	Pin Type	Power Rail	Description
GE0_CRS	I	CMOS	VDDO_B	MII Carrier Sense Indication This signal is relevant for half-duplex mode only. This signal is asynchronous.
				GMII Carrier Sense Indication This signal is relevant for half-duplex mode only. This signal is asynchronous.
GE0_RXD[3:0]	I	CMOS DDR	VDDO_A	RGMII Receive Data Contains the receive data nibble inputs that run at double data rate. Bits [3:0] are presented on the rising edge of GE0_RXCLK.
		CMOS SDR		MII Receive Data This bus is referenced to GE0_RXCLK.
				GMII Receive Data This bus is referenced to GE0_RXCLK.
GE0_RXD[7:4]	I	CMOS SDR	VDDO_A	GMII Receive Data This bus is referenced to GE0_RXCLK.
GE0_RXERR	I	CMOS SDR	VDDO_B	MII Receive Error This pin is referenced to GE0_RXCLK.
				GMII Receive Error This pin is referenced to GE0_RXCLK.
GE0_RXCTL/ GE0_RXDV	I	CMOS DDR	VDDO_A	RGMII Receive Control A logical derivative of receive data valid (RXDV) on GE0_RXCLK rising edge, and data error (RXERR) on GE0_RXCLK falling edge.
		CMOS SDR		MII Receive Data Valid This pin is referenced to GE0_RXCLK.
				GMII Receive Data Valid This pin is referenced to GE0_RXCLK.
GE0_RXCLK	I	CMOS	VDDO_A	RGMII Receive Clock Receives 125 MHz for 1000 Mbps, 25 MHz for 100 Mbps, and 2.5 MHz for 10 Mbps. All RGMII input pins are referenced to GE0_RXCLK.
				MII Receive Clock RXD, RXDV, and RXERR pins are referenced to GE0_RXCLK.
				GMII Receive Clock RXD, RXDV, and RXERR pins are referenced to GE0_RXCLK.
GE0_COL	I	CMOS	VDDO_B	MII Collision Indication This signal is relevant for half-duplex mode only. This signal is asynchronous.

Table 4: Gigabit Ethernet Port Interface Pin Assignments (Continued)

Pin Name	I/O	Pin Type	Power Rail	Description
GbE Port1				
GE1_ TXCLKOUT	O	CMOS	VDDO_B	RGMII Transmit Clock Provides 125 MHz for 1000 Mbps, 25 MHz for 100 Mbps, and 2.5 MHz for 10 Mbps. All RGMII output pins are referenced to GE1_TXCLKOUT.
GE1_TXD[3:0]	O	CMOS DDR	VDDO_B	RGMII Transmit Data Contains the transmit data nibble outputs that run at double data rate. Bits [3:0] are presented on the rising edge of GE1_TXCLKOUT.
GE1_TXCTL	O	CMOS DDR	VDDO_B	RGMII Transmit Control A logical derivative of transmit data enable (TXEN) on GE1_TXCLKOUT rising edge, and data error (TXERR) on GE1_TXCLKOUT falling edge.
GE1_RXD[3:0]	I	CMOS DDR	VDDO_B	RGMII Receive Data Contains the receive data nibble inputs that run at double data rate. Bits [3:0] are presented on the rising edge of GE1_RXCLK.
GE1_RXCTL	I	CMOS DDR	VDDO_B	RGMII Receive Control A logical derivative of receive data valid (RXDV) on GE1_RXCLK rising edge, and data error (RXERR) on GE1_RXCLK falling edge.
GE1_RXCLK	I	CMOS	VDDO_B	RGMII Receive Clock Receives 125 MHz for 1000 Mbps, 25 MHz for 100 Mbps, and 2.5 MHz for 10 Mbps. All RGMII input pins are referenced to GE1_RXCLK.

2.2.2 Serial Management Interface (SMI)

Table 5: Serial Management Interface (SMI) Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
GE_MDC	O	CMOS	VDDO_A	Serial Management Interface Data Clock Provides the timing reference for the transfer of the GE_MDIO signal. **NOTE:** When not used, can be left NC. This pin has an integrated pull-down resistor.
GE_MDIO	I/O	CMOS SDR	VDDO_A	Serial Management Interface Data Input/Output Must be pulled up to VDDO_A using a 2.0 kilohm resistor. **NOTE:** When not used, must be pulled up to VDDO_A.

2.2.3 Device Bus/NAND Flash Interface Pin Assignments

Table 6: Device Bus/NAND Flash Interface Pin Assignments

Pin Name	I/O	Pin Type	Power Rail	Description
DEV_CSn[3:0]	O	CMOS SDR	VDDO_ DEV	For a Device bus, used as the device bus chip select that corresponds to ranks [3:0]. **NOTE:** These pins have integrated pull-up resistors.
				For a NAND Flash interface, used as a chip enable signal. **NOTE:** DEV_CSn[0] is the boot chip select for the NAND Flash Controller 2.0, only.
DEV_BOOTCSn	O	CMOS SDR	VDDO_ DEV	Device Bus Boot Chip Select **NOTE:** This pin has an integrated pull-up resistor. When the boot device is a NAND Flash interface, use DEV_CSn[0] as the boot chip select for the NAND Flash Controller 2.0.
DEV_OEn/ DEV_A[15]	O	CMOS SDR	VDDO_ DEV	For a Device bus, used as device bus output enable. Used as DEV_A[15] (device address bus) during first ALE cycle (DEV_ALE[1]). **NOTE:** This pin has an integrated pull-up resistor.
				For a NAND Flash interface, used as NF_REn.
DEV_WEn[1:0]/ DEV_A[16]	O	CMOS SDR	VDDO_ DEV	For a Device bus, used as a device bus byte write enable (bit per byte). DEV_WEn[0] is used as DEV_A[16] (device address bus) during first ALE cycle (DEV_ALE[1]). **NOTE:** DEV_WEn[0] has an integrated pull-up resistor. DEV_WEn[1] has an integrated pull-down resistor. For the NAND Flash interface, see the functional specification for further information on their usage.
				For a NAND Flash interface, DEV_WEn[0] is used as NF_WEn.
DEV_ALE[1:0]	O	CMOS SDR	VDDO_ DEV	Device Bus Address Latch Enable **NOTE:** These pins have integrated pull-down resistors.
DEV_AD[7:0]/ DEV_A[13:6]/ DEV_A[26:19]	t/s I/O	CMOS SDR	VDDO_ DEV	For a Device bus, used as DEV_AD[7:0] (device data bus) during the data phase. Driven by MV78230 on write access, and by the device on read access. Used as DEV_A[13:6] (device address bus) during first ALE cycle (DEV_ALE[1]). Used as DEV_A[26:19] (device address bus) during second ALE cycle (DEV_ALE[0]). **NOTE:** These pins have integrated pull-up/down resistors.
				For a NAND Flash interface, used as NF_IO[7:0].

Table 6: Device Bus/NAND Flash Interface Pin Assignments (Continued)

Pin Name	I/O	Pin Type	Power Rail	Description
DEV_AD[15:8]/ DEV_A[14]/ DEV_A[15]	t/s I/O	CMOS SDR	VDDO_ DEV	For a Device bus, used as DEV_AD[15:8] (device data bus) during the data phase. Driven by MV78230 on write access, and by the device on read access. DEV_AD[8] is used as DEV_A[14] (device address bus) during first ALE cycle (DEV_ALE[1]). DEV_AD[8] is used as DEV_A[15] (device address bus) during second ALE cycle (DEV_ALE[0]). **NOTE:** These pins have integrated pull-up/down resistors.
				For a NAND Flash interface, used as NF_IO[15:8].
DEV_A[2:0]/ DEV_A[5:3]/ DEV_A[18:16]	t/s I/O	CMOS SDR	VDDO_ DEV	For a Device bus, used as the device bus address. DEV_A[2:0] is used during the data phase. DEV_A[2:0] is not latched, but connected directly to the device. It is an incrementing address in case of burst access. Used as DEV_A[5:3] during the first ALE cycle (DEV_ALE[1]). Used as DEV_A[18:16] during the second ALE cycle (DEV_ALE[0]). **NOTE:** These pins have integrated pull-up/down resistors.
				For a NAND Flash interface: • DEV_A[0] is NF_CLE (Command Latch Enable) • DEV_A[1] is NF_ALE (Address Latch Enable)
DEV_READYn	I	CMOS SDR	VDDO_ DEV	For a Device bus, used as the Device READY signal. Used as cycle extender when interfacing a slow device. When inactive during a device access, the access is extended until DEV_READYn assertion. **NOTE:** This pin has an integrated pull-down resistor.
DEV_BURSTn/ DEV_LASTn	O	CMOS SDR	VDDO_ DEV	Device Burst/Device Last **NOTE:** This signal is multiplexed on MPP, see Section 6.1, Multi Purpose Pins Functional Summary, on page 67.
DEV_CLK_OUT	O	CMOS SDR	VDDO_ DEV	Device Clock Output Clock reference when in synchronous device bus mode. The pin can be configured to drive a clock running at 1:N of TCLK rate. **NOTE:** This signal is multiplexed on MPP, see Section 6.1, Multi Purpose Pins Functional Summary, on page 67.
NF_RBn	I	CMOS SDR	VDDO_D EV	NAND Flash READY/BUSY signal to indicate the target status. When the signal is low, it indicates that one or more operations are in progress. **NOTE:** This signal is multiplexed on MPP, see Section 6.1, Multi Purpose Pins Functional Summary, on page 67.

2.2.4 Multi Purpose Pin Assignment

Note

See Section 6, Pin Multiplexing, on page 67 for additional information about the MPP pins.

Table 7: Multi Purpose Pin Assignments

Pin Name	I/O	Pin Type	Power Rails	Description
MPP[11:0]	t/s I/O	CMOS	VDDO_A	Multi Purpose Pins Various functionalities **NOTE:** These pins have internal pull-up/down resistors.
MPP[23:12]	t/s I/O	CMOS	VDDO_B	Multi Purpose Pins Various functionalities **NOTE:** These pins have internal pull-up/down resistors.
MPP[35:24]	t/s I/O	CMOS	VDDO_C	Multi Purpose Pins Various functionalities **NOTE:** These pins have internal pull-up/down resistors.
MPP[47:36]	t/s I/O	CMOS	VDDO_D	Multi Purpose Pins Various functionalities **NOTE:** These pins have internal pull-up/down resistors.
MPP[48]	t/s I/O	CMOS	VDDO_ DEV	Multi Purpose Pin Various functionalities **NOTE:** These pins have internal pull-up/down resistors.

2.2.5 Flat Panel Display (FPD) Interface

Note

- Before designing a system implementing the Flat Panel Display (FPD) interface, contact a Marvell® Field Applications Engineer (FAE).
- When unused, can be left unconnected.

Table 8: Flat Panel Display (FPD) Interface Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
LVLCD_CLKOUTn LVLCD_CLKOUT	O	LVDS	VDDO_FPD	Differential LVDS pixel clock output.
LVLCDn[3:0] LVLCD[3:0]	O	LVDS	VDDO_FPD	Differential LVDS data output.

2.2.6 General Purpose Pins (GPP)

Each individual pin can be defined as an input, output, or edge-sensitive interrupt input.

These pins can be used for indications retrieving or for peripherals control.

Table 9: Genera Purpose Pins (GPP) Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
GPIO[11:0]	I/O	CMOS	VDDO_A	General Purpose Pin(s)
GPIO[23:12]	I/O	CMOS	VDDO_B	General Purpose Pin(s)
GPIO[35:24]	I/O	CMOS	VDDO_C	General Purpose Pin(s)
GPIO[47:36]	I/O	CMOS	VDDO_D	General Purpose Pin(s)
GPIO[48]	I/O	CMOS	VDDO_ DEV	General Purpose Pin(s)

2.2.7 Inter-Integrated Circuit Interface (I^2C)

I2C and TWSI both refer to the same interface. Either name can be used in this document.

Table 10: Inter-Integrated Circuit Interface (I^2C) Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
Where <n> represents numbers 0 thru 1				
TWSI<n>_SCK	I/O OD	CMOS	VDDO_MISC	TWSI (I2C) Serial Clock Serves as output when acting as a TWSI (I2C) master. Serves as input when acting as a TWSI (I2C) slave. **NOTE:** Requires a 4.7 kohm pull-up resistor to VDDO_MISC.
TWSI<n>_SDA	I/O OD	CMOS SDR	VDDO_MISC	TWSI (I2C) Serial Data/Address Address or write data driven by the TWSI (I2C) master or read response data driven by the TWSI (I2C) slave. **NOTE:** Requires a 4.7 kohm pull-up resistor to VDDO_MISC.

2.2.8 JTAG Interface

The device supports a JTAG interface and is compliant with the IEEE 1149.1 standard.

It supports mandatory and optional boundary scan instructions.

Table 11: JTAG Interface Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
JT_CLK	I	CMOS	VDDO_MISC	JTAG Test Clock JT_TDI, JT_TDO, JT_TMS_CORE and JT_TMS_CPU are referenced to this clock. **NOTE:** This pin has an integrated pull-down resistor.
JT_TDI	I	CMOS SDR	VDDO_MISC	JTAG Test Data Input Sampled on JT_CLK rising edge. **NOTE:** This pin has an integrated pull-up resistor.
JT_TDO	O	CMOS SDR	VDDO_MISC	JTAG Test Data Output Driven on JT_CLK falling edge.
JT_TMS_CORE	I	CMOS SDR	VDDO_MISC	JTAG Test Mode Select Sampled on JT_CLK rising edge. TMS signal for boundary scan mode (see the JTAG Interface section). **NOTE:** When unused, must be pulled up to VDDO_MISC.
JT_TMS_CPU	I	CMOS SDR	VDDO_MISC	JTAG Test Mode Select Sampled on JT_CLK rising edge. TMS signal for CPU debugger and trace mode (see the JTAG Interface section). CPU for debugger connectivity **NOTE:** This pin has an integrated pull-up resistor.
JT_RSTn	I	CMOS	VDDO_MISC	JTAG Test Asynchronous Reset **NOTE:** This pin has an integrated pull-down resistor. If this pull-down conflicts with other devices, the JTAG tool must not use this signal. This signal is not mandatory for the JTAG interface, since the TAP (Test Access Port) can be reset by driving the JT_TMS signal HIGH for 5 JT_CLK cycles.

2.2.9 Liquid Crystal Display (LCD) Interface

The device supports the following resolutions:

- One layer: Up to 1024x768
- Two layers: Up to 1024x600

For the targeted resolution, select the 25 MHz or 27 MHz reference clock.

Note

- Before designing a system implementing the Liquid Crystal Display (LCD) interface, contact a Marvell® Field Applications Engineer (FAE).
- This interface is implemented on the Multi Purpose Pin interface. For more information, see Section 6, Pin Multiplexing.

Table 12: Liquid Crystal Display (LCD) Interface Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
LCD_CLK	O	CMOS	VDDO_C	LCD Pixel Clock LCD_E, LCD_D[23:0], LCD_HSYNC, and LCD_VSYNC are referenced to this clock.
LCD_D[11:0]	O	CMOS SDR	VDDO_A	LCD Data Bus This signal is referenced to LCD_CLK. **NOTE:** The power rail is determined by which MPP pin is configured to support these signals. For more information, see Section 6, Pin Multiplexing.
LCD_D[23:12]			VDDO_B	
LCD_E	O	CMOS SDR	VDDO_C	LCD Data Enable (pixel valid indication) This signal is referenced to LCD_CLK.
LCD_PWM	O	CMOS	VDDO_C	LCD Pulse Width Modulation Control
LCD_EXT_REF_CLK	I	CMOS	VDDO_C	LCD Reference clock for generating LCD pixel clock when internal clock is unused.
LCD_HSYNC	O	CMOS SDR	VDDO_C	LCD Horizontal Synchronization This signal is referenced to LCD_CLK. If an external VGA DAC is used, this signal can control the signals delay to compensate for the external DAC pipeline delay.
LCD_VSYNC	O	CMOS SDR	VDDO_C	LCD Vertical Synchronization This signal is referenced to LCD_CLK. If an external VGA DAC is used, this signal can control the signals delay to compensate for the external DAC pipeline delay.

2.2.10 Miscellaneous Signals

The Miscellaneous signals list contains clocks, reset, and PLL related signals.

Table 13: Miscellaneous Signals Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
CDRn	I	CMOS	VDDO_MISC	Active low, CPU Debugger Reset input. May be used by the debugger logic to reset the device. **NOTE:** This pin is internally pulled up.
MRn	I	CMOS	VDDO_MISC	Active-Low, Manual Reset Input MRn is the connected within the SoC to the interval Power on Reset (POR) logic, therefore triggering the assertion of the SYSRST_OUTn pin. The POR maintains the assertion of the SYSRST_OUTn pin as long as the MRn is asserted low, and for an additional 100 ms after MRn de-assertion. **NOTE:** MRn doesn't reset the device, it only triggers the SYSRST_OUTn pin. This pin is internally pulled up.
REF_CLK_XIN	I	CMOS	XTAL_AVDD	Reference clock input from the external oscillator or input from the external crystal. Used as input to core and CPU PLLs, LCD PLL, USB PLL, and Serdes PLL.
XOUT	O	Analog	XTAL_AVDD	Feedback signal to the external crystal.
REFCLK_OUT	O	CMOS	VDDO_D	25 MHz output clock **NOTE:** This signal is multiplexed. For more information, see Section 6.1, Multi Purpose Pins Functional Summary.
SYSRST_OUTn	O OD	CMOS	VDDO_MISC	Reset request from the device to the board reset logic. **NOTE:** Requires a pull-up resistor to VDDO_MISC.
SYSRSTn	I	CMOS	VDDO_MISC	System Reset Main reset signal of the device. Used to reset all units to their initial state. **NOTE:** For reset timing, see in the device Design Guide.
M_NCAL		Calib	VDDO_M	Memory SDRAM Interface Calibration. Calibrates output NMOS driver and ODT. Connect to VDDO_M through a 931 ohm +/- 1% resistor.
M_PCAL		Calib	VDDO_M	Memory SDRAM Interface Calibration. Calibrates output PMOS driver and ODT. Connect to VSS through a 931 ohm +/- 1% resistor.
CORE_AVS_FB	O	Analog	AVS_SSCG_AVDD	Feedback voltage to the VDD regulator. **NOTE:** This pin can be required for some specific frequency configurations that are listed in Table 30, Clock Frequency Options, on page 65. If this pin's usage is not required, leave this pin unconnected.

Table 13: Miscellaneous Signals Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
CPU_AVS_FB	O	Analog	AVS_SSCG_ AVDD	Feedback voltage to the VDD_CPU regulator. **NOTE:** This pin is required for some specific frequency configurations that are listed in Table 30, Clock Frequency Options, on page 65. If this pin's usage is not required, leave this pin unconnected.
SRD_ISET		Calib		Analog reference current for the SERDES and USB interfaces. This pin must be tied to a 6.04 kilohm ±1% pull-down resistor.

2.2.11 PCI Express (PCIe) Clocks/Reset

Table 14: PCI Express (PCIe) Clocks/Reset Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
PEX0_CLK_P/N	I/O	HCSL	XTAL_AVDD	PCI Express Reference Clock 100 MHz Differential pair. As an output, each pin must be pulled down through a 49.9 ohm ±1% resistor. **NOTE:** When unused, these signals can be left unconnected.
PEX1_CLK_P/N	O	HCSL	XTAL_AVDD	PCI Express Reference Clock 100 MHz Differential pair. Each pin must be pulled down through a 49.9 ohm ±1% resistor. **NOTE:** When unused, these signals can be left unconnected.
PCIe_RSTOUTn	O	CMOS	VDDO_D	Endpoint external triggered reset. For further details, refer to the RESET section. **NOTE:** This signal is multiplexed. For more information, see Section 6.1, Multi Purpose Pins Functional Summary.
Where <n> represents the numbers of 0 thru 1				
PCIe_CLKREQ<n>	I	CMOS	VDDO_D	Endpoint request to enable/disable the reference clock. **NOTE:** These signals are multiplexed. For more information, see Section 6.1, Multi Purpose Pins Functional Summary.

2.2.12 Precise Timing Protocol (PTP) Interface

Note This interface is implemented on the Multi Purpose Pin interface. For more information, see Section 6, Pin Multiplexing. The power rail is determined by the MPP selection.

Table 15: Precise Timing Protocol (PTP) Interface Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
PTP_CLK	I	CMOS	VDDO_B or VDDO_C	PTP reference clock for time stamping.
PTP_EVENT_REQ	I	CMOS	VDDO_B or VDDO_C	PTP capturing event time.
PTP_TRIG_GEN	O	CMOS	VDDO_B or VDDO_C	PTP pulse signal.

2.2.13 Real Time Clock (RTC) Interface

Table 16: Real Time Clock (RTC) Interface Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
RTC_ALARMn	O OD	CMOS	RTC_AVDD	Active low, open drain, real time clock alarm output. Indicates when the Real Time Clock (RTC) reaches the alarm date/time. **NOTE:** This pin requires an external 100 Kohm pull-up resistor to RTC_AVDD.
RTC_XIN	I	Analog	RTC_AVDD	Crystal Clock Input.
RTC_XOUT	O	Analog	RTC_AVDD	Crystal Clock Output (feedback).

2.2.14 Serial-ATA (SATA) Interface

Table 17: Serial-ATA (SATA) Interface Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
Where <n> represents numbers 0 thru 1				
SATA<n>_PRESENT _ACTIVEn	O	CMOS	VDDO_B, VDDO_C, or VDDO_D	Disk Present Indication. **NOTE:** These signals are multiplexed. For more information, see Section 6.1, Multi Purpose Pins Functional Summary. The power rail is determined by the MPP selection.
SATA<n>_RX_P SATA<n>_RX_N	I	CML	SRD_AVDD	Receive Lane Differential pair of SATA. **NOTE:** These pins are muxed on the SERDES interface. For more information, see Section 6.5 High Speed SERDES Multiplexing.
SATA<n>_TX_P SATA<n>_TX_N	O	CML	SRD_AVDD	Transmit Lane Differential pair of SATA. **NOTE:** These pins are muxed on the SERDES interface. For more information, see Section 6.5 High Speed SERDES Multiplexing.

2.2.15 Secure Digital Input/Output (SDIO) Interface

Note

This interface is implemented on the Multi Purpose Pin interface. For more information, see Section 6, Pin Multiplexing.

Table 18: Secure Digital Input/Output (SDIO) Interface Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
SD0_CLK	O	CMOS	VDDO_C	SDIO Clock Output SD0_CMD and SD0_D[3:0] signals are referenced to this clock.
SD0_CMD	I/O	CMOS SDR	VDDO_C	SDIO Command/Response This signal is referenced to SD0_CLK. **NOTE:** This pin must be pulled up to VDDO_C through a 10 kilohm resistor.
SD0_D[3:0]	I/O	CMOS SDR	VDDO_C	SDIO Data Bus This bus is referenced to SD0_CLK. **NOTE:** This bus must be pulled up to VDDO_C through a 10 kilohm resistor.

2.2.16 SDRAM DDR3 Interface

Table 19: SDRAM DDR3 Interface Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
M_A[15:0]	O	SSTL SDR	VDDO_M	DRAM Address Outputs Provides the row address for ACTIVE commands (RASn), the column address, Auto Precharge bit (A[10]) and Burst Chop (A[12]) information for READ/WRITE commands (CASn), to determine, with the bank address bits (BA), the DRAM address. These signals are referenced to M_CLKOUT[3:0] and M_CLKOUTn[3:0] **NOTE:** When unused, can be left unconnected.
M_BA[2:0]	O	SSTL SDR	VDDO_M	DRAM Bank Address Outputs Selects one of the eight virtual banks during an ACTIVE (M_RASn), READ/WRITE (M_CASn), or PRECHARGE command. These signals are referenced to M_CLKOUT[3:0] and M_CLKOUTn[3:0]. **NOTE:** When unused, can be left unconnected.
M_BB	I	CMOS	VDDO_B, VDDO_C, or VDDO_D	DRAM Battery Backup Trigger Once asserted high, the device will immediately put the DRAM in self refresh mode. **NOTE:** This pin is implemented on the Multi Purpose Pin interface. For more information, see Section 6, Pin Multiplexing. The power rail is determined by the MPP selection.
M_CASn	O	SSTL SDR	VDDO_M	DRAM Column Address Strobe Asserted to indicate an active column address driven on the address lines. This signal is referenced to M_CLKOUT[3:0] and M_CLKOUTn[3:0].
M_CB[7:0]	I/O	SSTL DDR	VDDO_M	DRAM ECC Check Bits Driven during writes to the DRAM. Driven by the DRAM during reads. These signals are referenced to M_DQS[4] and M_DQSn[4]. **NOTE:** When unused, can be left unconnected.

Table 19: SDRAM DDR3 Interface Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
M_CLKOUT[3:0] M_CLKOUTn[3:0]	O	SSTL	VDDO_M	DRAM Differential Clock Output All address and control output signals are clocked on the crossing of the positive edge of M_CLKOUT[3:0] and negative edge of M_CLKOUTn[3:0]. The M_DQS[4:0]/M_DQSn[4:0] output (during the WRITE data phase) is referenced to the crossings of M_CLKOUT[3:0] and M_CLKOUTn[3:0] (both directions of crossing). **NOTE:** When unused, can be left unconnected. For additional details, see also Unused Interface Strapping chapter. M_CLKOUT[0] and M_CLKOUTn[0] cannot be disabled and is always driven.
M_CKE[3:0]	O	SSTL SDR	VDDO_M	DRAM Clock Enable Control Driven high to enable DRAM clock. Driven low when setting the DRAM in self Refresh Mode or Power Down mode. All M_CKE[3:0] pins are driven together (no separate self refresh or power down mode per each DRAM rank). This signal is referenced to M_CLKOUT[3:0] M_CLKOUTn[3:0] and CKn. **NOTE:** When unused, can be left unconnected.
M_CSn[3:0]	O	SSTL SDR	VDDO_M	DRAM Chip Select Control Asserted to select a specific DRAM physical rank. This signal is referenced to M_CLKOUT[3:0] M_CLKOUTn[3:0] and CKn. **NOTE:** When unused, can be left unconnected.
M_DM[4:0]	O	SSTL DDR	VDDO_M	DRAM Data Mask Driven during writes to the DRAM to mask the corresponding group of M_DQ[31:0] and M_DQS[4:0]/ M_DQSn[4:0] pins. This signal is referenced to M_DQS[4:0] and M_DQSn[4:0]. **NOTE:** When unused, can be left unconnected.
M_DQ[31:0]	I/O	SSTL DDR	VDDO_M	DRAM Data Bus Driven during writes to the DRAM. Driven by the DRAM during reads. These signals are referenced to M_DQS[4:0] and M_DQSn[4:0]. **NOTE:** For additional details with unused pins, see the section “Unused Interface Strapping”.
M_DQS[4:0] M_DQSn[4:0]	I/O	SSTL DDR	VDDO_M	DRAM Data Strobe Data strobe for input and output data. Driven during writes to the DRAM. Driven by the DRAM during reads. **NOTE:** For additional details with unused pins, see the section “Unused Interface Strapping”.

Table 19: SDRAM DDR3 Interface Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
M_ODT[3:0]	O	SSTL SDR	VDDO_M	DRAM On Die Termination Control Driven to the DRAM to turn on/off DRAM on die termination resistor. This signal is referenced to M_CLKOUT[3:0] and M_CLKOUTn[3:0]. **NOTE:** When unused, can be left unconnected.
M_RASn	O	SSTL SDR	VDDO_M	DRAM Row Address Strobe Asserted to indicate an active row address driven on the address lines. This signal is referenced to M_CLKOUT[3:0] and M_CLKOUTn[3:0].
M_RESETn	O	CMOS	VDDO_M	DRAM active low asynchronous reset. **NOTE:** When unused, can be left unconnected.
M_WEn	O	SSTL SDR	VDDO_M	DRAM Write Enable Command Active low. Asserted to indicate a WRITE command to the DRAM. This signal is referenced to M_CLKOUT[3:0] and M_CLKOUTn[3:0].
M_VTT_CTRL	O	CMOS	VDDO_C or VDDO_D	Memory VTT Power Control Controls the EN pin of a VTT power regulator that is used for switching on/off the board's termination voltage for the address/control lines. **NOTE:** This signal is implemented on the Multi Purpose Pin interface. For more information, see Section 6, Pin Multiplexing. The power rail is determined by the MPP selection.
M_DECC_ERR	O	CMOS	VDDO_C	Memory Double ECC Error Asserted upon a double ECC error detected during read data phase from DRAM. Remains active as long as the <DBit> field in the in the DDR Controller Interrupt Cause register is asserted. For further information about the DDR Controller Interrupt Cause register, refer to the device's functional specifications. **NOTE:** This signal is implemented on the Multi Purpose Pin interface. For more information, see Section 6, Pin Multiplexing. The power rail is determined by the MPP option.

2.2.17 Serial Peripheral Interface (SPI)

Note

This interface is implemented on the Multi Purpose Pin interface. For more information, see Section 6, Pin Multiplexing.

Table 20: Serial Peripheral Interface 0 (SPI0) Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
SPI0_CSn[7:0]	O	CMOS SDR	VDDO_D	SPI Chip-Select This signal is referenced to SPI0_SCK. **NOTE:** This pin must be pulled up to VDDO_D.
SPI0_MISO	I	CMOS SDR	VDDO_D	SPI Data In (Master In / Slave Out) This signal is referenced to SPI0_SCK.
SPI0_MOSI	O	CMOS SDR	VDDO_D	SPI Data Out (Master Out / Slave In) This signal is referenced to SPI0_SCK.
SPI0_SCK	O	CMOS	VDDO_D	SPI Clock Output All SPI0 signals are referenced to this clock.

Table 21: Serial Peripheral Interface 1 (SPI1) Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
SPI1_CSn[7:0]	O	CMOS SDR	VDDO_B, VDDO_D	SPI Chip-Select This signal is referenced to SPI1_SCK. **NOTE:** This pin must be pulled up to the relevant power rail.
SPI1_MISO	I	CMOS SDR	VDDO_B, VDDO_D	SPI Data In (Master In / Slave Out) This signal is referenced to SPI1_SCK.
SPI1_MOSI	O	CMOS SDR	VDDO_B, VDDO_D	SPI Data Out (Master Out / Slave In) This signal is referenced to SPI1_SCK.
SPI1_SCK	O	CMOS	VDDO_B, VDDO_D	SPI Clock Output All SPI1 signals are referenced to this clock.

2.2.18 Time Division Multiplexing (TDM) Interface

Note

This interface is implemented on the Multi Purpose Pin interface. For more information, see Section 6, Pin Multiplexing.

Table 22: Time Division Multiplexing (TDM) Interface Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
TDM_DRX	I	CMOS SDR	VDDO_C	Pulse Code Modulation (PCM) Input Data This signal is referenced to TDM_PCLK.
TDM_DTX	O	CMOS SDR	VDDO_C	Pulse Code Modulation (PCM) Output Data This signal is referenced to TDM_TX_PCLK.
TDM_INTn[6:0]	I	CMOS	VDDO_C	Interrupt input from the SLIC device.
TDM_INTn[7]			VDDO_D	
TDM_RSTn	O	CMOS	VDDO_C	SLIC asynchronous reset signal.
TDM_FSYNC	I/O	CMOS SDR	VDDO_C	Frame Synchronous Signal Driven by the device if configured as Frame master. Input to the device (driven by an external component) if configured as Frame slave. This signal is referenced to TDM_PCLK.
TDM_PCLK	I/O	CMOS	VDDO_C	Pulse Code Modulation (PCM) Bit Clock Driven by the device if configured as PCLK master. Input to the device (driven by an external component) if configured as PCLK slave. TDM_FSYNC and TDM_DRX are referenced to this clock.

2.2.19 Universal Asynchronous Receiver Transmitter (UART) Interface

Note The following are dedicated pins: UA0_RXD, UA1_RXD, UA0_TXD, and UA1_TXD. The remaining signals are implemented on the Multi Purpose Pin interface. For more information, see Section 6, Pin Multiplexing.

Table 23: Universal Asynchronous Receiver Transmitter (UART) Interface Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
UA0_CTS UA1_CTS	I	CMOS	VDDO_D	UART Clear To Send **NOTE:** UART<n>_CTS pins are implemented on the Multi Purpose Pin interface. For more information, see Section 6, Pin Multiplexing.
UA2_CTS UA3_CTS			VDDO_D	
UA0_RTS UA1_RTS	O	CMOS	VDDO_D	UART Request To Send **NOTE:** UART<n>_RTS pins are implemented on the Multi Purpose Pin interface. For more information, see Section 6, Pin Multiplexing.
UA2_RTS UA3_RTS			VDDO_D	
UA0_RXD UA1_RXD	I	CMOS	VDDO_MISC	UART Receive Data **NOTE:** UART 2/3 RXD pins are implemented on the Multi Purpose Pin interface. For more information, see Section 6, Pin Multiplexing.
UA2_RXD UA3_RXD			VDDO_D	
UA0_TXD UA1_TXD	O	CMOS	VDDO_MISC	UART Transmit Data **NOTE:** UA0_TXD/UA1_TXD have an integrated pull-down resistor. UA2_TXD/UA3_TXD pins are implemented on the Multi Purpose Pin interface. For more information, see Section 6, Pin Multiplexing.
UA2_TXD UA3_TXD			VDDO_D	

2.2.20 USB 2.0 Interface

Note When unused, can be left unconnected.

Table 24: USB 2.0 Interface Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
Where <n> represents numbers 0 thru 2				
USB<n>_DP USB<n>_DM	I/O	CML	USB_AVDD and USB_AVDDL	USB 2.0 Data Differential Pair. **NOTE:** USB1_DP/DM pins are actually a CMOS pin type when configured to the Low Speed mode.

2.2.21 SERDES Port Interface

Note

The SERDES interface supports the following modes: PCI Express, SATA, USB, SGMII, DR-SGMII, QSGMII, and sETM.

Table 25: SERDES Port Interface Pin Description

Pin Name	I/O	Pin Type	Power Rail	Description
Where <n> represents numbers 0 thru 6				
SRD<n>_RX_N	I	CML	SRD_AVDD	Receive data: Differential analog input of SERDES Port <n>.
SRD<n>_RX_P	I	CML	SRD_AVDD	Receive data: Differential analog input of SERDES Port <n>.
SRD<n>_TX_N	O	CML	SRD_AVDD	Transmit data: Differential analog output of SERDES Port <n>.
SRD<n>_TX_P	O	CML	SRD_AVDD	Transmit data: Differential analog output of SERDES Port <n>.

2.2.22 Reserved/Not Connected Pins

Pin Name	Description
RSVD_VSS	Reserved Must be connected to VSS ground.
RSVD_VDD_CPU	Reserved. Must be connected to VDD_CPU power.
RSVD_VDD	Reserved. Must be connected to VDD power.
RSVD_NC	Reserved Must be not connected.
NC	Not connected.

2.2.23 Power Supply Pins

Table 26 provides the voltage levels for the various interface pins. These also include the analog power supplies for the PLLs or PHYS.

Table 26: Power Supply Pins

Pin Name	Pin Type	Description
VDD	Power	0.9V core voltage
VDD_CPU	Power	1.05/1.1V CPU core and CPU subsystem voltage
VDDO_MISC	Power	3.3V I/O supply voltage for the TWSI0/1, UART0/1, and JTAG interfaces, and the following signals: • SYSRSTn • SYSRST_OUTn • MRn • CDRn
VDDO_M	Power	1.35/1.5/1.8V I/O supply voltage for the SDRAM interface
VDDO_A	Power	1.8/2.5/3.3V I/O supply voltage for the SMI interface and MPP[11:0]
VDDO_B	Power	1.8/2.5/3.3V I/O supply voltage for the MPP[23:12]
VDDO_C	Power	1.8V or 3.3V I/O supply voltage for the MPP[35:24]
VDDO_D	Power	3.3V I/O supply voltage for the SPI interface and MPP[47:36]
VDDO_DEV	Power	1.8V or 3.3V I/O supply voltage for the Device Bus interface and MPP[48]
VDDO_FPD	Power	1.8V I/O supply voltage for Flat Panel Display interface
VHV	Power	1.8V I/O supply voltage for eFuse Connect the power supply to the VHV ball only when burning the eFuse. When reading the eFuse and in all other times, disconnect the power supply from the VHV ball. The VHV is left floating.
CORE_TDM_PLL_AVDD	Analog Power	1.8V Core PLL and TDM PLL quiet power supply **NOTE:** Implement the PLL filter as described in the *ARMADA*® XP Highly Integrated Multi-Core ARMv7 Based System-on-Chip Processors *Design Guide*.
CPU_PLL_AVDD	Analog Power	1.8V CPU PLL quiet power supply **NOTE:** Implement the PLL filter as described in the *ARMADA*® XP Highly Integrated Multi-Core ARMv7 Based System-on-Chip Processors *Design Guide*.
USB_AVDD	Analog Power	3.3V USB 2.0 PHY quiet power supply **NOTE:** See the *ARMADA*® XP Highly Integrated Multi-Core ARMv7 Based System-on-Chip Processors *Design Guide* for power supply filtering recommendations.
USB_AVDDL	Analog Power	1.8V USB 2.0 PHY quiet power supply **NOTE:** See the *ARMADA*® XP Highly Integrated Multi-Core ARMv7 Based System-on-Chip Processors *Design Guide* for power supply filtering recommendations.
SRD_AVDD	Analog Power	1.8V SERDES quiet power supply **NOTE:** See the *ARMADA*® XP Highly Integrated Multi-Core ARMv7 Based System-on-Chip Processors *Design Guide* for power supply filtering recommendations.
RTC_AVDD	Analog Power	3.0V (via the battery) or 3.3V (via the board) RTC interface voltage

Table 26: Power Supply Pins (Continued)

Pin Name	Pin Type	Description
XTAL_AVDD	Analog Power	1.8V XTAL and PCI Express clock outputs quiet power supply **NOTE:** See the *ARMADA*® XP Highly Integrated Multi-Core ARMv7 Based System-on-Chip Processors *Design Guide* for power supply filtering recommendations.
AVS_SSCG_AVDD	Analog Power	1.8V CORE_AVS, CPU_AVS, and the Spread Spectrum Clock Generator (SSCG) quiet power supply
VSS	Ground	Ground
XTAL_AVSS	Analog Ground	XTAL quiet ground
CPU_PLL_AVSS	Analog Ground	CPU PLL quiet ground
CORE_TDM_PLL_ AVSS	Analog Ground	TDM PLL quiet ground
AVS_SSCG_AVSS	Analog Ground	CORE_AVS, CPU_AVS, and SSCG quiet ground

2.3 Internal Pull-up and Pull-down Pins

Table 27 and Table 28 lists the pins of the device package that are connected to internal pull-up and pull-down resistors. When these pins are Not Connected (NC) on the system board, these resistors set the default value for input and sample at reset configuration pins.

The internal pull-up and pull-down resistor value is 50 kΩ. An external resistor with a lower value can override this internal resistor.

For the pin location, see the attached Excel file in Section 4, MV78230 Pin Map, Pin List, and Package Trace Lengths, on page 63.

Table 27: Internal Pull-up Pins

Pin Name	Pin Name	Pin Name	Pin Name	Pin Name
CDRn	JT_TDI	MPP[14]	MPP[29]	MPP[42]
DEV_AD[3]	JT_TMS_CORE	MPP[15]	MPP[30]	MPP[43]
DEV_AD[5]	JT_TMS_CPU	MPP[16]	MPP[31]	MPP[44]
DEV_AD[7]	GE_MDIO	MPP[18]	MPP[32]	MPP[45]
DEV_AD[8]	MPP[0]	MPP[19]	MPP[33]	MPP[46]
DEV_AD[9]	MPP[3]	MPP[20]	MPP[34]	MPP[47]
DEV_BOOTCSn	MPP[6]	MPP[21]	MPP[35]	MRn
DEV_CSn[0]	MPP[7]	MPP[22]	MPP[36]	TWSI0_SCK
DEV_CSn[1]	MPP[8]	MPP[23]	MPP[37]	TWSI0_SDA
DEV_CSn[2]	MPP[9]	MPP[25]	MPP[38]	TWSI1_SCK
DEV_CSn[3]	MPP[10]	MPP[26]	MPP[39]	TWSI1_SDA
DEV_OEn	MPP[11]	MPP[27]	MPP[40]	
DEV_Wen[0]	MPP[13]	MPP[28]	MPP[41]	

Table 28: Internal Pull-down Pins

Pin Name	Pin Name
DEV_A[0]	DEV_ALE[1]
DEV_A[1]	DEV_READYn
DEV_A[2]	DEV_WEn[1]
DEV_AD[0]	GE_MDC
DEV_AD[1]	JT_CLK
DEV_AD[2]	JT_RSTn
DEV_AD[4]	MPP[1]
DEV_AD[6]	MPP[2]
DEV_AD[10]	MPP[4]
DEV_AD[11]	MPP[5]
DEV_AD[12]	MPP[12]
DEV_AD[13]	MPP[17]
DEV_AD[14]	MPP[24]
DEV_AD[15]	UA0_TXD
DEV_ALE[0]	UA1_TXD

3 Unused Interface Strapping

Table 29 lists the signal strapping for systems in which some of the MV78230 interfaces are unused.

Table 29: Unused Interface Strapping

Unused Interface	Strapping
Device	Connect VDDO_DEV to 1.8V or 3.3V. The Device bus signals can be left unconnected.
SDRAM	If there are unused clock pairs: • Leave the unused pair unconnected. • In the DDR Controller Control (Low) register (Offset: 0x1404), set <Clk1Drv> (bit[12]),<Clk2Drv> (bit[13]), or <Clk3Drv> (bit[15]) to 0 (high-Z). **NOTE:** M_CLKOUT[0] and M_CLKOUTn[0] cannot be disabled and are always driven. The following SDRAM signals can be left unconnected when unused: • M_A • M_BA • M_CB • M_DM • M_DQ • M_DQS/DQSn • M_CSn • M_ODT • M_CKE
Ethernet SMI	GE_MDIO must be pulled up with a 1–4.7 kilohm resistor to VDDO_A.
I^2C	Unused TWSI<n>_SDA and TWSI<n>_SCK signals must be pulled up with a 1–4.7 kilohm resistor to VDDO_MISC.
JTAG	If the JT_TMS_CORE is: • Not connected: There is no need for an external pull-up. • Connected: JT_TMS_CORE must kept high if unused (i.e. pulled up).
UART	Unused UA<n>_RXD signals must be pulled up with a 1–4.7 kilohm resistor to VDDO_MISC. Unused UA<n>_TXD signals can be left unconnected.
MPP	Configure unused signals as GPIO outputs. No external pullups are required. Leave the power rail driving the unused MPPs connected as follows: • Leave VDDO_A connected to 1.8V or 2.5V or 3.3V. • Leave VDDO_B connected to 1.8V or 2.5V or 3.3V. • Leave VDDO_C connected to 1.8V or 3.3V. • Leave VDDO_D connected to 3.3V. • Leave VDDO_DEV connected to 1.8V or 3.3V.

Table 29: Unused Interface Strapping

Unused Interface	Strapping
USB	Unused USB<n>_DP and USB<n>_DM signals can be left unconnected. Power down any unused USB ports via the register configuration. If all the USB ports are unused: • Discard the power filter. • Connect USB_AVDD to VSS. • Connect USB_AVDDL to VSS.
SERDES	Unused SRD<n>_TX_P/N and SRD<n>_RX_P/N signals can be left unconnected. Power down any unused SERDES port via register configuration. If all the SERDES ports are unused: • Discard the power filter. • Connect SRD_AVDD to VSS.
PCI Express Clocks	Unused signals can be left unconnected. To power down the PECL receiver, write 0 to the Ana Grp Config register (offset: 0x0001847C) <PU_CLK> bit[10]. If the PCIe_CLKREQ pins are not required, the relevant MPP pins must be configured to a different mode. For further information, see Section 6.1, Multi Purpose Pins Functional Summary, on page 67.
Flat Panel Display	Unused signals can be left unconnected If all signals in this interface are unused, VDDO_FPD can also be left unconnected.
RTC	RTC_AVDD, RTC_XIN, and RTC_XOUT can be left unconnected.
RTC Alarm	RTC_ALARMn can be left unconnected. If unused, the external pull-up can be removed. Configure the alarm register to 32'b0 and then the clear control register field to 1.
Adaptive Voltage Scaling (AVS)	CPU_AVS_FB and CORE_AVS_FB can be left unconnected. AVS_SSCG_AVDD and AVS_SSCG_AVSS must be left connected. Discard the power filter only if all of the following pins are not in use: • CPU AVS • CORE AVS • SSCG

4 MV78230 Pin Map, Pin List, and Package Trace Lengths

The MV78230 pin lists and package trace lengths are provided as Excel file attachments.

To open the attached Excel pin list file, double-click the pin icon below:

MV78230 Pin Map and Pin List

Note

File attachments are only supported by Adobe Reader 6.0 and above.

To download the latest version of free Adobe Reader go to http://www.adobe.com.

5 Clocking

5.1 Clock Domain

The MV78230 has multiple clock domains:

- PCLK0, PCLK1: Marvell® Core Processor ARM CPU clocks—up to 1.6 GHz[1]
- NBCLK: The Coherent Fabric clock. Also used as the L2 cache clock—up to 800 MHz[1]
- HCLK: The SDRAM controller internal clock—up to 400 MHz[1]
- DRAMCLK: The SDRAM interface clock—up to 800 MHz[1]
- TCLK: The device's core clock—250 MHz.
- DEV_CLK_OUT: Up to TCLK/4
- PCI Express clock:
  - Runs at 250 MHz when configured to Gen1.1
  - Runs at 500 MHz when configured to Gen2.0
- GbE ports clock:
  - 125 MHz for 1000 Mbps
  - 25 MHz for 100 Mbps
  - 2.5 MHz for 10 Mbps
- SMI clock: Up to TCLK/8
- SATA clock: Runs at 150 MHz
- USB clock: Runs up to 480 MHz (at High Speed mode)
- UART clock: Up to TCLK frequency divided by 16
- SPI clock: Up to 50 MHz
- I^2C clock: Up to 100 kHz
- LCD clock: Up to 65 MHz for both parallel and LVDS interfaces
- SDIO clock: Up to 50 MHz
- TDM clock: Up to 8.192 MHz

5.1.1 Clock Ratios

The supported PCLK0-to-NBCLK clock ratios are 1:1, 1:2, 1:3 and 2:3.

The supported NBCLK-to-HCLK clock ratios are 1:N and 2:N.

The supported HCLK-to-DRAMCLK clock ratios are 1:1 and 1:2. According to this defined ratio, SW needs to configure the DRAM controller's working mode to be 1:1 or 1:2.

The supported PCLK0-to-PCLK<n> clock ratios are 1:1, 1:2 and 1:3.

1. Controlled by the Spread Spectrum Clock Generator (SSCG). For details, see Section 5.3, Spread Spectrum Clock Generator (SSCG), on page 66.

The PCLK0-to-NBCLK ratios, NBCLK-to-HCLK ratios, and HCLK-to-DRAMCLK ratios are determined via reset strapping. Table 30 summarizes the possible frequencies of the various domains as a function of the selected CPU speed.

Note

- To set up target clock frequencies, first select the target CPU speed via CPU0 Clock Frequency Select in Table 36, Reset Configuration Pins, on page 81 reset straps, and then configure the Fabric Frequency Options reset straps to the specified index according to Table 30.
- The PCLK0 frequency specifies the target frequency of CPU0. The other CPU core default clock frequency is set to the selected NBCLK frequency. As part of the CPU0 boot flow, and in case a different speed target is required for the other core, the software needs to reconfigure the target frequencies for the other core through the software.
- PCLK0 frequency must always be greater or equal to PCLK<n>.

5.2 Clock Frequency Configuration Options

Table 30 lists the various frequency options and the supported CPU0 speeds that may be configured via the <CPU0 Clock Frequency Select> field in Non-Core and Core Voltages (Table 35 p. 84) reset straps.

Table 30: Clock Frequency Options

NOTE: The Fabric Frequency Configuration Index column applies to the reset strap vector represented by the <Fabric Frequency Options> field in Non-Core and Core Voltages (Table 35 p. 84).

CPU0 Clock Frequency (PCLK) [MHz]	NBCLK [MHz]	HCLK [MHz]	DRAMCLK [MHz]	Fabric Frequency Configuration Index
800	400	200	400	5
1066	533	267	533	5
1200	600	300	600	5
1200	600	200	400	9
1333	667	333	667	5
1500[1]	750	375	750	5
1500[2]	750	250	500	9
1600[2]	800	266	533	9
1600[2]	800	320	640	10
1600[2]	800	400	800	5

1. The CPU_AVS_FB pin must be used with this clock frequency. For further information on AVS usage, see the *MV78230/78x60 Design Guide* (MV-S301878-00).
2. The CORE_AVS_FB and CPU_AVS_FB pins must be used with this clock frequency. For further information on AVS usage, see the *MV78230/78x60 Design Guide*.

5.3 Spread Spectrum Clock Generator (SSCG)

The Spread Spectrum Clock Generator (SSCG) may be used to generate the spread spectrum clock for the PLL input. See <SSCG Disable> in Table 36, Reset Configuration Pins, on page 81, for SSCG enable/disable configuration settings.

The SSCG block can be configured to perform up spread, down spread and center spread.

The modulation frequency is configurable. The typical frequency is 30 kHz.

The spread percentage can also be configured up to 1%.

For additional details, see the SSCG Configuration Register description in the device's *Functional Specifications*.

6 Pin Multiplexing

6.1 Multi Purpose Pins Functional Summary

The device contains 49 Multi Purpose Pins (MPP).

Each pin can be assigned a different functionality through the configuration of the MPP Control register. These configuration options include:

- GPIO: General Purpose In/Out Port, each of the 49 MPP pins may be configured as a GPIO signals—see the General Purpose I/O Port section in the device's *Functional Specifications*.
- DEV_BURSTn/DEV_LASTn: Device Bus interface signals—see the Device Bus section in the device's *Functional Specifications*.
- NF_RBn: Ready/Busy indication for the NAND Flash interface—See Table 6, Device Bus/NAND Flash Interface Pin Assignments, on page 33
- DEV_CLK_OUT: Outputs a divided core clock (TCLK)—see the Device Bus section in the device's *Functional Specifications*.
- TDM_INTn[7:0], TDM_RSTn, TDM_PCLK, TDM_FSYNC, TDM_DRX, TDM_DTX: TDM (Voice) interface signals—see the TDM section in the device's *Functional Specifications*.
- SPI<n>_CS[7:0]n, SPI<n>_SCK, SPI<n>_MISO, SPI<n>_MOSI (n= 0 thru 1): SPI (Serial Peripheral Interface) signals—see the SPI section in the device's *Functional Specifications*.
- UA0_CTSn, UA0_RTSn, UA1_CTSn, UA1_RTSn, UA2_RXD, UA2_TXD, UA2_CTSn, UA2_RTSn, UA3_RXD, UA3_TXD, UA3_CTSn, UA3_RTSn: UART pins—see the UART section in the device's *Functional Specifications*.
- I^2C signals: TWSI0/1_SDA, TWSI0/1_SCK
- SD0_CLK, SD0_CMD, SD0_D[3:0]: SDIO interface—see the SDIO section in the device's *Functional Specifications*.
- PTP_EVENT_REQ, PTP_TRIG_GEN, PTP_CLK: Precise Timing Protocol signals—see the Gigabit Ethernet Controller section in the device's *Functional Specifications*.
- GE<n>_TXCLKOUT, GE<n>_TXD[3:0], GE<n>_TXCTL, GE<n>_RXD[3:0], GE<n>_RXCTL, GE<n>_RXCLK (n= 0 thru 1): Ethernet RGMII signals for ports 0 and 1 —see the Gigabit Ethernet Controller section in the device's *Functional Specifications*.
- GE0_TXD[7:4], GE0_TXCLK, GE0_COL, GE0_RXERR, GE0_CRS, GE0_RXD[7:4]: GbE port0 signals when configured to GMII/MII interface—see the Gigabit Ethernet Controller section in the device's *Functional Specifications*. Also, see Table 31, Gigabit Ethernet Pins Multiplexing for port mode selections.
- SATA<n>_PRESENT_ACTIVEn (n= 0 thru 1): Combined SATA active and SATA present indications—see the Serial-ATA section in the device's *Functional Specifications*.
- M_BB: SDRAM battery backup trigger—see the SDRAM Self Refresh section in the device's *Functional Specifications*.
- M_VTT_CTRL, M_DECC_ERR: VTT power regulator control and asserted signal upon double ECC error detection during the read data phase from DRAM. See the SDRAM section the device's *Functional Specifications.*
- LCD_D[23:0], LCD_HSYNC, LCD_VSYNC, LCD_PWM, LCD_CLK, LCD_E, LCD_VGA_HSYNC, LCD_VGA_VSYNC: LCD interface signals—see Table 32, LCD Interface Modes, on page 70 for pin allocation and the LCD section in the device's *Functional Specifications*.

- LCD_EXT_REF_CLK: Optional reference clock for the LCD interface. See the LCD section in the device's *Functional Specifications*.
- REFCLK_OUT: Stable 25 MHz output clock from the device. Can be used as reference input clock for other components on the board.
- PCIe_CLKREQ0, PCIe_CLKREQ1: When the port is configured as RC, endpoints may drive the clock request to high. This causes the PCI clock request to be gated. During normal operations, the clock request should be driven low, which means the PCI clock is not held. For further information, see the PCI Express section in the device's *Functional Specifications*.
- PCIe_RSTOUTn: PCIe reset out indication. See the PCI Express section in the device's *Functional Specifications*.

The attached Excel file lists each MPP pins' functionality as determined by the MPP Multiplex registers. For more information, refer to the Pins Multiplexing Interface Registers section in the device's *Functional Specifications*.

To open the attached Excel MPP map file, double-click the pin icon below:

MV78230 MPP Map

Note

File attachments are only supported by Adobe Reader 6.0 and above.

To download the latest version of free Adobe Reader go to http://www.adobe.com.

6.2 Multi Purpose Pins Power Segments

The different power segments for each of the MPP pins is listed in the Power Pins Description table in Table 26, Power Supply Pins, on page 57.

The voltage level of VDDO_C and VDDO_DEV is determined by a reset strap. The voltage level of VDDO_A and VDDO_B is 3.3V by default, with a register configurable option to 1.8/2.5V or 2.5V. Refer to the System Considerations section in the *ARMADA*® XP Highly Integrated Multi-Core ARMv7 Based System-on-Chip Processors *Functional Specifications* for more information about voltage setting.

6.3 Multi Purpose Pins Functional Considerations

When configuring MPP pins note the following issues, also refer to the attached Multi Purpose Pin Functional Summary Table:

- For MPPs assigned as NOR or SPI flash, the wake-up mode after reset depends on the Boot mode (see the Boot Device Type Selection field in Table 36, Reset Configuration Pins, on page 81).
- There are a few options for the boot device as listed in Table 36. The value set in field Boot Device Type Selection determines the type of the boot select during reset. The values set in Table 36 effect the default value of <MPPSel> fields in the MPP Control registers.
  - If Boot Device Type Selection is set to 0x3, MPP[39:36] pins wake up as SPI flash signals.
- UART0, UART1, UART2, and UART3 signals are duplicated on some MPP pins. The UART0, UART1, UART2, or UART3 signals must not be configured to more than one MPP option.

- All other MPP interface pins wake up after reset in 0x0 mode (GPIO). By default, these pins are set to Data Output disabled (Tri-State). Therefore, these MPPs are in fact inputs.
- Some of the MPP pins are sampled during SYSRSTn de-assertion to set the device configuration. These pins must be driven to the correct value during reset (see Table 36, Reset Configuration Pins, on page 81).
- Pins that are left as GPIO and are not connected must be configured as outputs via the GPIO registers after SYSRSTn de-assertion (see General Purpose I/O section in the *ARMADA*® XP Highly Integrated Multi-Core ARMv7 Based System-on-Chip Processors *Functional Specifications*).

6.4 Gigabit Ethernet Pins Multiplexing on the MPP

There are two Gigabit Ethernet ports that are multiplexed on the MPP pins.

- Each of these Gigabit Ethernet ports can operate in RGMII mode.
- Port 0 also supports GMII/MII signaling.

The device also contains a SERDES interface that can be used as SGMII interfaces for port 0, 1, 2. Once a port is configured as an SGMII port, it cannot be selected as an RGMII/GMII/MII port on the MPP pins. The SGMII interface may be selected on various SERDES options (see Section 6.7, High-Speed SERDES Multiplexing, on page 74. Do not select more than one SERDES option for the same GbE port.

Table 31 lists the Gigabit Ethernet multiplexing pin configuration options for Port0 and Port1, when the port is not used as SGMII.

Table 31: Gigabit Ethernet Pins Multiplexing

MPP #	GE0 GMII, GE1 is SGMII or N/A	GE0 MII, GE1 is SGMII or N/A	GE0 RGMII, GE1 either SGMII or N/A	GE1 RGMII, GE0 either SGMII or N/A	Both GE0 and GE1 are RGMII
MPP[0]	GE0_TXCLKOUT (out)	N/A	GE0_TXCLKOUT (out)	N/A	GE0_TXCLKOUT (out)
MPP[1]	GE0_TXD[0] (out)	GE0_TXD[0] (out)	GE0_TXD[0] (out)	N/A	GE0_TXD[0] (out)
MPP[2]	GE0_TXD[1] (out)	GE0_TXD[1] (out)	GE0_TXD[1] (out)	N/A	GE0_TXD[1] (out)
MPP[3]	GE0_TXD[2] (out)	GE0_TXD[2] (out)	GE0_TXD[2] (out)	N/A	GE0_TXD[2] (out)
MPP[4]	GE0_TXD[3] (out)	GE0_TXD[3] (out)	GE0_TXD[3] (out)	N/A	GE0_TXD[3] (out)
MPP[5]	GE0_TXEN (out)	GE0_TXEN (out)	GE0_TXCTL (out)	N/A	GE0_TXCTL (out)
MPP[6]	GE0_RXD[0] (in)	GE0_RXD[0] (in)	GE0_RXD[0] (in)	N/A	GE0_RXD[0] (in)
MPP[7]	GE0_RXD[1] (in)	GE0_RXD[1] (in)	GE0_RXD[1] (in)	N/A	GE0_RXD[1] (in)
MPP[8]	GE0_RXD[2] (in)	GE0_RXD[2] (in)	GE0_RXD[2] (in)	N/A	GE0_RXD[2] (in)
MPP[9]	GE0_RXD[3] (in)	GE0_RXD[3] (in)	GE0_RXD[3] (in)	N/A	GE0_RXD[3] (in)
MPP[10]	GE0_RXDV (in)	GE0_RXDV (in)	GE0_RXCTL (in)	N/A	GE0_RXCTL (in)
MPP[11]	GE0_RXCLK (in)	GE0_RXCLK (in)	GE0_RXCLK (in)	N/A	GE0_RXCLK (in)
MPP[12]	GE0_TXD[4] (out)	N/A	N/A	GE1_TXCLKOUT (out)	GE1_TXCLKOUT (out)

Table 31: Gigabit Ethernet Pins Multiplexing (Continued)

MPP #	GE0 GMII, GE1 is SGMII or N/A	GE0 MII, GE1 is SGMII or N/A	GE0 RGMII, GE1 either SGMII or N/A	GE1 RGMII, GE0 either SGMII or N/A	Both GE0 and GE1 are RGMII
MPP[13]	GE0_TXD[5] (out)	N/A	N/A	GE1_TXD[0] (out)	GE1_TXD[0] (out)
MPP[14]	GE0_TXD[6] (out)	N/A	N/A	GE1_TXD[1] (out)	GE1_TXD[1] (out)
MPP[15]	GE0_TXD[7] (out)	N/A	N/A	GE1_TXD[2] (out)	GE1_TXD[2] (out)
MPP[16]	N/A	GE0_TXCLK (in)	N/A	GE1_TXD[3] (out)	GE1_TXD[3] (out)
MPP[17]	GE0_COL (in)	GE0_COL (in)	N/A	GE1_TXCTL (out)	GE1_TXCTL (out)
MPP[18]	GE0_RXERR (in)	GE0_RXERR (in)	N/A	GE1_RXD[0] (in)	GE1_RXD[0] (in)
MPP[19]	GE0_CRS (in)	GE0_CRS (in)	N/A	GE1_RXD[1] (in)	GE1_RXD[1] (in)
MPP[20]	GE0_RXD[4] (in)	N/A	N/A	GE1_RXD[2] (in)	GE1_RXD[2] (in)
MPP[21]	GE0_RXD[5] (in)	N/A	N/A	GE1_RXD[3] (in)	GE1_RXD[3] (in)
MPP[22]	GE0_RXD[6] (in)	N/A	N/A	GE1_RXCTL (in)	GE1_RXCTL (in)
MPP[23]	GE0_RXD[7] (in)	N/A	N/A	GE1_RXCLK (in)	GE1_RXCLK (in)

Note When using GbE signals on MPPs, all relevant GbE signals (except those marked as N/A) must be implemented. For example, if using MII, and the chosen PHY does not have an MII_RXERR out signal, the GE0_RXERR on the MPP pin must still be configured accordingly and must have a pull-down resistor.

6.5 LCD Pin Multiplexing on the MPP

The LCD interface is multiplexed on MPP[28:0] (see Table 32). Not all LCD panels require the full 29 pins. Any pins that are not used as LCD pins, may be used for different pin assignment according to the options shown in the attached Excel file (see Section 6.1, Multi Purpose Pins Functional Summary, on page 67). The supported LCD interface modes are listed in Table 32.

Table 32: LCD Interface Modes

MPP Pin	LCD Pin	Mode 0	Mode 1	Mode 2	Mode 3
		Dumb Panel 24-bit Color 8:8:8	Dumb Panel 18-bit Color 6:6:6	Dumb Panel 16-bit Color 5:6:5	Dumb Panel 12-bit Color 4:4:4
MPP[0]	LCD_D[0]	Red[0]	Red[2]	Red[3]	Red[4]
MPP[1]	LCD_D[1]	Red[1]	Red[3]	Red[4]	Red[5]
MPP[2]	LCD_D[2]	Red[2]	Red[4]	Red[5]	Red[6]
MPP[3]	LCD_D[3]	Red[3]	Red[5]	Red[6]	Red[7]

Table 32: LCD Interface Modes (Continued)

MPP Pin	LCD Pin	Mode 0	Mode 1	Mode 2	Mode 3
		Dumb Panel 24-bit Color 8:8:8	Dumb Panel 18-bit Color 6:6:6	Dumb Panel 16-bit Color 5:6:5	Dumb Panel 12-bit Color 4:4:4
MPP[4]	LCD_D[4]	Red[4]	Red[6]	Red[7]	Green[4]
MPP[5]	LCD_D[5]	Red[5]	Red[7]	Green[2]	Green[5]
MPP[6]	LCD_D[6]	Red[6]	Green[2]	Green[3]	Green[6]
MPP[7]	LCD_D[7]	Red[7]	Green[3]	Green[4]	Green[7]
MPP[8]	LCD_D[8]	Green[0]	Green[4]	Green[5]	Blue[4]
MPP[9]	LCD_D[9]	Green[1]	Green[5]	Green[6]	Blue[5]
MPP[10]	LCD_D[10]	Green[2]	Green[6]	Green[7]	Blue[6]
MPP[11]	LCD_D[11]	Green[3]	Green[7]	Blue[3]	Blue[7]
MPP[12]	LCD_D[12]	Green[4]	Blue[2]	Blue[4]	N/A
MPP[13]	LCD_D[13]	Green[5]	Blue[3]	Blue[5]	N/A
MPP[14]	LCD_D[14]	Green[6]	Blue[4]	Blue[6]	N/A
MPP[15]	LCD_D[15]	Green[7]	Blue[5]	Blue[7]	N/A
MPP[16]	LCD_D[16]	Blue[0]	Blue[6]	N/A	N/A
MPP[17]	LCD_D[17]	Blue[1]	Blue[7]	N/A	N/A
MPP[18]	LCD_D[18]	Blue[2]	N/A	N/A	N/A
MPP[19]	LCD_D[19]	Blue[3]	N/A	N/A	N/A
MPP[20]	LCD_D[20]	Blue[4]	N/A	N/A	N/A
MPP[21]	LCD_D[21]	Blue[5]	N/A	N/A	N/A
MPP[22]	LCD_D[22]	Blue[6]	N/A	N/A	N/A
MPP[23]	LCD_D[23]	Blue[7]	BIAS_OUT (32 kHz)	BIAS_OUT (32 kHz)	BIAS_OUT (32 kHz)
MPP[24]	LCD_HSYNC	H_Sync	H_Sync	H_Sync	H_Sync
MPP[25]	LCD_VSYNC	V_Sync	V_Sync	V_Sync	V_Sync
MPP[26]	LCD_CLK	Pixel_Clock	Pixel_Clock	Pixel_Clock	Pixel_Clock
MPP[27]	LCD_E	Data Enable	Data Enable	Data Enable	Data Enable
MPP[28]	LCD_PWM	BIAS_OUT (32 kHz)	N/A	N/A	N/A

Note When a touch panel SPI interface is required, use one of the available SPI interface configuration options on the MPP pins. The SPI interface may be configured through MPP[47:36].

6.6 Serialized LVDS Transmitter

The integrated serialized LVDS transmitter supports the following features at up to 65 MSPS:

- 18-bit or 24-bit per pixel (three or four transmit differential data/control lanes)
- Transmit differential clock lane (driven by the LCD_CLK output)
- Two data serialization options in 24-bit per pixel mode
- Option to disable serialization and force constant zero output in data/control lanes
- Configurable tick delay on data/control lanes relative to clock lane
- Option to disable the fast reference clock when LVDS is not in use
- Option to power down LVDS pads when not in use

The LVDS and parallel RGB interface are usually not used together. When LVDS is not used, Marvell recommends powering down the pads and disabling serialization for power saving.

Figure 5 displays the connectivity between the LCD unit and the LVDS.

Figure 5: Pin Multiplexing and Connectivity Diagram

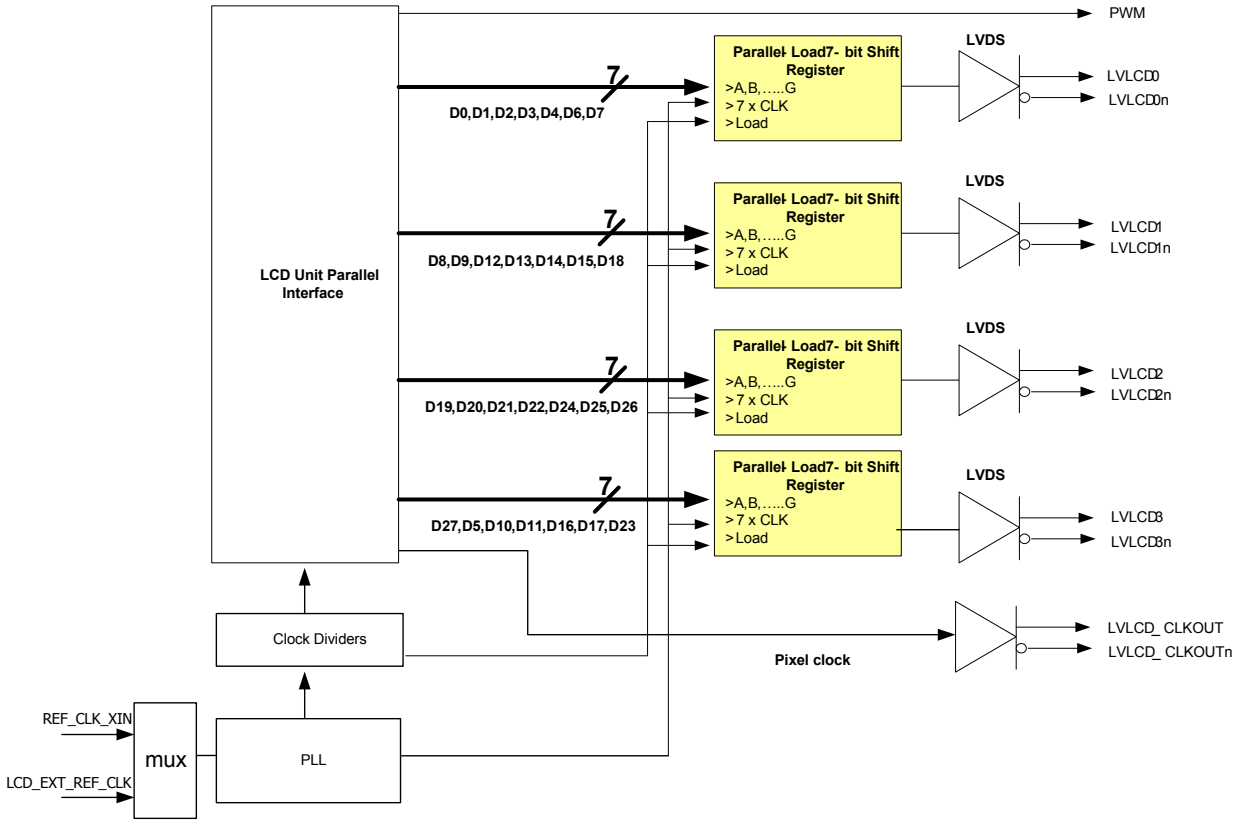


Table 33 lists the connectivity between the LCD and the LVDS options.

Table 33: LCD Connectivity to LVDS

Pin	24 BPP Controller and Panel			18 BPP Controller and Panel	
	Mode0 Dumb Panel 24-bit Color 8:8:8	LVDS Option1	LVDS Option2	Mode1 Dumb Panel 18-bit Color 6:6:6	LVDS Option1
0	Red[0] (LSB)	D0	D27	Red[2] (LSB)	D0
1	Red[1]	D1	D5	Red[3]	D1
2	Red[2]	D2	D0	Red[4]	D2
3	Red[3]	D3	D1	Red[5]	D3
4	Red[4]	D4	D2	Red[6]	D4
5	Red[5]	D6	D3	Red[7] (MSB)	D6
6	Red[6]	D27	D4	Green[2] (LSB)	D7
7	Red[7] (MSB)	D5	D6	Green[3]	D8
8	Green[0] (LSB)	D7	D10	Green[4]	D9
9	Green[1]	D8	D11	Green[5]	D12
10	Green[2]	D9	D7	Green[6]	D13
11	Green[3]	D12	D8	Green[7] (MSB)	D14
12	Green[4]	D13	D9	Blue[2] (LSB)	D15
13	Green[5]	D14	D12	Blue[3]	D18
14	Green[6]	D10	D13	Blue[4]	D19
15	Green[7] (MSB)	D11	D14	Blue[5]	D20
16	Blue[0] (LSB)	D15	D16	Blue[6]	D21
17	Blue[1]	D18	D17	Blue[7] (MSB)	D22
18	Blue[2]	D19	D15	NA	GND
19	Blue[3]	D20	D18	NA	GND
20	Blue[4]	D21	D19	NA	GND
21	Blue[5]	D22	D20	NA	GND
22	Blue[6]	D16	D21	NA	GND
23	Blue[7] (MSB)	D17	D22	BIAS_OUT (32 kHz)	GND
24	H_sync	D24	D24	H_sync	D24
25	V_sync	D25	D25	V_sync	D25

Table 33: LCD Connectivity to LVDS (Continued)

Pin	24 BPP Controller and Panel			18 BPP Controller and Panel	
	Mode0 Dumb Panel 24-bit Color 8:8:8	LVDS Option1	LVDS Option2	Mode1 Dumb Panel 18-bit Color 6:6:6	LVDS Option1
26	Pixel clk	CLK*	CLK*	Pixel clk	CLK*
27	DENA	D26	D26	DENA	D26
28	BIAS_OUT (32 kHz)	D23=RSRVD	D23=RSRVD	NA	D23=RSRVD

6.7 High-Speed SERDES Multiplexing

The MV78230 integrates seven high-speed SERDES lanes.

The SERDES lanes provide a physical SERDES link to the following interfaces:

- The following PCI Express operational modes:
  - Gen2.0 up to 5 Gbps
  - Gen1.1 up to 2.5 Gbps

  PCIe unit 0 may be configured to x4 or quad x1 lanes. PCIe unit 1 is always x1.
- SGMII interface:
  - SGMII0 and SGMII2 can operate at 1.25 Gbps or 3.125 Gbps.
  - SGMII1 operate at 1.25 Gbps.
- QSGMII (up to 5 Gbps)
- SATA Gen1 (1.5 Gbps) and SATA Gen2 (3 Gbps)
- Embedded Trace Module (ETM)

Table 34, MV78230 SERDES Lanes Multiplex Options presents the different modes available for each SERDES lane. Each lane can be configured independently for the required link type, according to the specified application. If a lane is unused, it can be turned off.

Note

For SERDES configuration information, see the Shared SERDES Selectors registers (offsets: 0x00018270 and 0x00018274) in the device's *Functional Specifications*.

Table 34: MV78230 SERDES Lanes Multiplex Options

Lanes						
0	**1**	**2**	**3**	**4**	**5**	**6**
PCIe0.0	PCIe0.1	PCIe0.2	PCIe0.3	PCIe1.0		
				SATA 0	SATA 1	SATA0
		SGMII0	SGMII 1	SGMII 2	SGMII1	SGMII 2
						SGMII0
	ETM0	ETM1		ETM0		
			QSGMII		QSGMII	

7 Reset and Initialization

This section details the device's reset sequence and initialization procedure.

7.1 Power Up/Down Sequence

7.1.1 Power-Up Sequence

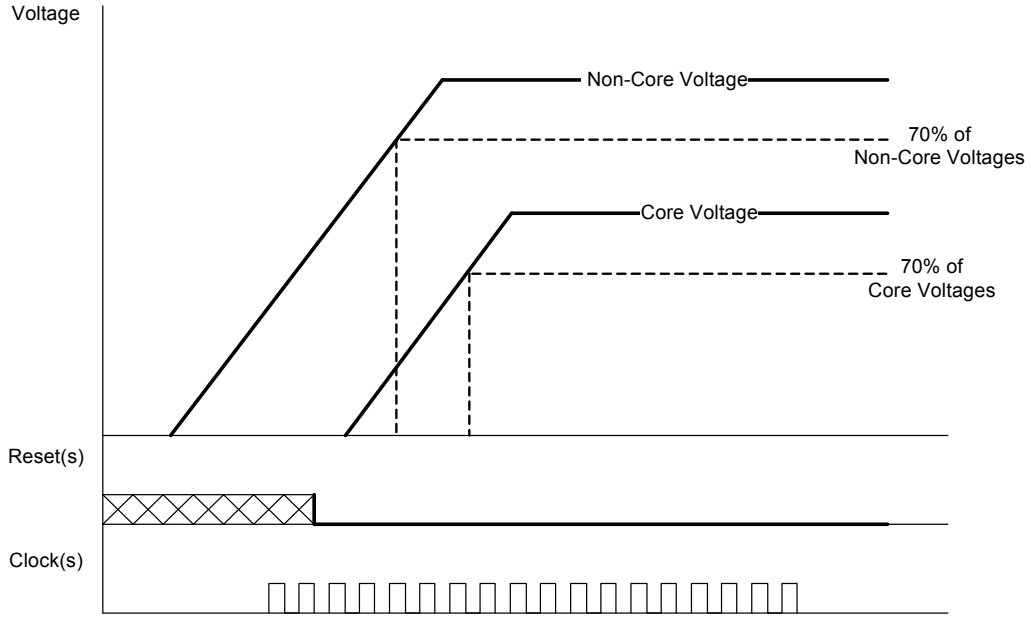
These requirements must be applied to meet the device power-up sequence (see Figure 6):

- The Non-Core voltages (I/O and Analog), as listed in Table 35, must reach 70% of their voltage level before the Core voltages.
  The order of the power up sequence between the Non-Core voltages is unimportant. The order of the power up sequence between the Core voltages is unimportant either.
- The reset signal(s) must be asserted before the Core voltages reach 70% of their voltage level.
- Each reference clock input must toggle with its respective voltage level before the first Core voltage reaches 70% of their voltage level. If a crystal oscillator is used, the system can rely on the oscillator wake-up mechanism.

Table 35: Non-Core and Core Voltages

Non-Core Voltages		Core Voltages
I/O Voltages	Analog Power Supplies	
VDDO_A VDDO_B VDDO_C VDDO_D VDDO_DEV VDDO_M VDDO_MISC VDDO_FPD VHV	RTC_AVDD SRD_AVDD CORE_TDM_AVDD CPU_PLL_AVDD XTAL_AVDD USB_AVDD USB_AVDDL	VDD VDD_CPU

Figure 6: Power Up Sequence Example



Note

- It is the designer's responsibility to verify that the power sequencing requirements of other components are also met.
- Although the Non-Core voltages can be powered up any time before the Core voltages, allow a reasonable time limit (for example 100 ms) between the **first** Non-Core voltage power-up and the **last** Core voltage power-up.

7.1.2 Power-Down Sequence

Allow a reasonable time limit (for example 100 ms) between the **first** and **last** voltage power-down.

7.2 Hardware Reset

The device has three reset inputs pin: SYSRSTn, CDRn, MRn. The following sections describe the functionality of these signals.

7.2.1 Global System Reset (SYSRSTn)

When asserted, the entire chip is placed in its initial state. Most outputs are placed in high-Z.

The following output pins are still active during SYSRSTn assertion:

- M_CLKOUT[3:0], M_CLKOUTn[3:0]
- M_CKE[3:0]
- M_ODT[3:0]
- M_RESET
- SRD<n>_TX_P
- SRD<n>_TX_N
- USB<n>_DM
- USB<n>_DP

- PEX<n>_CLK_N
- PEX<n>_CLK_P

The device has an optional SYSRST_OUTn open drain output signal, that is used as a reset request from the device to the board reset logic. This signal is set when one of the following maskable events occurs. In each of these cases, SYSRST_OUTn is asserted for a duration of 100 ms:

- Received a hot reset indication from the PCI Express port 0 link when used as a PCI Express endpoint, and bit <PCIe0RstOutMaskSysRstOut> is cleared to 0, and <GlobalSoftRstOutEn> is set to 1 in the RSTOUTn Mask Register (offset 0x00018260) (see the System Registers appendix of the device's *Functional Specifications*).
- PCI Express port 0 link failure, when used as a PCI Express endpoint, and bit <PCIe0RstOutMaskSysRstOut> is cleared to 0, and <GlobalSoftRstOutEn> is set to 1 in the RSTOUTn Mask Register (see the System Registers appendix of the device's *Functional Specifications*).
- One of the Watchdog timers expires and bit <WDRstOutEn> of the relevant watchdog counter is set to 1 in the RSTOUTn Mask Register (see the System Registers appendix of the device's *Functional Specifications*).
- Bit <SystemSoftRst> is set to 1 in System Soft Reset Register (offset 0x00018264) and bit <SoftRstOutEn> is set to 1 in RSTOUTn Mask Register (offset 0x00018260) (see the System Registers appendix of the device's *Functional Specifications*).
- An assertion of the internal power-on-reset (POR) circuit (see Section 7.4, Power On Reset (POR), on page 80 for further details). This assertion is not maskable. The duration of this assertion is for at least 100ms.
- SYSRST_OUTn is asserted as long as the MRn input signal is asserted low, and for an additional at least 100 ms after MRn de-assertion (This is useful for implementations that include a manual reset button).

Note

SYSRSTn must be active for a minimum length of 20 ms. Core power, I/O power, and analog power must be stable (VDD +/- 5%) during that time and onward.

7.2.1.1 SYSRSTn Duration Counter

When SYSRSTn is asserted low, a SYSRSTn duration counter starts counting. It continues to count as long as the SYSRSTn signal remains asserted.

- The counter clock is the 25 MHz reference clock.
- It is a 29-bit counter, yielding a maximum counting duration of 2^29/25 MHz (21.4 seconds).
- The host software can read the counter value and reset the counter.
- When the counter reaches its maximum value, it remains at this value until the counter reset is triggered by software.

See the device's *Functional Specifications* for details on how to configure the SYSRSTn duration counter.

Note

The SYSRSTn duration counter is useful for implementing manufacturer/factory reset. Upon a long reset assertion, greater than a pre-configured threshold, the host software may reset all settings to the factory default values.

7.2.2 Manual Reset (MRn)

The Manual Reset pin (MRn) provide the user the ability to reset the device without powering down the device. This is useful for implementations that include a reset button. Once MRn pin is asserted low, the device's reset logic, that includes a bouncer circuit to avoid false reset spikes, will propagate a reset indication to the SYSRST_OUTn pin. The SYSRST_OUTn will be asserted as long as the MRn pin is kept asserted and for additional 100ms. The external (on board) logic may drive this indication back to the SYSRSTn pin to reset the device, and in addition use the SYSRST_OUTn pin to reset the entire board.

7.2.3 Marvell® Core Processor CPU Debugger Reset

Connect the CPU debugger reset to the CDRn pin.

When the CPU Debugger reset is asserted, the device returns to its default value. The device mechanisms related to the debugger are excluded from the reset event. This includes the PLLs, the SSCG, the XTAL, and the registers controlling those mechanisms.

In general, the CDRn is de-asserted after all processes on the TAP controller are completed (refer to the specific Debugger specifications).

CPU debugger reset should be fed into two separate circuits:

- The device's CDRn pin (the reset pin for the debugger).
- The board reset for all other devices (not including the device's SYSRSTn pin), since SYSRST_OUTn will not be forced by the CDR pin.

7.3 PCI Express Reset

As a Root Complex, the device can generate a Hot Reset to the PCI Express port. Upon CPU setting of the PCI Express Control register's <ConMstrHot Reset> bit, the PCI Express unit sends a Hot Reset indication to the Endpoint (see the PCI Express Interface section in the device's *Functional Specifications*).

When the device works as an Endpoint, and a Hot Reset packet is received:

- A maskable interrupt is asserted.
- If the PCI Express Debug Control register's <DisHotResetRegRst> is cleared, the device also resets the PCI Express register file to its default values.
- The device triggers an internal reset, if not masked by PCI Express Debug Control register's <ConfMskHotReset> bit.

Link failure is detected if the PCI Express link was up (LTTSSM L0 state) and dropped back to an inactive state (LTSSM Detect state). When Link failure is detected:

- A maskable interrupt is asserted
- If the PCI Express Debug Control register's <DisLinkFailRegRst> is cleared, the device also resets the PCI Express register file to its default values.
- The device triggers an internal reset, if not masked by PCI Express Debug Control register's <ConfMskLinkFail> bit.

Whether initiated by a hot reset or link failure, this internal reset indication can be routed to the PCIe_RSTOUTn signal (multiplexed on MPP[43]) to reset components on the board without resetting the entire device (e.g reset only the endpoint card).

Note Only the PCIe0 port (or PCIe0.0 port in Quad x1 configuration) can act as a PCI Express endpoint, and only this port can generate the PCI Express internal reset indication.

7.4 Power On Reset (POR)

The device integrates a Power On Reset (POR) circuit. The circuit is triggered when the VDD (digital core voltage) and VDD_CPU (CPU core Voltage) power up levels reach a VDD threshold (with a threshold maximum value of 0.8V).

Hysteresis: Another trigger will only occur after any of the power first drops to 50 mV, and then a power up occurs.

Once the POR logic was triggered the SYSRST_OUTn output signal is asserted low for 100 ms.

The SYSRST_OUTn signal may be connected externally to the device's SYSRSTn input signal asserting the device's internal reset signal. In addition, the SYSRST_OUTn signal may be used in this case as the POR generator for the entire board.

7.5 Reset Configuration

The device uses certain pins as configuration inputs to set certain critical parameters following a reset. The definition of the sampled at reset configuration pins revert immediately after reset to their regular function.

7.5.1 Pin Sampling Configuration

The following pins are sampled during SYSRSTn de-assertion. Some of the device's pins integrate an internal pull-up/pull-down resistors to set a default mode. Smaller external pull-up/pull-down resistors are required to change the default mode of operation, if required. These signals must remain pulled up or down until SYSRSTn de-assertion (zero Hold time in respect to SYSRSTn de-assertion).

Note

- If external logic is used instead of pull-up and pull-down resistors, the logic must drive all of these signals to the desired values during SYSRSTn assertion. To prevent bus contention on these pins, the external logic must float the bus no later than the third TCLK cycle after SYSRSTn de-assertion.
- All reset sampled values are registered in the Sample at Reset register (see the MPP Registers in the device's *Functional Specifications*). This is useful for board debug purposes and identification of board and system settings for the host software.
- If a signal is pulled up on the board for reset sampling, it must be pulled to the appropriate voltage level of the power domain that the signal is assigned to. For example, if MPP[X] should be pulled up for reset sampling, it should be pulled to the voltage level of the VDDO who is feeding MPP[X] according to the pin description table.
- If an external device is driving any of the pins that are used as sampled at reset signals, make sure to keep this external device in reset state (prevent it from driving) or use glue logic to disconnect it from the device as long as the device SYSRSTn input is asserted.

Table 36 lists the reset configuration pins for the device.

Table 36: Reset Configuration Pins

Pins	Power Rail	Configuration Function	SAR Register[1] Bit Location
UA0_TXD	VDDO_MISC	I^2C0 Serial ROM Initialization	[0]
		0x0 = Disabled 0x1 = Enabled **NOTE:** Internally pulled down to 0x0.	
UA1_TXD	VDDO_MISC	I^2C1 Debug Port	[1]
		0x0 = Disabled 0x1 = Enabled **NOTE:** Internally pulled down to 0x0.	
DEV_AD[7]	VDDO_DEV	PCI Express Clock (100 MHz Differential Clock) Configuration	[2]
		0x0 = PCIe clock input enable. The device uses an external source for PCI Express clock. Pins PEX0_CLK_N/P are inputs. PEX1_CLK_N/P are not used. 0x1 = PCIe clock output enable. The device uses an internally generated clock for PCI Express clock. Pins PEX0_CLK_N/P and PEX1_CLK_N/P are outputs, driving out the PCI Express differential clock. **NOTE:** Internally pulled to 0x1.	
DEV_AD[15]	VDDO_DEV	Boot Device Width	[3]
		For boot via NOR/NAND flash: 0x0 = 8 bits 0x1 = 16 bits For boot via SPI flash: 0x0 = SPI 32 bits 0x1 = SPI 24 bits **NOTE:** Internally pulled down to 0x0.	

Table 36: Reset Configuration Pins (Continued)

Pins	Power Rail	Configuration Function	SAR Register[1] Bit Location
DEV_AD[14:11]	VDDO_DEV	Boot Device Type Selection 0x0 = BootROM enabled, Boot from Device (NOR) flash 0x1 = BootROM enabled, Boot from NAND flash (see NAND Flash Page Type Initialization Sequence / SERDES Selection for more details) 0x2 = BootROM enabled, Boot from UART 0x3 = BootROM enabled, Boot from SPI0 (CS0) 0x4 = BootROM enabled, Boot from PCIe Port 0.0 0x5 = BootROM enabled, Boot from SATA Port (see NAND Flash Page Type Initialization Sequence / SERDES Selection for more details) 0x6 = Reserved 0x7 = BootROM enabled, UART debug prompt mode **NOTE:** 1. If DEV_AD[14:11] are set to 0x3, MPP[39:36] pins wake up as SPI flash signals (affect default value of MPPSel registers). 2. Internally pulled to 0x0.	[8:5]
MPP[0]	VDDO_A	VDDO_C Voltage Select 0x0 = 1.8V 0x1 = 3.3V **NOTE:** Internally pulled up to 0x1.	[9]
MPP[36]	VDDO_D	VDDO_DEV Voltage Select 0x0 = 1.8V 0x1 = 3.3V **NOTE:** Internally pulled up to 0x1.	[10]
MPP[2:1]	VDDO_A	NAND Flash Page Type Initialization Sequence / SERDES Selection Only relevant if booting with NAND Flash. 0x0 = 512B 0x1 = 2KB 0x2 = 4KB 0x3 = 8KB If booting with SATA, select the SERDES lane that the initialization sequence uses: 0x0 = Lane 4 (SATA0) 0x1 = Lane 5 (SATA1) 0x2 = Lane 6 (SATA0) 0x3 = Reserved **NOTE:** Internally pulled down to 0x0.	[12:11]

Table 36: Reset Configuration Pins (Continued)

Pins	Power Rail	Configuration Function	SAR Register[1] Bit Location
MPP[4]	VDDO_A	DEV_WEn and DEV_OEn multiplexing option for A[16:15] bits.	[13]
		In case boot device is a NOR flash, defines if OE and WE are latched at first ALE cycle as A[15] and A[16]. This fact influences the OEn and WEn signal as follows: 0 = A[16:15] bits are not multiplexed on OE and WE signals. Whenever CS is inactive OE and WE are inactive. 1 = A[16:15] bits are multiplexed on OE and WE signals. Whenever CS is inactive and ALE[1:0] are high, OE and WE are inactive. **NOTE:** Internally pulled down to 0x0.	
MPP[13:12]	VDDO_B	NAND Flash ECC Algorithm	[15:14]
		In case boot device is NAND flash, defines the type of ECC algorithm that is used by the internal bootROM for ECC calculation on the boot NAND flash: 0x0 = 4-bit ECC 0x1 = 8-bit ECC 0x2 = 12-bit ECC 0x3 = 16-bit ECC **NOTE:** Internally pulled down to 0x2.	
MPP[3]	VDDO_A	Reserved	[16]
		This signal must be sampled as 0x1 at reset de-assertion. **NOTE:** Internally pulled up to 0x1.	
MPP[38]	VDDO_D	Reserved	[17]
		This signal must be sampled as 0x1 at reset de-assertion. **NOTE:** Internally pulled up to 0x1.	
MPP[14]	VDDO_B	SSCG Disable	[18]
		0 = Enable 1 = Disable **NOTE:** Internally pulled to 0x1.	
{MPP[27], MPP[15]}	MPP[27]: VDDO_C MPP[15]: VDDO_B	Reserved	[20:19]
		These signals must be sampled as 0x1 at reset de-assertion. **NOTE:** Internally pulled to 0x3.	

Table 36: Reset Configuration Pins (Continued)

Pins	Power Rail	Configuration Function	SAR Register[1] Bit Location
{DEV_ALE[0], DEV_AD[10:8]}	VDDO_DEV	CPU0 Clock Frequency Select	{[52], [23:21]}
		Determines the frequency of CPU(0): 0x0 = 1000 MHz 0x1 = 1066 MHz 0x2 = 1200 MHz 0x3 = 1333 MHz 0x4 = 1500 MHz 0x9 = 667 MHz 0xA = 800 MHz 0xB = 1600 MHz All other options are reserved. **NOTE:** Internally pulled to 0x3.	
{GE_MDC, DEV_AD[6:3]}	GE_MDC: VDDO_A DEV_AD[6:3]: VDDO_DEV	Fabric Frequency Options	[51, 27:24]
		Determines the ratios between PCLK0, NBCLK, and DRAMCLK clock. For full details about the various options, refer to Section 5, Clocking, on page 64. **NOTE:** Internally pulled to 0x5.	
MPP[24]	VDDO_C	Reserved	[28]
		This signal must be sampled as 0x0 at reset de-assertion. **NOTE:** Internally pulled down to 0x0.	
DEV_AD[2:1]	VDDO_DEV	Reserved	[30:29]
		This signal must be sampled as 0x0 at reset de-assertion. These signals must be sampled as 0x0 at reset de-assertion. **NOTE:** Internally pulled down to 0x0.	
DEV_A[1:0]	VDDO_DEV	Reserved	[32:31]
		These signals must be sampled as 0x3 at reset de-assertion. **NOTE:** Internally pulled down to 0x0.	
DEV_AD[0]	VDDO_DEV	Reserved	[33]
		NOTE: This signal must be sampled as 0x0 at reset de-assertion.	
DEV_ALE[1]	VDDO_DEV	CPU0 Non-maskable Fast Interrupt Enable	[34]
		Disables fast interrupt software masking. 0 = Software masking for fast interrupts 1 = Software cannot mask fast interrupts **NOTE:** Internally pulled down to 0x0.	

Table 36: Reset Configuration Pins (Continued)

Pins	Power Rail	Configuration Function	SAR Register[1] Bit Location
MPP[48]	VDDO_DEV	Reserved	[35]
		This signal must be sampled as 0x1 at reset de-assertion. **NOTE:** Internally pulled down to 0x0.	
DEV_A[2]	VDDO_DEV	CPU0 Pclk WFI Enable	[38]
		Enable wake-up from interrupt through a debugger. 0 = Disable 1 = Enable **NOTE:** With WFI enabled, there is no effective power saving. This feature is used for Debug mode only. Internally pulled down to 0x0.	
DEV_OEn	VDDO_DEV	Reserved	[39]
		This signal must be sampled as 0x1 at reset de-assertion. **NOTE:** Internally pulled up to 0x1.	
DEV_WEn[0]	VDDO_DEV	Reserved	[41]
		This signal must be sampled as 0x1 at reset de-assertion. **NOTE:** Internally pulled up to 0x1.	
DEV_WEn[1]	VDDO_DEV	Reserved	[42]
		This signal must be sampled as 0x0 at reset de-assertion. **NOTE:** Internally pulled down to 0x0.	

1. Bits[31:0] refer to the Sample at Reset register (offset: 0x00018230). Bits[63:32] refer to the Sample at Reset High register (offset:0x00018234). Both registers are defined in the device's *Functional Specifications*.

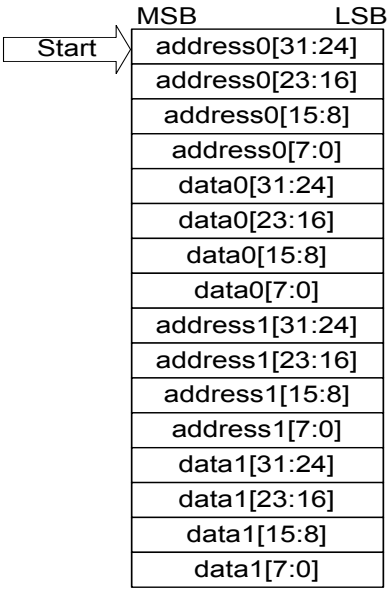
7.6 Serial ROM Initialization

The device supports initialization of ALL of its internal and configuration registers through the I^2C0 master interface. If serial ROM initialization is enabled by pulling up I2C0 Serial ROM Initialization during SYSRSTn assertion, the device I^2C0 master starts reading initialization data from serial ROM and writes it to the appropriate registers.

7.6.1 Serial ROM Data Structure

The Serial ROM data structure consists of a sequence of 32-bit address and 32-bit data pairs, as shown in Figure 7.

Figure 7: Serial ROM Data Structure



The serial ROM initialization logic reads eight bytes at a time. It performs address decoding on the 32-bit address being read, and based on address decoding result, writes the next four bytes to the required target.

The Serial Initialization Last Data Register contains the expected value of last serial data item (default value is 0xFFFFFFFF). When the device reaches last data, it stops the initialization sequence.

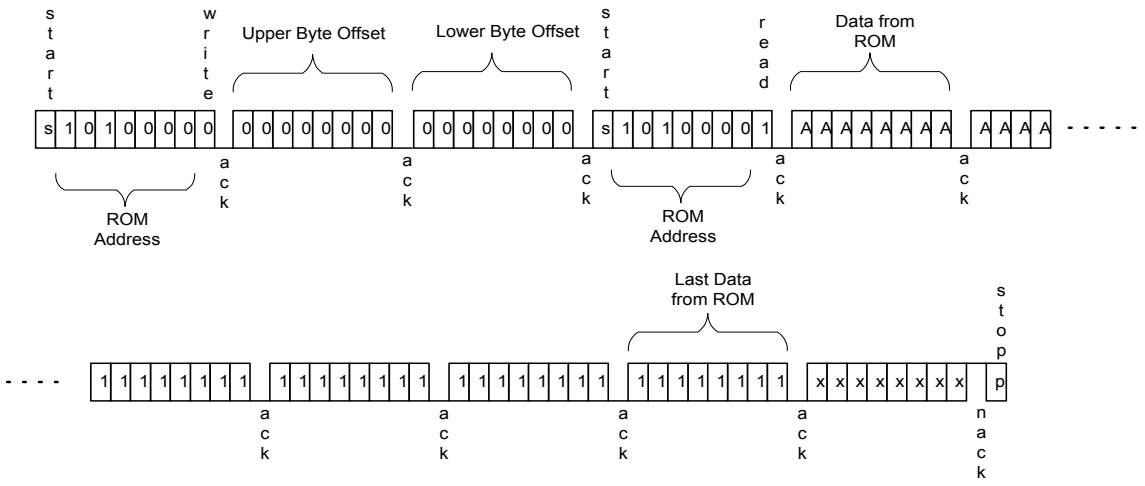
Note

Users must not generate requests through the I^2C0 auto-loader to addresses that are not 32-bit aligned.

7.6.2 Serial ROM Initialization Operation

On SYSRSTn de-assertion, the device starts the initialization process. It first performs a dummy write access to the serial ROM, with data byte(s) of 0x0, to set the ROM byte offset to 0x0. Then, it performs a sequence of reads, until it reaches last data item, as shown in Figure 8.

Figure 8: Serial ROM Read Example



Implementation Notes:

- Initialization data must be programmed in the serial ROM starting at offset 0x0.
- The serial EEPROM must contain two address offset bytes (16-bits). These bytes must not be less than a 256 byte ROM.
- The device assumes 7-bit serial ROM address of ‘b1010000.
- After receiving the last data identifier (default value is 0xFFFFFFFF), the device receives an additional byte of dummy data. It responds with no-ack, and then asserts the stop bit.

For a detailed description of I^2C implementation, see the I^2C Interface section in the device’s *Functional Specifications*.

7.7 Boot Sequence

The device requires that SYSRSTn stay asserted for at least 100 ms after power and clocks are stable. The following procedure describes the boot sequence starting with SYSRSTn assertion:

1. While SYSRSTn is asserted, the CPU PLL and the core PLL are locked.
2. Upon SYSRSTn de-assertion, the pad drive auto-calibration process starts and the DRAM PHY DLL starts to lock on the target frequency speed. It requires 3ms to gain lock indication and be ready for normal operation.
3. If Serial ROM initialization is enabled, an initialization sequence is started.

Upon completing the above sequence, the internal CPU reset is de-asserted, and the CPU starts executing boot code from the internal Boot ROM, according to sample at reset setting of Boot Device Type Selection.

For boot sequence details, see the BootROM Firmware section in the device’s *Functional Specifications*.

As part of the CPU boot code, the CPU typically performs these steps:

1. Configures the PCI Express address map.
2. Configure device bus timing parameters, according to devices attached to device bus.
3. Configures the proper SDRAM controller parameters, and then triggers SDRAM initialization.
4. Sets <InitEn> bit [0] to 1 in the SDRAM Initialization Control register. Initializes proper ECC to the entire SDRAM space.
5. Sets the <PEXxEn> bits in the SoC Control register to wake up the PCI Express link.

8 JTAG Interface

The MV78230 JTAG interface is used for chip boundary scan, and for CPU core debugging and tracing.

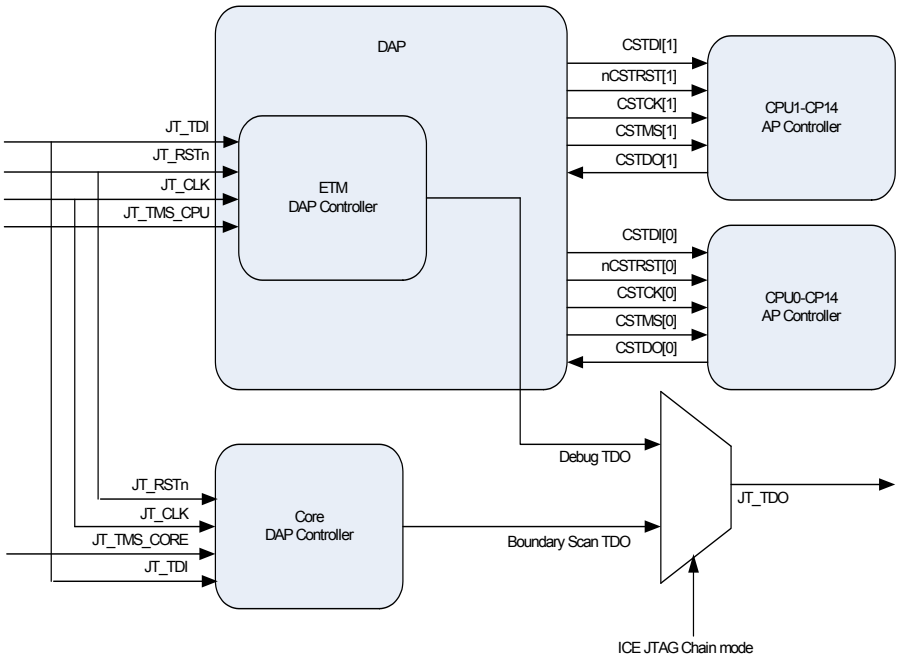
The device supports the following test modes:

Boundary scan The JT_TMS_CPU is kept high. This state resets the CPUs and the ETM DAP controllers, and multiplexes the boundary scan TDO signal on the JT_TDO pin.

CPU debugger and trace The JT_TMS_CORE is kept high. This state resets the MV78230 TAP controller, and multiplexes the ETM DAP controller TDO signal on the JT_TDO pin.

Figure 9 shows the connection between the JTAG signals, between the ETM DAP controller, and the device's AP controller.

Figure 9: ETM-JTAG-AP-Parallel Mode



8.1 Instruction Register

The Instruction register (IR) is a 4-bit, two-stage register. It contains the command that is shifted in when the DAP FSM is in the *Shift-IR* state. When the DAP FSM is in the *Capture-IR* state, the IR outputs all four bits in parallel.

Table 37 lists the instructions supported by the device.

Table 37: Supported JTAG Instructions

Instruction	Code	Description
HIGH-Z	00011	Select the single bit Bypass register between TDI and TDO. Sets the device output pins to high-impedance state.
IDCODE	00010	Selects the Identification register between TDI and TDO. This 32-bit register is used to identify the device.
EXTEST	00000	Selects the Boundary Scan register between TDI and TDO. Outputs the boundary scan register cells to drive the output pins of the device. Inputs the boundary scan register cell to sample the input pin of the device.
SAMPLE/ PRELOAD	00001	Selects the Boundary Scan register between TDI and TDO. Samples input pins of the device to input boundary scan register cells. Preloads the output boundary scan register cells with the Boundary Scan register value.
BYPASS	11111	Selects the single bit Bypass register between TDI and TDO. This allows for rapid data movement through an untested device.

8.2 Bypass Register

The Bypass register (BR) is a single bit serial shift register that connects TDI to TDO, when the IR holds the Bypass command, and the DAP FSM is in *Shift-DR* state. Data that is driven on the TDI input pin is shifted out one cycle later on the TDO output pin. The Bypass register is loaded with 0 when the DAP FSM is in the *Capture-DR* state.

8.3 JTAG Scan Chain

The JTAG Scan Chain is a serial shift register used to sample and drive all of the device pins during the JTAG tests. It is a 2-bit per pin shift register in the device, thereby allowing the shift register to sequentially access all of the data pins both for driving and strobing data. For further details, refer to the BSDL Description file for the device.

8.4 ID Register

The ID register is a 32-bit deep serial shift register. The ID register is loaded with vendor and device information when the DAP FSM is in the *Capture-DR* state. The Identification code format of the ID register is shown in Table 38, which describes the various ID Code fields.

Table 38: IDCODE Register Map

Bits	Value	Description
31:28	0x2	Version
27:12	0x8230	Part number
11:1	0x1AB	Manufacturer ID
0	1	Mandatory

9 Electrical Specifications

9.1 Absolute Maximum Ratings

Table 39: Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
VDD	-0.5	1.1	V	Core voltage
VDD_CPU	-0.5	1.32	V	CPU core and CPU subsystem voltage
CORE_TDM_PLL_AVDD	-0.5	2.2	V	Analog supply for the internal PLL
CPU_PLL_AVDD	-0.5	2.2	V	Analog supply for the CPU PLL
VDDO_M	-0.5	2.2	V	I/O voltage for: SDRAM interface
VDDO_A, VDDO_B, VDDO_C, VDDO_D	-0.5	4	V	I/O voltage for: SMI interface, Device Bus interface, and MPP[47:0]
VDDO_DEV	-0.5	4	V	I/O voltage for: Device Bus interface and MPP[48]
VDDO_MISC	-0.5	4	V	I/O voltage for: I^2C0/1, UART0/1/2/3, SPI0/1, and JTAG interfaces and the following signals: • SYSRSTn • SYSRST_OUTn • MRn • CDRn
VDDO_FPD	-0.5	2.2	V	I/O voltage for: Flat Panel Display interface
USB_AVDD	-0.5	4	V	I/O voltage for: USB interface
USB_AVDDL	-0.5	2.2	V	I/O voltage for: USB interface
SRD_AVDD	-0.5	2.2	V	I/O voltage for: SERDES interface
RTC_AVDD	-0.5	4	V	I/O voltage for: RTC interface
XTAL_AVDD	-0.5	2.2	V	I/O voltage for: XTAL interface

Table 39: Absolute Maximum Ratings (Continued)

Parameter	Min	Max	Units	Comments
AVS_SSCG_AVDD	-0.5	2.2	V	I/O voltage for: SSCG, CPU AVS, and Core AVS blocks
VHV	-0.5	2.2	V	I/O voltage for: eFuse (for eFuse burning only)
TC	-40	125	° C	Case temperature
TSTG	-40	125	° C	Storage temperature

Caution

- Exposure to conditions at or beyond the maximum rating can damage the device.
- Operation beyond the recommended operating conditions (Table 40) is neither recommended nor guaranteed.

Note

Before designing a system, it is recommended that you read application note AN-63: *Thermal Management for Marvell® Technology Products*. This application note presents basic concepts of thermal management for Integrated Circuits (ICs) and includes guidelines to ensure optimal operating conditions for Marvell Technology's products.

9.2 Recommended Operating Conditions

Table 40: Recommended Operating Conditions

Parameter	Min	Typ	Max	Units	Comments
VDD	0.85	0.9	0.95	V	Core voltage
VDD_CPU	1	1.05	1.10	V	**NOTE:** CPU core and CPU voltage The 1.1V is supported by the AVS feature for specific clock configurations. The power source must be set to 1.05V. The AVS unit will drive the power source to adjust the voltage to 1.1V. For additional details, see Table 30, Clock Frequency Options, on page 65.
	1.05	1.1	1.15	V	
CORE_TDM_PLL_AVDD	1.7	1.8	1.9	V	Analog supply for the internal PLL
CPU_PLL_AVDD	1.7	1.8	1.9	V	Analog supply for the CPU PLL
VDDO_M	1.283	1.35	1.418	V	I/O voltage for: SDRAM DDR3 (1.5/1.35V) **NOTE:** If DDR3 is configured to 800 MHz, VDDO_M must be operating at 1.5V.
	1.425	1.5	1.575	V	
	1.7	1.8	1.9	V	
VDDO_A, VDDO_B	1.7	1.8	1.9	V	I/O voltage for: SMI interface and MPP[23:0] pins
	2.375	2.5	2.625		
	3.15	3.3	3.45		
VDDO_C	1.7	1.8	1.9	V	I/O voltage for: MPP[35:24] pins
	3.15	3.3	3.45		
VDDO_D	3.15	3.3	3.45	V	I/O voltage for: MPP[47:36] pins
VDDO_DEV	1.7	1.8	1.9	V	I/O voltage for: Device Bus interface and MPP[48]
	3.15	3.3	3.45		

Table 40: Recommended Operating Conditions (Continued)

Parameter	Min	Typ	Max	Units	Comments
VDDO_MISC	3.15	3.3	3.45	V	I/O voltage for: I^2C0/1, UART0/1/2/3, SPI0/1, and JTAG interfaces and the following signals: • SYSRSTn • SYSRST_OUTn • MRn • CDRn
VDDO_FPD	1.7	1.8	1.9	V	I/O voltage for: Flat Panel Display interface
USB_AVDD	3.15	3.3	3.45	V	I/O voltage for: USB interface
USB_AVDDL	1.7	1.8	1.9	V	I/O voltage for: USB interface
SRD_AVDD	1.7	1.8	1.9	V	Voltage for: SERDES interface
RTC_AVDD	3.15	3.3	3.45	V	I/O voltage for: RTC interface (via the board)
	2.6	3	3.6	V	I/O voltage for: RTC interface (via the battery)
XTAL_AVDD	1.7	1.8	1.9	V	I/O voltage for: XTAL interface
AVS_SSCG_AVDD	1.7	1.8	1.9	V	I/O voltage for: SSCG, CPU AVS, and Core AVS blocks
VHV	1.7	1.8	1.9	V	I/O voltage for: eFuse (for eFuse burning only)
TJ	0		105	° C	Junction Temperature

Caution Operation beyond the recommended operating conditions is neither recommended nor guaranteed.

9.3 Thermal Power Dissipation

Note The device was characterized and tested for production at 105°C. The other data points are for reference purposes only.

Table 41: Core and CPU Thermal Power Dissipation

Interface	Symbol	Parameter	Power	Units
Core	P_{VDD}	Core at 250 MHz, VDD=0.9V, Tj=85°C	1.5	W
		Core at 250 MHz, VDD=0.9V, Tj=105°C	1.9	W
Embedded CPU0, CPU1, and 1 MB L2 cache	P_{VDD_CPU}	CPU0/1 at 800 MHz, L2 at 400 MHz, VDD_CPU=1.05V, Tj=85°C	3.3	W
		CPU0/1 at 800 MHz, L2 at 400 MHz, VDD_CPU=1.05V, Tj=105°C	4.2	W
		CPU0/1 at 1066 MHz, L2 at 533 MHz, VDD_CPU=1.05V, Tj=85°C	3.6	W
		CPU0/1 at 1066 MHz, L2 at 533 MHz, VDD_CPU=1.05V, Tj=105°C	4.6	W
		CPU0/1 at 1333 MHz, L2 at 667 MHz, VDD_CPU=1.05V, Tj=85°C	4	W
		CPU0/1 at 1333 MHz, L2 at 667 MHz, VDD_CPU=1.05V, Tj=105°C	5	W
		CPU0/1 at 1600 MHz, L2 at 800 MHz, VDD_CPU=1.1V, Tj=85°C	4.9	W
		CPU0/1 at 1600 MHz, L2 at 800 MHz, VDD_CPU=1.1V, Tj=105°C	5.9	W

Table 42: I/O Interface Thermal Power Dissipation

Interface	Symbol	Parameter	Power	Units
DDR3 interface (40-bit, 400 MHz, 1.5V)	P_{VDDO_M}	M_CLKOUT = 400 MHz, 4 DRAM ranks,75 ohm internal termination, 40 ohm DRAM termination	0.6	W
DDR3 interface (40-bit, 667 MHz, 1.35V)		M_CLKOUT = 667 MHz, 2 DRAM ranks, 75 ohm internal termination, 40 ohm DRAM termination	0.5	W
DDR3 interface | (40-bit, 667 MHz, 1.5V)		M_CLKOUT = 667 MHz, 4 DRAM ranks, 75 ohm internal termination, 40 ohm DRAM termination	0.7	W
DDR3 interface (40-bit, 800 MHz, 1.5V)		M_CLKOUT = 800 MHz, 2 DRAM ranks, 75 ohm internal termination, 40 ohm DRAM termination	0.7	W
RGMII 3.3V interface	P_{RGMII}	One Port, VDDO = 3.3V	100	mW
RGMII 2.5V interface		One Port, VDDO = 2.5V	60	mW
RGMII 1.8V interface		One Port, VDDO = 1.8V	35	mW
LCD 3.3V interface	P_{LCD}	VDDO = 3.3V, Trace Length = 5 inches	360	mW
LCD 1.8V interface		VDDO = 1.8V Trace Length = 5 inches	110	mW
SERDES interface	P_{SRD_AVDD}	Single Serdes Port	95	mW
USB interface	P_{USB_AVDD}	Three USB Ports	99	mW
USB interface	P_{USB_AVDDL}		180	mW

Notes:

1. The power dissipation values are for a device operating at the nominal recommended voltage.
2. The Trace length is 3 inches, unless otherwise specified.
3. The power values for each interface are stated relevant to the common application usage.

9.4 SoC Power Dissipation for Power Management Unit Low Power Modes

The MV78230 Power Management Unit (PMU) controls power management functions and enables the optimization of the device's overall power consumption and performance.

The PMU allows for Idle, Deep Idle, and Sleep low power modes that supply different levels of power consumption, with hardware controlling wake-up events and power mode transitions.

Table 43 lists the MV78230 power dissipation for specific SoC configurations, and not the total power of the device.

The following system configuration were used for testing:

- Dual core CPU @ 1600 MHz
- DDR 32-bit (ECC and dual CS), 1.5V@ 800 MHz
- 1 SGMII SERDES
- 2 x PCIe x1
- 1 SATA
- 1 USB
- SPI

Note

- For more details on the MV78230 power modes and additional PMU features, refer to the Power Management Unit section of the *MV78230 Functional Specifications*.
- To calculate the overall power for any other SoC configuration, use the power values in Table 41 on page 94 and Table 42.

Table 43: SoC Power Dissipation

Power Mode	Power Watts (W)						Notes
	CPU Subsystem	SoC Core	DDR	SERDES	Other interfaces[1]	Total	
Run Thermal CPU/L2 – On SERDES – On DDR – On	5.9	1.9	0.7	0.4	0.5	9.4	2
Run Typical CPU/L2 – On SERDES – On DDR – On	4.9	1.5	0.7	0.4	0.5	8	3
Idle CPU/L2 – WFI SERDES – On DDR – On	2.4	1.5	0.7	0.4	0.5	5.5	4
Deep Idle CPU/L2 – Off SERDES – On DDR – On	0.07	1.5	0.7	0.4	0.5	3.17	5
Sleep CPU/L2 – Off SERDES – Off DDR – Self-Refresh	0.07	0.8	0	0	0.2	1.07	6

Notes:

1. Other interfaces include: 1xUSB, GPIO, PLLs, XTAL, RTC, JTAG, I2C, and UART.
2. Run Thermal: Voltages are in nominal values, Tj=105°C, CPU is running stress test
3. Run Typical: Voltages are in nominal values, Tj=85°C
4. Idle: Voltage are in nominal values, Tj=85°C, CPU is in Wait for Interrupt (WFI) mode
5. Deep Idle: voltage are in nominal values, Tj=85°C, CPU is in Deep Idle mode
6. Sleep: User Activated mode. Tj=35°C, CPU in Deep Idle mode, SERDES are Powered down, USB PHY is shutdown, DDR in Self Refresh mode. Peripheral interfaces are set as clock gated, and wake from GPIO.

9.5 Current Consumption

Table 44: Current Consumption

Interface	Symbol	Test Conditions	Max	Units
Core	I_{VDD}	Core at 250 MHz, VDD=0.9V, Tj=85°C	1.6	A
		Core at 250 MHz, VDD=0.9V, Tj=105°C	2	A
Embedded CPU0, CPU1, and 1 MB L2 cache	I_{VDD_CPU}	CPU0/1 at 800 MHz, L2 at 400 MHz, VDD_CPU=1.05V, Tj=85°C	3.6	A
		CPU0/1 at 800 MHz, L2 at 400 MHz, VDD_CPU=1.05V, Tj=105°C	4.6	A
		CPU0/1 at 1066 MHz, L2 at 533 MHz, VDD_CPU=1.05V, Tj=85°C	4.2	A
		CPU0/1 at 1066 MHz, L2 at 533 MHz, VDD_CPU=1.05V, Tj=105°C	5.1	A
		CPU0/1 at 1333 MHz, L2 at 667 MHz, VDD_CPU=1.05V, Tj=85°C	4.7	A
		CPU0/1 at 1333 MHz, L2 at 667 MHz, VDD_CPU=1.05V, Tj=105°C	5.6	A
		CPU0/1 at 1600 MHz, L2 at 800 MHz, VDD_CPU=1.1V, Tj=85°C	5.4	A
		CPU0/1 at 1600 MHz, L2 at 800 MHz, VDD_CPU=1.1V, Tj=105°C	6.4	A
DDR3 interface (40-bit, 400 MHz, 1.5V)	I_{VDDO_M}	M_CLKOUT = 400 MHz, 4 DRAM ranks, 75 ohm internal termination, 150 ohm DRAM termination	1	A
DDR3 interface (40-bit, 667 MHz, 1.35V)		M_CLKOUT = 667 MHz, 2 DRAM ranks, 75 ohm internal termination, 40 ohm DRAM termination	0.9	A
DDR3 interface (40-bit, 667 MHz, 1.5V)		M_CLKOUT = 667 MHz, 4 DRAM ranks, 75 ohm internal termination, 40 ohm DRAM termination	1.2	A
DDR3 interface (40-bit, 800 MHz, 1.5V)		M_CLKOUT = 800 MHz, 2 DRAM ranks, 75 ohm internal termination, 40 ohm DRAM termination	1.2	A
RGMII 3.3V interface	I_{RGMII}	One Port, VDDO = 3.3V	60	mA
RGMII 2.5V interface		One Port, VDDO = 2.5V	50	mA
RGMII 1.8V interface		One Port, VDDO = 1.8V	40	mA
NOTE: I_{VDDO_A} and I_{VDDO_B} can be reduced to equal I_{RGMII} when the GbE interface is configured to RGMII mode.				

Table 44: Current Consumption

Interface	Symbol	Test Conditions	Max	Units
LCD 3.3V interface	I_{LCD}	VDDO = 3.3V, Trace Length = 5 inches	450	mA
LCD 1.8V interface		VDDO = 1.8V, Trace Length = 5 inches	250	mA
NOTE: I_{VDDO_A}, I_{VDDO_B}, and I_{VDDO_C} can be reduced to equal I_{LCD} when the MPP pins are configured to support the LCD interface.				
SERDES interface	I_{SRD_AVDD}	For a single SERDES port	60	mA
USB interface	I_{USB_AVDD}	For three ports	30	mA
	I_{USB_AVDDL}		100	mA
RTC Interface	I_{RTC_AVDD}	3V battery supply	4	uA
		3.3V battery supply	5	uA
MPP **NOTE:** All MPP pins are configured as GPIOs and consume the current as tested in Section 9.6.1, General 3.3V (CMOS) DC Electrical Specifications, on page 100.	I_{VDDO_A}	MPP[11:0], GE_MDC, GE_MDIO	96	mA
	I_{VDDO_B}	MPP[23:12]	96	mA
	I_{VDDO_C}	MPP[35:24]	96	mA
	I_{VDDO_D}	MPP[47:36]	96	mA
	I_{VDDO_DEV}	MPP[48] and Device interface	50	mA
Miscellaneous Signals	I_{VDDO_MISC}	3.3V JTAG, UART, TWSI, SPI, and reset signals	40	mA
VHV (eFuse) Power Supply	I_{VHV}	1.8V for programming	30	mA
PLL	$I_{CORE\_TDM\_PLL\_AVDD}$	1.8V Core PLL and TDM PLL	20	mA
	$I_{CPU\_PLL\_AVDD}$	1.8V CPU PLL	20	mA
XTAL	I_{XTAL_AVDD}	1.8V XTAL	50	mA
LVDS	I_{VDDO_FPD}	1.8V Flat Panel Display	40	mA
AVS	$I_{AVS\_SSCG\_AVDD}$	1.8V SSCG, CPU AVS, and Core AVS blocks	25	mA

Notes:

1. Trace is 3 inches, unless otherwise specified.
2. Current in mA is calculated using maximum recommended voltage specification for each power rail.
3. All output clocks toggling at their specified rate.
4. Maximum drawn current from the power supply.
5. The typical RTC_AVDD current at 3V is 1.5 uA.

9.6 DC Electrical Specifications

Note See the Pin Description Section for internal pullup/pulldown information.

9.6.1 General 3.3V (CMOS) DC Electrical Specifications

The DC electrical specifications in Table 45 are applicable for the following interfaces and signals:

- Device
- JTAG
- MPP
- SMI
- UART
- SYSRSTn
- SYSRST_OUTn
- MRn
- CDRn

Table 45: General 3.3V Interface (CMOS) DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL		-0.3		0.8	V	-
Input high level	VIH		2.0		VDDIO+0.3	V	-
Output low level	VOL	IOL = 8 mA	-		0.6	V	-
Output high level	VOH	IOH = -8 mA	2.2		-	V	-
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

1. While I/O is in High-Z.
2. This current does not include the current flowing through the pullup/pulldown resistor.

9.6.2 General 2.5V (CMOS) DC Electrical Specifications

The DC electrical specifications in Table 46 are applicable for the following interfaces and signals:

- MPP[23:0]
- SMI

Table 46: General 2.5V Interface (CMOS) DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL		-0.3		0.7	V	-
Input high level	VIH		1.7		VDDIO+0.3	V	-
Output low level	VOL	IOL = 8 mA	-		0.6	V	-
Output high level	VOH	IOH = -8 mA	1.8		-	V	-
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

1. While I/O is in High-Z.
2. This current does not include the current flowing through the pullup/pulldown resistor.

9.6.3 General 1.8V (CMOS) DC Electrical Specifications

The DC electrical specifications in Table 47 are applicable for the following interfaces and signals:

- eFuse
- MPP[35:0]
- Device Bus

Table 47: General 1.8V Interface (CMOS) DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL		-0.3		0.35*VDDIO	V	-
Input high level	VIH		0.65*VDDIO		VDDIO+0.3	V	-
Output low level	VOL	IOL = 8 mA	-		0.45	V	-
Output high level	VOH	IOH = -8 mA	VDDIO-0.45		-	V	-
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

1. While I/O is in High-Z.
2. This current does not include the current flowing through the pullup/pulldown resistor.

9.6.4 Flat Panel Display (LVDS) DC Electrical Specifications

Table 48: Flat Panel Display Interface (LVDS) DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Output high level single ended	VOH	RL = 50 Ohm			1550	mV	-
Output low level single ended	VOL	RL = 50 Ohm	850			mV	-
Output differential voltage	VOD	RL = 50 Ohm	500		900	mV	-
Output common mode voltage	VOS	RL = 50 Ohm	1050		1350	mV	-
Input leakage current	IIL	0 < VIN < VDDIO	-20		20	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

1. While I/O is in High-Z.
2. This current does not include the current flowing through the pullup/pulldown resistor.

9.6.5 SDRAM DDR3 (1.5V) Interface DC Electrical Specifications

Note VDDIO refers to the VDDO_M pin.

Table 49: SDRAM DDR3 (1.5V) Interface DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Single ended input low level	VIL		-0.3		VDDIO/2 - 0.100	V	-
Single ended input high level	VIH		VDDIO/2 + 0.100		VDDIO + 0.3	V	-
Differential input low level	VDIL		Note 6		-0.2	V	6
Differential input high level	VDIH		0.2		Note 6	V	6
Output low level	VOL	IOL = 8.8 mA			0.2*VDDIO	V	7
Output high level	VOH	IOH = -8.8 mA	0.8*VDDIO			V	7
Rtt effective impedance value	RTT	See note 2	50	60	70	ohm	1 , 2
Deviation of VM with respect to VDDIO/2	dVm	See note 3	-5		5	%	3
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	4, 5
Pin capacitance	Cpin	-		5		pF	-

Notes:

1. See SDRAM functional description section for ODT configuration.
2. Measurement definition for RTT: Apply (VDDIO/2) +/- 0.15 to input pin separately, then measure current $I_{(VDDIO/2+0.15)}$ and $I_{(VDDIO/2-0.15)}$ respectively.

$$RTT = \frac{0.30}{I_{(\frac{VDDIO}{2}+0.15)} - I_{(\frac{VDDIO}{2}-0.15)}}$$

3. Measurement definition for VM: Measured voltage (VM) at input pin (midpoint) with no load.

$$dVM = \left(\frac{2 \times Vm}{VDDIO} - 1\right) \times 100\%$$

4. While I/O is in High-Z.
5. This current does not include the current flowing through the pullup/pulldown resistor.
6. Limitations are same as for single ended signals.
7. Defined when driver impedance is calibrated to 35 ohms.

9.6.6 SDRAM DDR3L (1.35V) Interface DC Electrical Specifications

Note

- VDDIO refers to the VDDO_M pin.
- VREF is VDDO_M/2.

Table 50: SDRAM DDR3L (1.35V) Interface DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Single ended input low level	VIL		-0.3		VDDIO/2 - 0.09	V	-
Single ended input high level	VIH		VDDIO/2 + 0.09		VDDIO + 0.3	V	-
Differential input low level	VDIL		Note 6		-0.16	V	6
Differential input high level	VDIH		0.16		Note 6	V	6
Output low level	VOL	IOL = 8.8 mA			0.2*VDDIO	V	7
Output high level	VOH	IOH = -8.8 mA	0.8*VDDIO			V	7
Rtt effective impedance value	RTT	See note 2	50	60	70	ohm	1 , 2
Deviation of VM with respect to VDDIO/2	dVm	See note 3	-5		5	%	3
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	4, 5
Pin capacitance	Cpin	-		5		pF	-

Notes:

1. See SDRAM functional description section for ODT configuration.
2. Measurement definition for RTT: Apply (VDDIO/2) +/- 0.15 to input pin separately, then measure current $I_{(VDDIO/2+0.15)}$ and $I_{(VDDIO/2-0.15)}$ respectively.

$$RTT = \frac{0.30}{I_{(\frac{VDDIO}{2}+0.15)} - I_{(\frac{VDDIO}{2}-0.15)}}$$

3. Measurement definition for VM: Measured voltage (VM) at input pin (midpoint) with no load.

$$dVM = \left(\frac{2 \times Vm}{VDDIO} - 1\right) \times 100\%$$

4. While I/O is in High-Z.
5. This current does not include the current flowing through the pullup/pulldown resistor.
6. Limitations are same as for single ended signals.
7. Defined when driver impedance is calibrated to 35 ohms.

9.6.7 I²C Interface 3.3V DC Electrical Specifications

Table 51: I²C Interface 3.3V DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL		-0.5		0.3*VDDIO	V	-
Input high level	VIH		0.7*VDDIO		VDDIO+0.5	V	-
Output low level	VOL	IOL = 3 mA	-		0.4	V	-
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

1. While I/O is in High-Z.
2. This current does not include the current flowing through the pullup/pulldown resistor.

9.6.8 Serial Peripheral Interface (SPI) 3.3V DC Electrical Specifications

Table 52: SPI Interface 3.3V DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL		-0.5		0.3*VDDIO	V	-
Input high level	VIH		0.7*VDDIO		VDDIO+0.5	V	-
Output low level	VOL	IOL = 4 mA	-		0.4	V	-
Output high level	VOH	IOH = -4 mA	VDDIO-0.6		-	V	-
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

1. While I/O is in High-Z.
2. This current does not include the current flowing through the pullup/pulldown resistor.

9.6.9 Time Division Multiplexing (TDM) 3.3V DC Electrical Specifications

Table 53: TDM Interface 3.3V DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL		-0.5		0.3*VDDIO	V	-
Input high level	VIH		0.7*VDDIO		VDDIO+0.5	V	-
Output low level	VOL	IOL = 4 mA	-		0.4	V	-
Output high level	VOH	IOH = -4 mA	VDDIO-0.6		-	V	-
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

1. While I/O is in High-Z.
2. This current does not include the current flowing through the pullup/pulldown resistor.

9.6.10 NAND Flash 3.3V DC Electrical Specification

Note VDDIO refers to the VDDO_DEV pin.

Table 54: NAND Flash 3.3V DC Electrical Specification

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL		-0.3		0.8	V	-
Input high level	VIH		2.0		VDDIO+0.3	V	-
Output low level	VOL	IOL = 2 mA	-		0.4	V	-
Output high level	VOH	IOH = -2 mA	0.85 * VDDIO		-	V	-
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

1. While I/O is in High-Z.
2. This current does not include the current flowing through the pullup/pulldown resistor.

9.6.11 NAND Flash 1.8V DC Electrical Specification

Note

VDDIO refers to the VDDO_DEV pin.

Table 55: NAND Flash 1.8V DC Electrical Specification

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	Notes
Input low level	VIL		-0.3		0.35*VDDIO	V	-
Input high level	VIH		0.65*VDDIO		VDDIO+0.3	V	-
Output low level	VOL	IOL = 2 mA	-		0.45	V	-
Output high level	VOH	IOH = -2 mA	0.85 * VDDIO		-	V	-
Input leakage current	IIL	0 < VIN < VDDIO	-10		10	uA	1, 2
Pin capacitance	Cpin			5		pF	-

Notes:

1. While I/O is in High-Z.
2. This current does not include the current flowing through the pullup/pulldown resistor.

9.7 AC Electrical Specifications

See Section 9.8, Differential Interface Electrical Characteristics, on page 145 for differential interface specifications.

9.7.1 Reference Clock and Reset AC Timing Specifications

Table 56: Reference Clock and Reset AC Timing Specifications

Description	Symbol	Min	Max	Units	Notes
CPU and Core Reference Clock					
Frequency	$F_{REF\_CLK\_XIN}$	25		MHz	
Accuracy	$PPM_{REF\_CLK\_XIN}$	-50	50	PPM	
Duty cycle	$DC_{REF\_CLK\_XIN}$	40	60	%	
Slew rate	$SR_{REF\_CLK\_XIN}$	0.5		V/ns	1
		0.7		V/ns	1, 2
Pk-Pk jitter	$JR_{REF\_CLK\_XIN}$		120	ps	2, 5
			200	ps	
Reference Clock Out					
Frequency	F_{REFCLK_OUT}	25		MHz	
Accuracy	PPM_{REFCLK_OUT}	-50	50	PPM	
Duty cycle	DC_{REFCLK_OUT}	$DC_{REF\_CLK\_XIN - 5\%}$	$DC_{REF\_CLK\_XIN + 5\%}$	%	3, 4
Pk-Pk jitter	JR_{REFCLK_OUT}		$JR_{REF\_CLK\_XIN + 50\ ps}$	ps	2, 3, 5
Ethernet Interface in MII/MMII-Mac mode					
Frequency	F_{GE0_TXCLK}	2.5	50	MHz	
	F_{GE0_RXCLK}				
Accuracy	PPM_{GE0_TXCLK}	-100	100	PPM	
	PPM_{GE0_RXCLK}				
Duty cycle	DC_{GE0_TXCLK}	35	65	%	
	DC_{GE0_RXCLK}				
Slew rate	SR_{GE0_TXCLK}	0.7		V/ns	1
	SR_{GE0_RXCLK}				
SMI Clock					
SMI output MDC clock	F_{GE_MDC}	TCLK/128	TCLK/8	MHz	

Table 56: Reference Clock and Reset AC Timing Specifications

Description	Symbol	Min	Max	Units	Notes
I^2C Master Mode Clock					
SCK output clock	F_{TWSI0_SCK} F_{TWSI1_SCK}		100	kHz	7
SPI Output Clock					
SPI output clock	F_{SPI0_SCK} F_{SPI1_SCK}	TCLK/1920	50	MHz	8
DEV_CLK_OUT Reference Clock					6
Frequency	$F_{DEV\_CLK\_OUT}$	TCLK/15	TCLK/4	MHz	
Duty cycle	$DC_{DEV\_CLK\_OUT}$	40	60	%	4
PTP Reference Clock					
Frequency	F_{PTP_CLK}	12.5	125	MHz	
Accuracy	PPM_{PTP_CLK}	-100	100	PPM	
Duty cycle	DC_{PTP_CLK}	40	60	%	
Slew rate	SR_{PTP_CLK}	0.7		V/ns	1
Pk-Pk jitter	JR_{PTP_CLK}		100	ps	
LCD Reference Clock					
Frequency	$F_{LCD\_EXT\_REF\_CLK}$	2.5	27	MHz	
Accuracy	$PPM_{LCD\_EXT\_REF\_CLK}$	-50	50	PPM	
Clock duty cycle	$DC_{LCD\_EXT\_REF\_CLK}$	45	55	%	
Slew rate	$SR_{LCD\_EXT\_REF\_CLK}$	0.7		V/ns	1
Pk-Pk jitter	$JR_{LCD\_EXT\_REF\_CLK}$		150	ps	
LCD Output Clock					
LCD Output Frequency	F_{LCD_CLK}		100	MHz	
RTC Reference Clock					
RTC_XIN crystal frequency	F_{RTC_XIN}	32.768		kHz	9
MMC Reference Clock					
Frequency	F_{SD0_CLK}		50	MHz	
JTAG Reference Clock					
Frequency	F_{JT_CLK}		15	MHz	

Table 56: Reference Clock and Reset AC Timing Specifications

Description	Symbol	Min	Max	Units	Notes
Reset Specifications					
Refer to Section 7, Reset and Initialization, on page 76.					

Notes:

1. Slew rate is defined from 20% to 80% of the reference clock signal.
2. This value is required when using the internal PLL to drive the SERDES.
3. The REFCLK_OUT duty cycle/jitter is driven by the REF_CLK_XIN duty cycle/jitter. There is a 5% degradation of the output duty cycle. There is a 50 ps degradation of the output jitter.
4. The load is CL = 15 pF.
5. This value is assumed to contain above 95% random components characterized by 1/f behavior, defined with a BER = 1e-12.
6. It is possible to use this reference clock when working in source synchronous device bus mode.
7. For additional information regarding configuring this clock, see the Inter-Integrated Circuit Registers in the device's *Functional Specification*.
8. For additional information regarding configuring this clock, see the SPI Interface Configuration Register in the device's *Functional Specification*.
9. The RTC design was optimized for a standard CL = 12.5 pF crystal. No passive components are provided internally. Connect the crystal and the passive network as recommended by the crystal manufacturer.

Figure 10: DEV_CLK_OUT and REFCLK_OUT Reference Clock Test Circuit

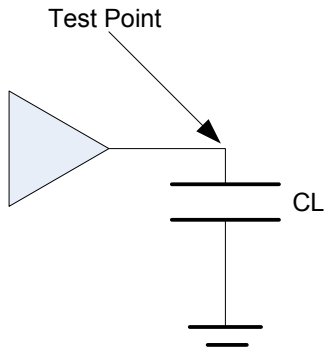
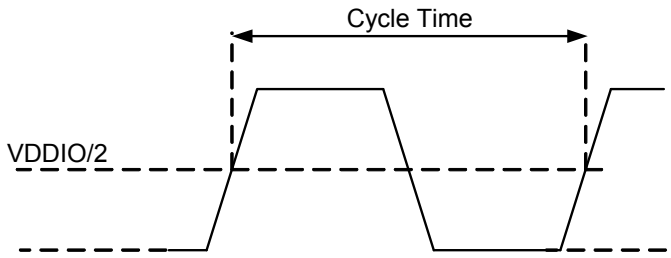


Figure 11: DEV_CLK_OUT and REFCLK_OUT AC Timing Diagram



9.7.2 Flat Panel Display (FPD) Interface AC Timing

Note

Before designing a system implementing the Flat Panel Display (FPD) interface, contact a Marvell® Field Applications Engineer (FAE).

9.7.2.1 FPD AC Timing Table

Table 57: FPD AC Timing Table

Description	Symbol	Min	Max	Units	Notes
Transmitter output clock frequency	fCK	-	65	MHz	1
Transmitter clock jitter cycle-to-cycle	tJCC	-	0.23	ns	-
Transmitter clock output rise/fall time	tR/tF	-	1.5	ns	2
Transmitter output pulse position for Bit 0	tPPos0	-0.2	0.2	ns	-
Transmitter output pulse position for Bit 1	tPPos1	1/7*tCK - 0.2	1/7*tCK + 0.2	ns	-
Transmitter output pulse position for Bit 2	tPPos2	2/7*tCK - 0.2	2/7*tCK + 0.2	ns	-
Transmitter output pulse position for Bit 3	tPPos3	3/7*tCK - 0.2	3/7*tCK + 0.2	ns	-
Transmitter output pulse position for Bit 4	tPPos4	4/7*tCK - 0.2	4/7*tCK + 0.2	ns	-
Transmitter output pulse position for Bit 5	tPPos5	5/7*tCK - 0.2	5/7*tCK + 0.2	ns	-
Transmitter output pulse position for Bit 6	tPPos6	6/7*tCK - 0.2	6/7*tCK + 0.2	ns	-
Transmitter channel-to-channel skew	tCCS	-	0.25	ns	-

Notes:

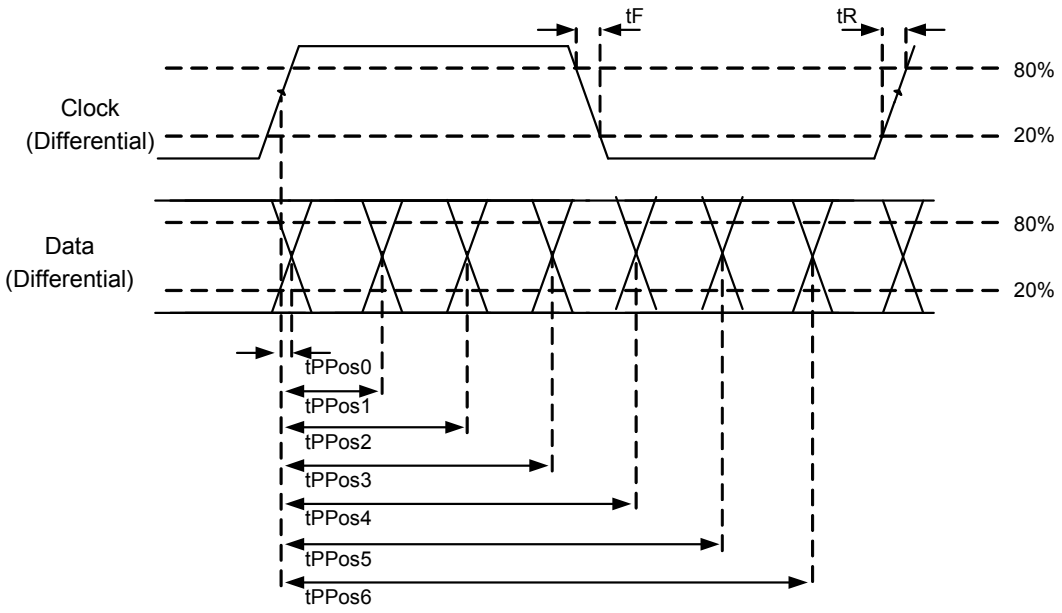
General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

General comment: tCK = 1/fCK.

1. See functional specification for available operating frequencies.
2. Defined from 20% to 80% of the transition.

9.7.2.2 FPD AC Timing Diagram

Figure 12: FPD AC Timing Diagram



9.7.3 Liquid Crystal Display Interface AC Timing

Note Before designing a system implementing the Liquid Crystal Display (LCD) interface, contact a Marvell® Field Applications Engineer (FAE).

9.7.3.1 LCD AC Timing Table

Table 58: LCD AC Timing Table

Description	Symbol	Min	Max	Units	Notes
DCLK clock frequency	fCK	See note 2		MHz	2
DCLK clock high time	tWCH	0.45	0.55	tCK	1
DCLK clock low time	tWCL	0.45	0.55	tCK	1
Output Data & Data Enable invalid relative to DCLK rise time	tOIV	-1.25	1.25	ns	1, 3
Output Data & Data Enable valid granularity	tOVG	-	0.1	ns	1, 3

Notes:

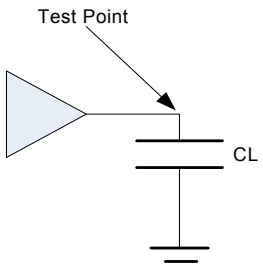
General comment: General comment: All values were measured from vddio/2 to vddio/2, unless otherwise specified.

General comment: tCK = 1/fCK.

1. For all signals, the load is CL = 10 pF.
2. See "Reference Clocks" table for more details.
3. The granularity should be considered when changing default data window position.
   See functional specification for more information.

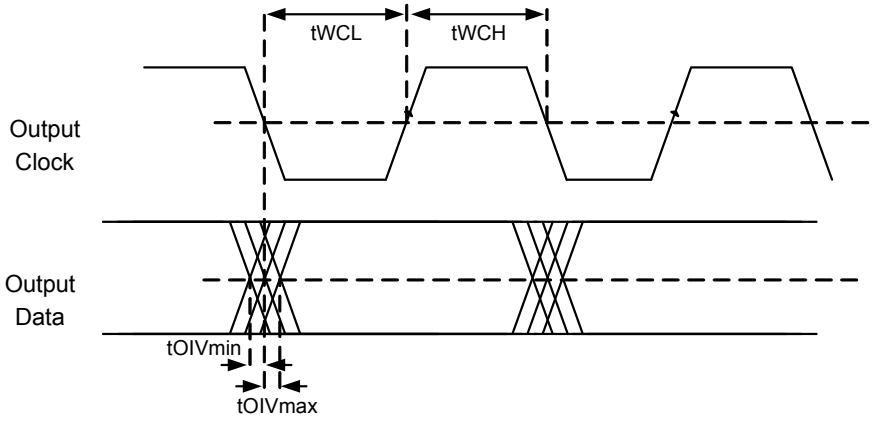
9.7.3.2 LCD Test Circuit

Figure 13: LCD Test Circuit



9.7.3.3 LCD AC Timing Diagram

Figure 14: LCD Transmit AC Timing Diagram



9.7.4 Reduced Gigabit Media Independent Interface (RGMII) AC Timing

9.7.4.1 RGMII AC Timing Table

Table 59: RGMII AC Timing Table

Description	Symbol	Min	Max	Units	Notes
Clock frequency	fCK	125.0		MHz	-
Data to Clock output skew	Tskew T	-0.50	0.50	ns	2
Data to Clock input skew	Tskew R	1.00	2.60	ns	-
Clock cycle duration	Tcyc	7.20	8.80	ns	1 , 2
Duty cycle for Gigabit	Duty_G	0.45	0.55	tCK	2
Duty cycle for 10/100 Megabit	Duty_T	0.40	0.60	tCK	2

Notes:

General comment: All values were measured from vddio/2 to vddio/2, unless otherwise specified.

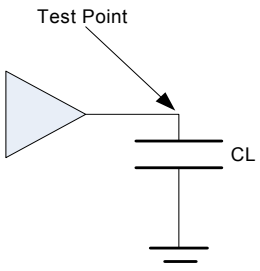
General comment: tCK = 1/fCK.

General comment: If the PHY does not support internal-delay mode, the PC board design requires routing clocks so that an additional trace delay of greater than 1.5 ns and less than 2.0 ns is added to the associated clock signal.
For 10/100 Mbps RGMII, the Max value is unspecified.

1. For RGMII at 10 Mbps and 100 Mbps, Tcyc will scale to 400 ns +/-40 ns and 40 ns +/-4 ns, respectively.
2. For all signals, the load is CL = 5 pF.

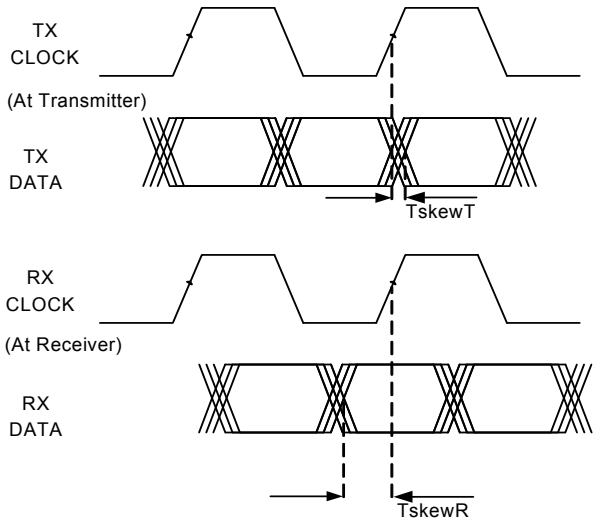
9.7.4.2 RGMII Test Circuit

Figure 15: RGMII Test Circuit



9.7.4.3 RGMII AC Timing Diagram

Figure 16: RGMII AC Timing Diagram



9.7.5 Gigabit Media Independent Interface (GMII) AC Timing

9.7.5.1 GMII AC Timing Table

Table 60: GMII AC Timing Table

Description	Symbol	125 MHz		Units	Notes
		Min	Max		
GTX_CLK cycle time	tCK	7.5	8.5	ns	-
RX_CLK cycle time	tCKrx	7.5	-	ns	-
GTX_CLK and RX_CLK high level width	tHIGH	2.5	-	ns	1
GTX_CLK and RX_CLK low level width	tLOW	2.5	-	ns	1
GTX_CLK and RX_CLK rise time	tR	-	1.0	ns	1, 2
GTX_CLK and RX_CLK fall time	tF	-	1.0	ns	1, 2
Data input setup time relative to RX_CLK rising edge	tSETUP	2.0	-	ns	-
Data input hold time relative to RX_CLK rising edge	tHOLD	0.0	-	ns	-
Data output valid before GTX_CLK rising edge	tOVB	2.5	-	ns	1
Data output valid after GTX_CLK rising edge	tOVA	0.5	-	ns	1

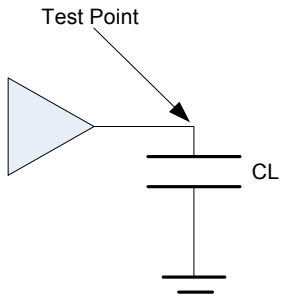
Notes:

General comment: All values were measured from VIL(max) to VIH(min), unless otherwise specified.

1. For all signals, the load is CL = 5 pF.
2. Rise time measured from VIL(max) to VIH(min), fall time measured from VIH(min) to VIL(max).

9.7.5.2 GMII Test Circuit

Figure 17: GMII Test Circuit



9.7.5.3 GMII AC Timing Diagrams

Figure 18: GMII Output AC Timing Diagram

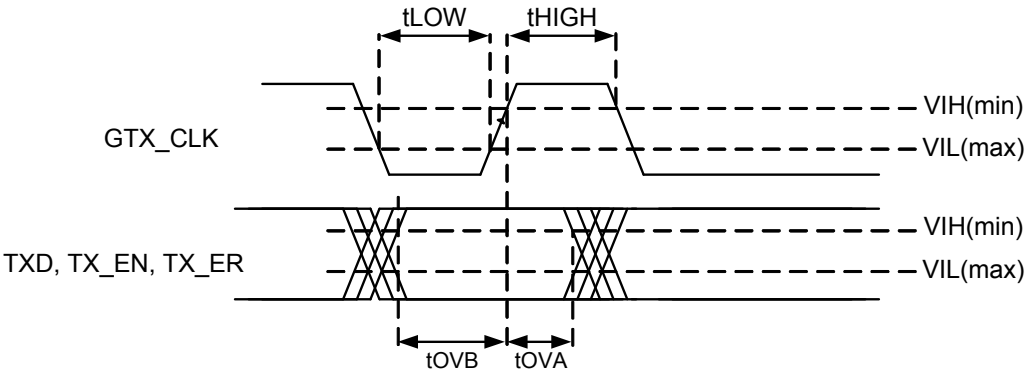
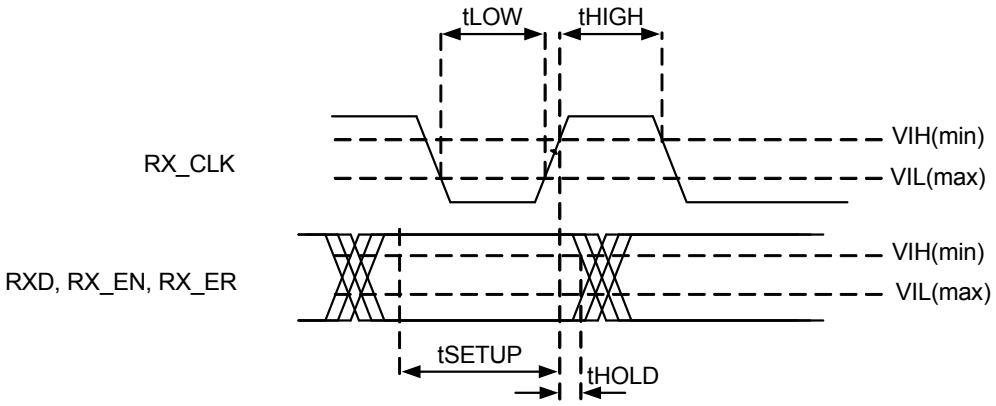


Figure 19: GMII Input AC Timing Diagram



9.7.6 Media Independent Interface (MII/MMII) AC Timing

9.7.6.1 MII/MMII MAC Mode AC Timing Table

Table 61: MII/MMII MAC Mode AC Timing Table

Description	Symbol	Min	Max	Units	Notes
Data input setup relative to RX_CLK rising edge	tSU	3.5	-	ns	-
Data input hold relative to RX_CLK rising edge	tHD	2.0	-	ns	-
Data output delay relative to MII_TX_CLK rising edge	tOV	0.0	10.0	ns	1

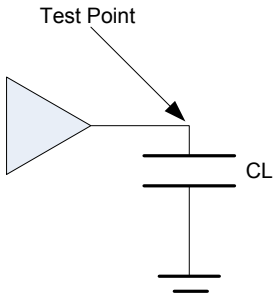
Notes:

General comment: All values were measured from VIL(max) to VIH(min), unless otherwise specified.

1. For all signals, the load is CL = 5 pF.

9.7.6.2 MII/MMII MAC Mode Test Circuit

Figure 20: MII/MMII MAC Mode Test Circuit



9.7.6.3 MII/MMII MAC Mode AC Timing Diagrams

Figure 21: MII/MMII MAC Mode Output Delay AC Timing Diagram

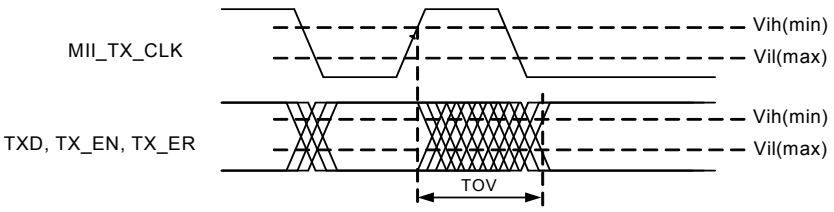
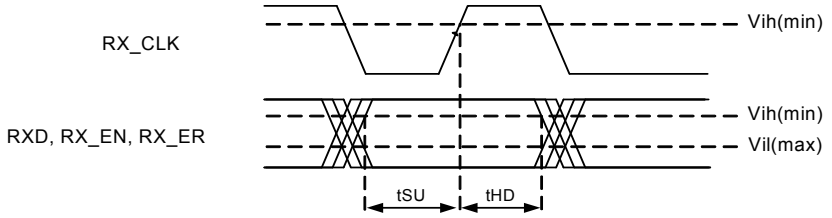


Figure 22: MII/MMII MAC Mode Input AC Timing Diagram



9.7.7 Serial Management Interface (SMI) AC Timing

9.7.7.1 SMI Master Mode AC Timing Table

Table 62: SMI Master Mode AC Timing Table

Description	Symbol	Min	Max	Units	Notes
MDC clock frequency	fCK	See note 2		MHz	2
MDC clock duty cycle	tDC	0.4	0.6	tCK	-
MDIO input setup time relative to MDC rise time	tSU	12.0	-	ns	-
MDIO input hold time relative to MDC rise time	tHO	0.0	-	ns	3
MDIO output valid before MDC rise time	tOVB	12.0	-	ns	1
MDIO output valid after MDC rise time	tOVA	12.0	-	ns	1

Notes:

General comment: All timing values were measured from VIL(max) and VIH(min) levels, unless otherwise specified.

General comment: tCK = 1/fCK.

1. For all signals, the load is CL = 10 pF.
2. See "Reference Clocks" table for more details.
3. For this parameter, the load is CL = 2 pF.

9.7.7.2 SMI Master Mode Test Circuit

Figure 23: MDIO Master Mode Test Circuit

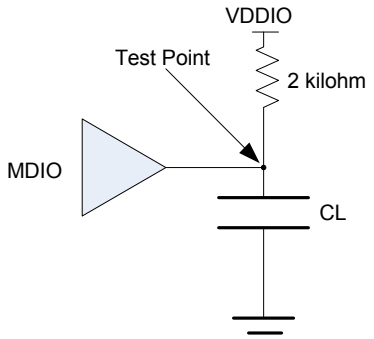
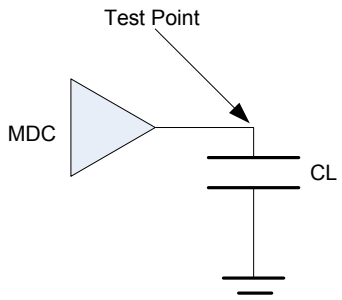


Figure 24: MDC Master Mode Test Circuit



9.7.7.3 SMI Master Mode AC Timing Diagrams

Figure 25: SMI Master Mode Output AC Timing Diagram

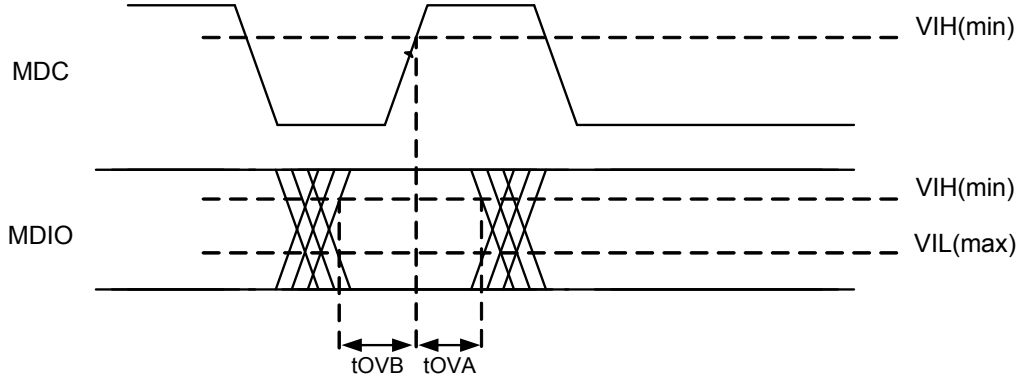
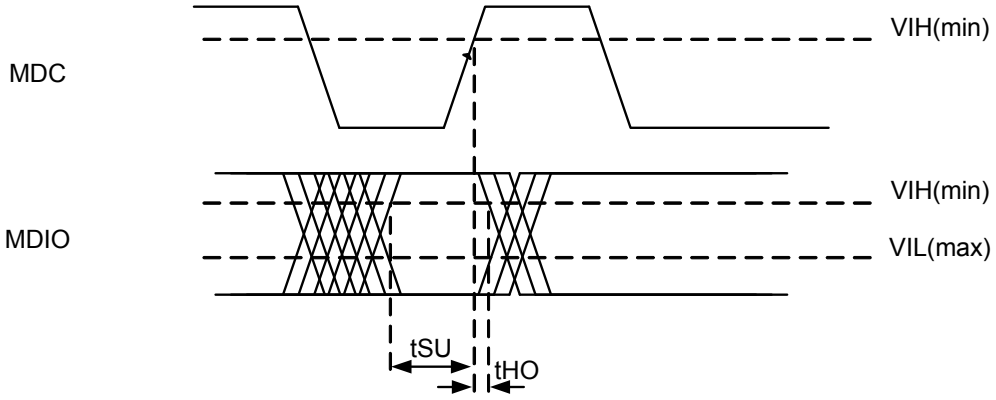


Figure 26: SMI Master Mode Input AC Timing Diagram



9.7.8 SDRAM DDR3 Interface AC Timing

9.7.8.1 SDRAM DDR3 Interface Timing Tables

Note The timing values in the following table are based on a tuning algorithm that runs automatically during the device initialization. For more information, contact your local Marvell® representative.

Table 63: SDRAM DDR3 (667 MHz) Interface AC Timing Table

Description	Symbol	667 MHz		Units	Notes
		Min	Max		
Clock frequency	fCK	667.0		MHz	-
DQ and DM valid output time before DQS transition	tDOVB	215	-	ps	-
DQ and DM valid output time after DQS transition	tDOVA	215	-	ps	-
CLK-CLKn Period Jitter	tJIT(per)	-80	80	ps	1
DQS falling edge setup time to CLK-CLKn rising edge	tDSS	0.34	-	tCK(avg)	-
DQS falling edge hold time from CLK-CLKn rising edge	tDSH	0.34	-	tCK(avg)	-
DQS latching rising transitions to associated clock edges	tDQSS	-0.11	0.11	tCK(avg)	-
Address and Control valid output time before CLK-CLkn rising edge	tAOVB	440	-	ps	2
Address and Control valid output time after CLK-CLKn rising edge	tAOVA	450	-	ps	2
DQ input setup time relative to DQS in transition	tDSI	-275	-	ps	-
DQ input hold time relative to DQS in transition	tDHI	475	-	ps	-

Notes:

General comment: All timing values are defined from VREF to VREF, unless otherwise specified.

General comment: All input timing values assume minimum slew rate of 1 V/ns (slew rate defined from VREF +/-100 mV).

General comment: All timing parameters with DQS signal are defined on DQS-DQSn crossing point.

General comment: All timing parameters with CLK signal are defined on CLK-CLKn crossing point.

General comment: For all signals, the load is CL = 10 pF.

General comment: tCK = 1/fCK.

1. tJIT(per) = Min/max of {tCKi - tCK where i = 1 to 200}.

2. This timing value is defined when Address and Control signals are output on CLK-CLKn falling edge.

Note The timing values in the following table are based on a tuning algorithm that runs automatically during device initialization. For more information, contact your local Marvell® representative.

Table 64: SDRAM DDR3 (800 MHz) Interface AC Timing Table

Description	Symbol	800 MHz		Units	Notes
		Min	Max		
Clock frequency	fCK	800.0		MHz	-
DQ and DM valid output time before DQS transition	tDOVB	185	-	ps	-
DQ and DM valid output time after DQS transition	tDOVA	185	-	ps	-
CLK-CLKn Period Jitter	tJIT(per)	-70	70	ps	1
DQS falling edge setup time to CLK-CLKn rising edge	tDSS	0.32	-	tCK(avg)	-
DQS falling edge hold time from CLK-CLKn rising edge	tDSH	0.32	-	tCK(avg)	-
DQS latching rising transitions to associated clock edges	tDQSS	-0.13	0.13	tCK(avg)	-
Address and Control valid output time before CLK-CLKn rising edge	tAOVB	420	-	ps	2
Address and Control valid output time after CLK-CLKn rising edge	tAOVA	350	-	ps	2
DQ input setup time relative to DQS in transition	tDSI	-260	-	ps	-
DQ input hold time relative to DQS in transition	tDHI	365	-	ps	-

Notes:

General comment: All timing values are defined from VREF to VREF, unless otherwise specified.

General comment: All input timing values assume minimum slew rate of 1 V/ns (slew rate defined from VREF +/-100 mV).

General comment: All timing parameters with DQS signal are defined on DQS-DQSn crossing point.

General comment: All timing parameters with CLK signal are defined on CLK-CLKn crossing point.

General comment: For all signals, the load is CL = 4.6 pF.

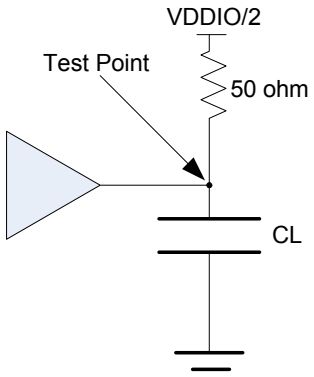
General comment: tCK = 1/fCK.

1. tJIT(per) = Min/max of {tCKi - tCK where i = 1 to 200}.

2. This timing value is defined when Address and Control signals are output on CLK-CLKn falling edge.

9.7.8.2 SDRAM DDR3 Interface Test Circuit

Figure 27: SDRAM DDR3 Interface Test Circuit



9.7.8.3 SDRAM DDR3 Interface AC Timing Diagrams

Figure 28: SDRAM DDR3 Interface Write AC Timing Diagram

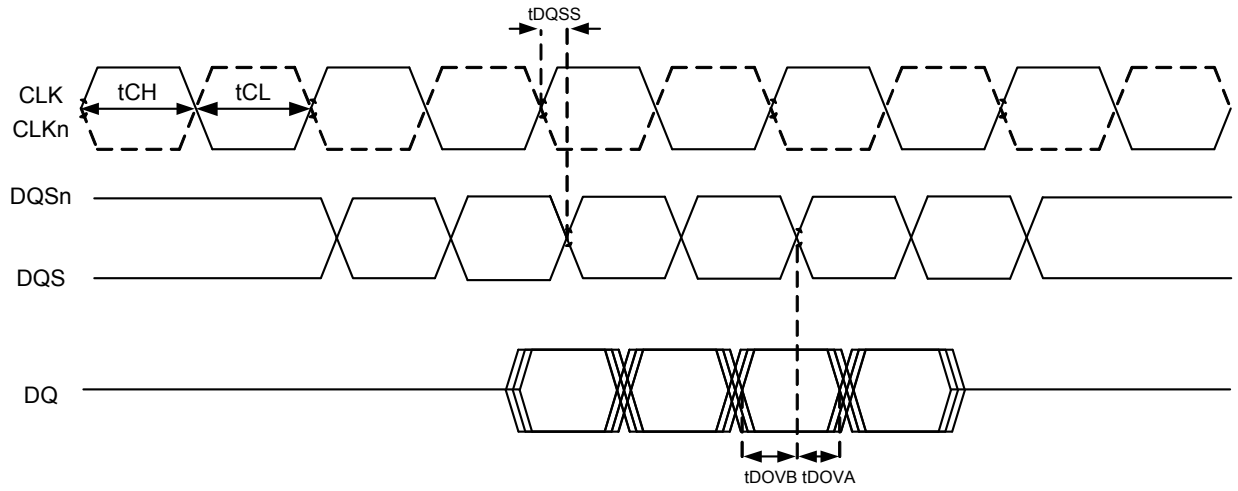


Figure 29: SDRAM DDR3 Interface Address and Control AC Timing Diagram

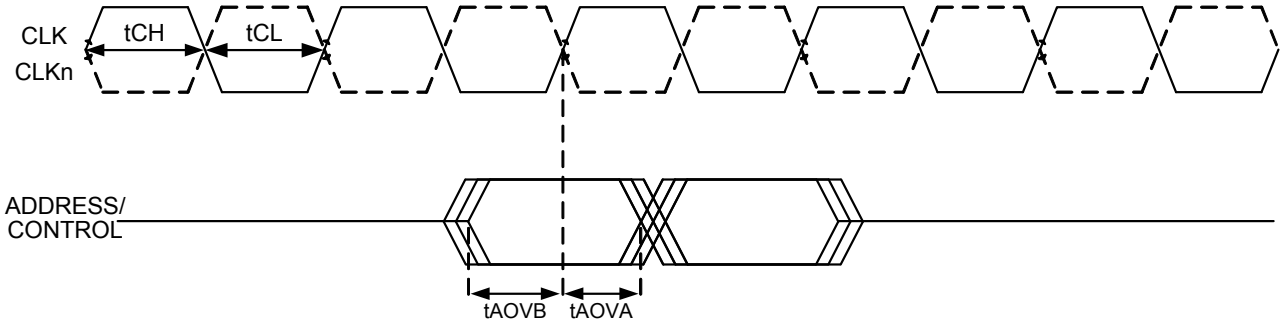
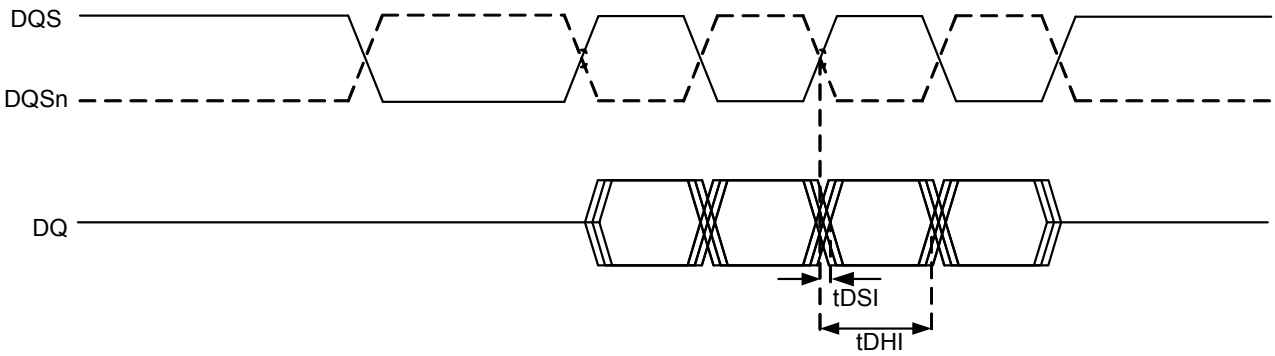


Figure 30: SDRAM DDR3 Interface Read AC Timing Diagram



9.7.9 Secure Digital Input/Output (SDIO) Interface AC Timing

9.7.9.1 Secure Digital Input/Output (SDIO) AC Timing Table

Table 65: SDIO Host in High-Speed Mode AC Timing Table

Description	Symbol	Min	Max	Units	Notes
Clock frequency in Data Transfer Mode	fCK	0	50	MHz	-
Clock high/low level pulse width	tWL/tWH	0.35	-	tCK	1, 3
Clock rise/fall time	tTLH/tTHL	-	3.0	ns	1, 3
CMD, DAT output valid before CLK rising edge	tDOVB	6.5	-	ns	2, 3
CMD, DAT output valid after CLK rising edge	tDOVA	2.5	-	ns	2, 3
CMD, DAT input setup relative to CLK rising edge	tISU	7.0	-	ns	2
CMD, DAT input hold relative to CLK rising edge	tIHD	0.0	-	ns	2, 4

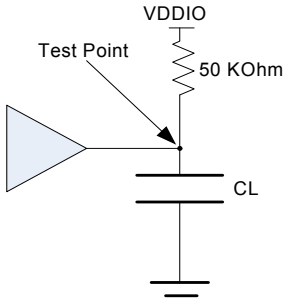
Notes:

General comment: tCK = 1/fCK.

1. Defined on VIL(max) and VIH(min) levels.
2. Defined on VDDIO/2 for Clock signal, and VIL(max) / VIH(min) for CMD & DAT signals.
3. For all signals, the load is CL = 10 pF.
4. For this parameter, the load is CL = 2 pF.

9.7.9.2 Secure Digital Input/Output (SDIO) Test Circuit

Figure 31: Secure Digital Input/Output (SDIO) Test Circuit



9.7.9.3 Secure Digital Input/Output (SDIO) AC Timing Diagrams

Figure 32: SDIO Host in High Speed Mode Output AC Timing Diagram

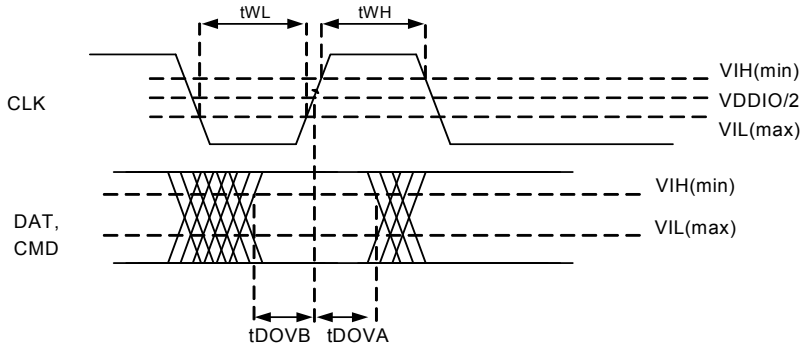
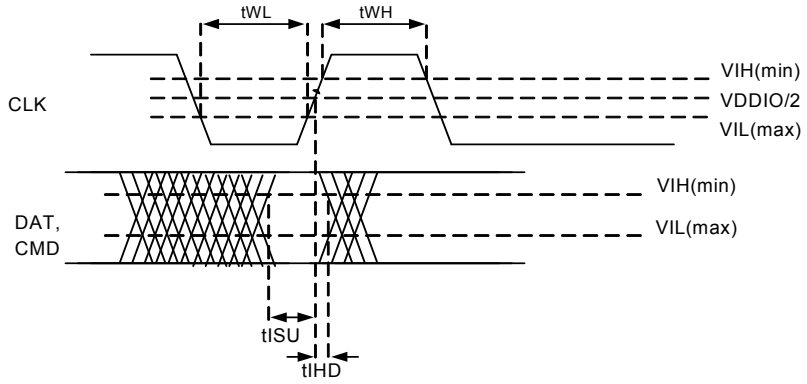


Figure 33: SDIO Host in High Speed Mode Input AC Timing Diagram



9.7.10 Multimedia Card (MMC) Interface AC Timing

9.7.10.1 MMC AC Timing Table

Table 66: MMC Host AC Timing Table

Description	Symbol	Min	Max	Units	Notes
Clock frequency in Data Transfer mode	fCK	See note 5		MHz	5
Clock high/low level pulse width	tWL/tWH	0.34	-	tCK	1, 3
Clock rise/fall time	tTLH/tTHL	-	3.0	ns	1, 3
CMD, DAT output valid before CLK rising edge	tDOVB	3.5	-	ns	2, 3
CMD, DAT output valid after CLK rising edge	tDOVA	3.5	-	ns	2, 3
CMD, DAT input setup relative to CLK rising edge	tISU	6.5	-	ns	2
CMD, DAT input hold relative to CLK rising edge	tIHD	0.0	-	ns	2, 4

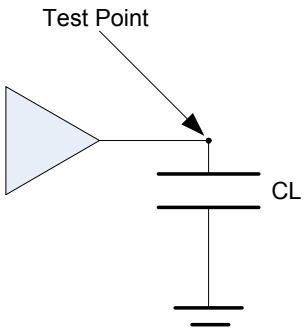
Notes:

General comment: tCK = 1/fCK.

1. Defined on VIL(max) and VIH(min) levels.
2. Defined on VDDIO/2 for Clock signal, and VIL(max) / VIH(min) for CMD and DAT signals.
3. For all signals, the load is CL = 10 pF.
4. For this parameter, the load is CL = 2 pF.
5. See "Reference Clocks" table for more details.

9.7.10.2 MMC Test Circuit

Figure 34: MMC Test Circuit



9.7.10.3 MMC AC Timing Diagrams

Figure 35: MMC High-Speed Host Output AC Timing Diagram

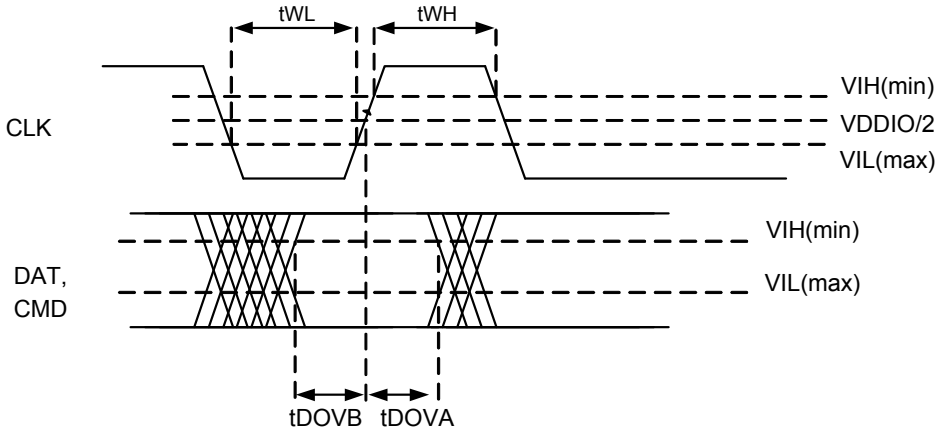
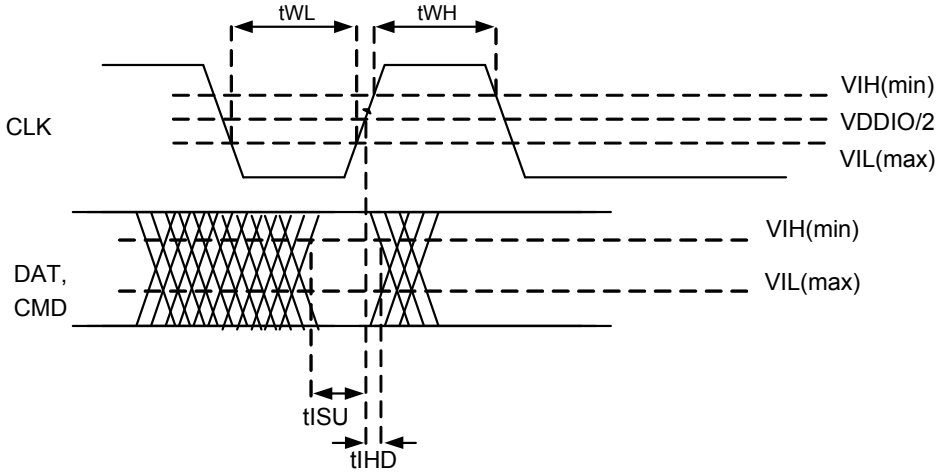


Figure 36: MMC High-Speed Host Input AC Timing Diagram



9.7.11 Device Bus Interface AC Timing

9.7.11.1 Device Bus Interface AC Timing Table

Table 67: Device Bus Interface AC Timing Table

Description	Symbol	Min	Max	Units	Notes
Data/READYn input setup relative to clock rising edge	tSU	7.0	-	ns	-
Data/READYn input hold relative to clock rising edge	tHD	1.0	-	ns	-
Address/Data output delay relative to clock rising edge	tOV	0.8	8.0	ns	1
Address output valid before ALE signal falling edge	tAOAB	10.0	-	ns	1 , 2
Address output valid after ALE signal falling edge	tAOAA	6.0	-	ns	1 , 2

Notes:

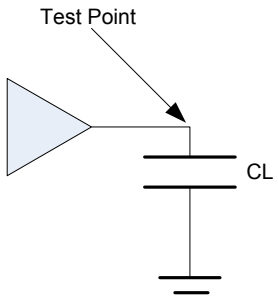
General comment: All timing values are for interfacing synchronous devices.

General comment: All values were measured from VIL(max) to VIH(min), unless otherwise specified.

1. For all signals, the load is CL = 10 pF.
2. The AD bus is normally loaded with high capacitance. Make sure to work according to hardware design guidelines or simulations to meet the latch AC timing requirements.

9.7.11.2 Device Bus Interface Test Circuit

Figure 37: Device Bus Interface Test Circuit



9.7.11.3 Device Bus Interface AC Timing Diagram

Figure 38: Device Bus Interface Output Delay AC Timing Diagram

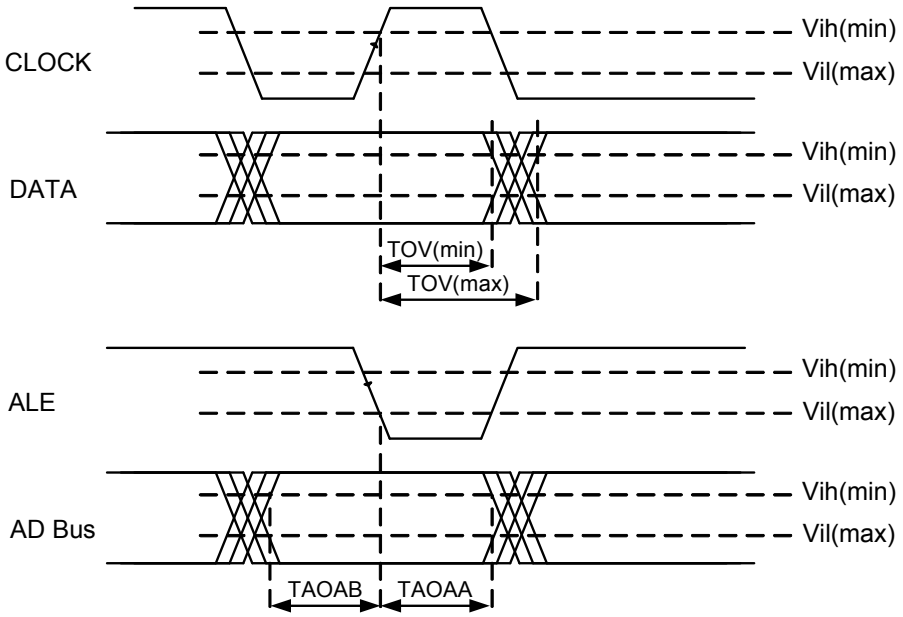
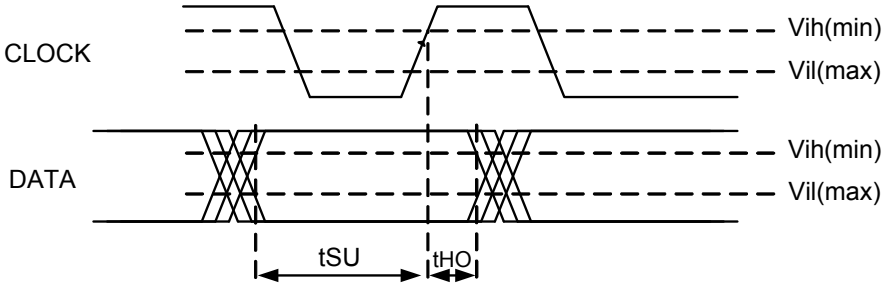


Figure 39: Device Bus Interface Input AC Timing Diagram



9.7.12 Serial Peripheral Interface (SPI) AC Timing

9.7.12.1 SPI (Master Mode) AC Timing Table

Table 68: SPI (Master Mode) AC Timing Table

Description	Symbol	SPI		Units	Notes
		Min	Max		
SCLK clock frequency	fCK	See Note 3		MHz	3
SCLK high time	tCH	0.46	-	tCK	1, 2
SCLK low time	tCL	0.46	-	tCK	1, 2
SCLK slew rate	tSR	0.5	-	V/ns	1
Data out valid relative to SCLK falling edge	tDOV	-2.5	2.5	ns	1
CS active before first SCLK rising edge	tCSB	0.4	-	tCK	1, 4
CS not active after SCLK rising edge	tCSA	0.4	-	tCK	1, 4
Data in setup time relative to SCLK rising edge	tSU	0.2	-	tCK	2
Data in hold time relative to SCLK rising edge	tHD	5.0	-	ns	2

Notes:

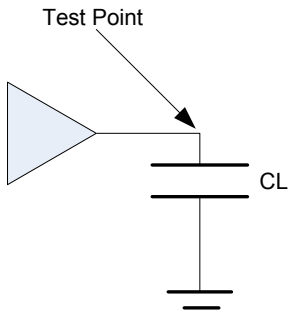
General comment: All values were measured from 0.3*vddio to 0.7*vddio, unless otherwise specified.

General comment: tCK = 1/fCK.

1. For all signals, the load is CL = 10 pF.
2. Defined from vddio/2 to vddio/2.
3. See "Reference Clocks" table for more details.
4. When working with CPOL=1 mode, the CS is relative to first SCLK falling edge.

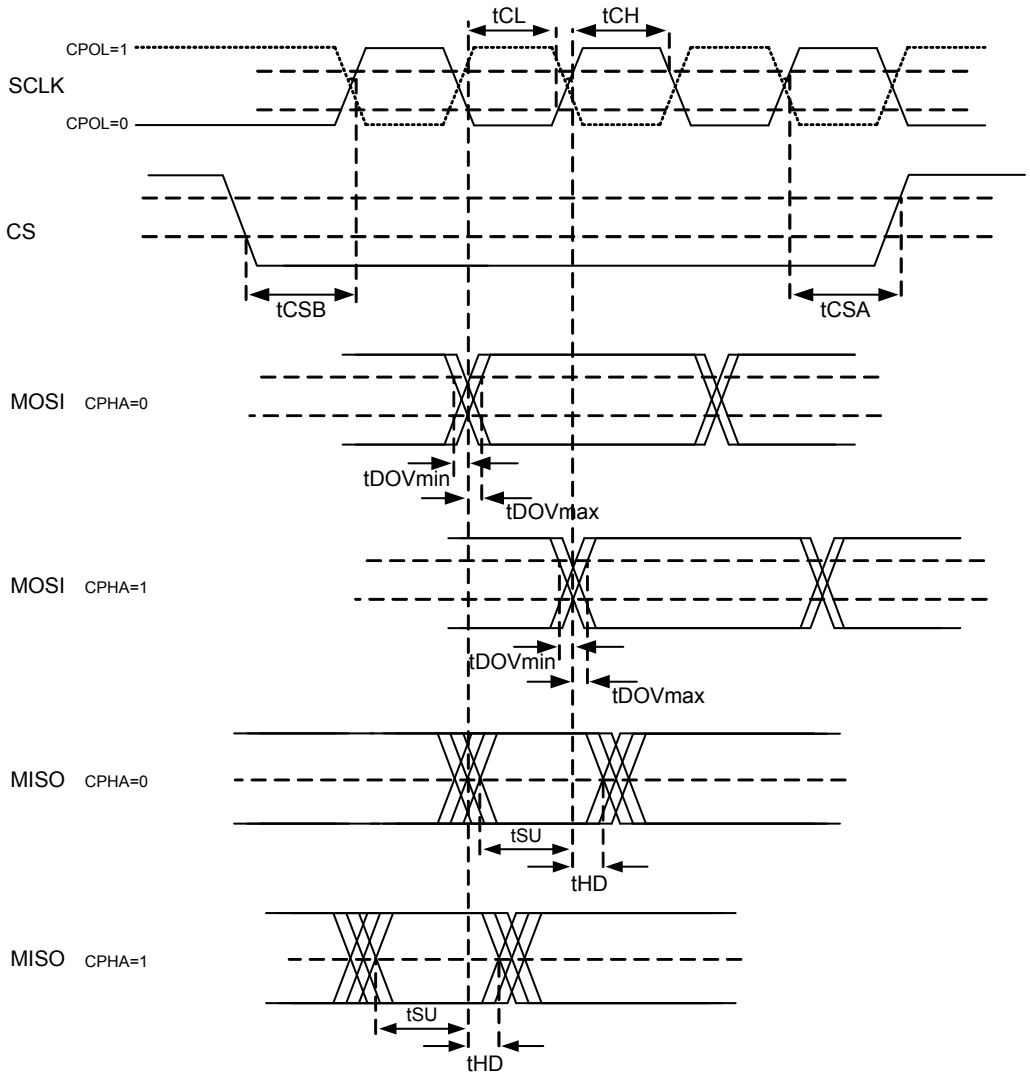
9.7.12.2 SPI (Master Mode) Test Circuit

Figure 40: SPI (Master Mode) Test Circuit



9.7.12.3 SPI (Master Mode) Timing Diagrams

Figure 41: SPI (Master Mode) AC Timing Diagram



9.7.13 Time Division Multiplexing (TDM) Interface AC Timing

9.7.13.1 TDM Interface AC Timing Table

Table 69: TDM Interface AC Timing Table

Description	Symbol	8.192 MHz		Units	Notes
		Min	Max		
PCLK frequency	1/tC	0.256	8.192	MHz	1, 3
PCLK accuracy	tPPM	-50	50	ppm	1
PCLK period jitter	tCJIT	-8	8	ns	1
PCLK duty cycle	tDTY	0.4	0.6	tC	1
PCLK rise/fall time	tR/tF	-	3	ns	1, 2, 8
FSYNC period	tFS	125		us	1
FSYNC period jitter	tFJIT	-120	120	ns	1
DTX and FSYNC valid after PCLK rising edge	tD	0	20	ns	1, 4, 6
DRX and FSYNC setup time relative to PCLK falling edge	tSU	10	-	ns	5, 7
DRX and FSYNC hold time relative to PCLK falling edge	tHD	10	-	ns	5, 7

Notes:

General comment: All values were measured from vddio/2 to vddio/2, unless otherwise specified.

1. For all signals, the load is CL = 20 pF.
2. Rise and Fall times are referenced to the 20% and 80% levels of the waveform.
3. PCLK can be configured to several frequency options. Refer to the Functional Specifications or to the Clock settings for details.
4. This parameter is relevant for the FSYNC signal in Master mode only.
5. This parameter is relevant for the FSYNC signal in Slave mode only.
6. In negative-mode, the DTX signal is relative to PCLK falling edge.
7. In negative-mode, the DRX signal is relative to PCLK rising edge.
8. This parameter is relevant when the PCLK pin is output.

9.7.13.2 High Level Data Link Control (HDLC) AC Timing Table

Table 70: HDLC Interface AC Timing Table

Description	Symbol	Min	Max	Units	Notes
PCLK frequency	1/tC	See note #3		MHz	1, 3
PCLK accuracy	tPPM	-50	50	ppm	1
PCLK duty cycle	tDTY	0.4	0.6	tC	1
PCLK rise/fall time	tR/tF	-	3	ns	1, 2
DTX and FSYNC valid after PCLK rising edge	tD	1	10	ns	1, 4
DRX and FSYNC setup time relative to PCLK falling edge	tSU	4	-	ns	5
DRX and FSYNC hold time relative to PCLK falling edge	tHD	1	-	ns	5

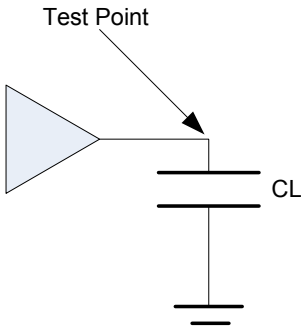
Notes:

General comment: All values were measured from vddio/2 to vddio/2, unless otherwise specified.

1. For all signals, the load is CL = 10 pF.
2. Rise and Fall times are referenced to the 20% and 80% levels of the waveform.
3. PCLK can be configured to several frequency options. Refer to the Functional Specifications or to the Clock settings for details.
4. In negative-mode, the DTX signal is relative to PCLK falling edge.
5. In negative-mode, the DRX signal is relative to PCLK rising edge.

9.7.13.3 TDM Interface Test Circuit

Figure 42: TDM Interface Test Circuit



9.7.13.4 TDM Interface Timing Diagrams

Figure 43: TDM Interface Output Delay AC Timing Diagram

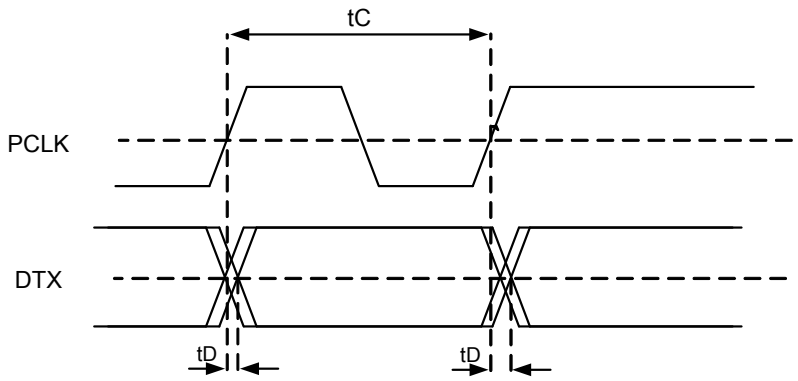
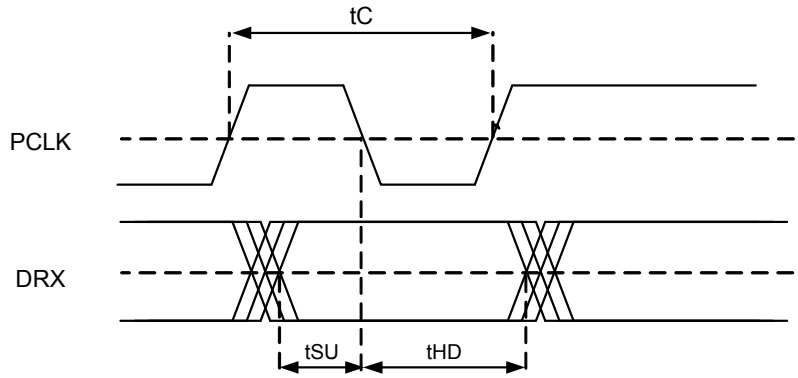


Figure 44: TDM Interface Input Delay AC Timing Diagram



9.7.14 Inter-integrated Circuit Interface (I^2C) AC Timing

9.7.14.1 I^2C AC Timing Table

Table 71: I^2C Master AC Timing Table

Description	Symbol	Min	Max	Units	Notes
SCK clock frequency	fCK	See note 1		kHz	1
SCK minimum low level width	tLOW	0.47	-	tCK	2
SCK minimum high level width	tHIGH	0.40	-	tCK	2
SDA input setup time relative to SCK rising edge	tSU	250.0	-	ns	-
SDA input hold time relative to SCK falling edge	tHD	0.0	-	ns	4
SDA and SCK rise time	tr	-	1000.0	ns	2, 3
SDA and SCK fall time	tf	-	300.0	ns	2, 3
SDA output delay relative to SCK falling edge	tOV	0.0	0.4	tCK	2

Notes:

General comment: All values referred to VIH(min) and VIL(max) levels, unless otherwise specified.

General comment: tCK = 1/fCK.

1. See "Reference Clocks" table for more details.
2. For all signals, the load is CL = 100 pF, and RL value can be 500 ohm to 8 kilohm.
3. Rise time measured from VIL(max) to VIH(min), fall time measured from VIH(min) to VIL(max).
4. For this parameter, the load is CL = 10 pF.

Table 72: I^2C Slave AC Timing Table

Description	Symbol	100 kHz (Max)		Units	Notes
		Min	Max		
SCK minimum low level width	tLOW	4.7	-	us	1
SCK minimum high level width	tHIGH	4.0	-	us	1
SDA input setup time relative to SCK rising edge	tSU	250.0	-	ns	-
SDA input hold time relative to SCK falling edge	tHD	0.0	-	ns	-
SDA and SCK rise time	tr	-	1000.0	ns	1, 2
SDA and SCK fall time	tf	-	300.0	ns	1, 2
SDA output delay relative to SCK falling edge	tOV	0.0	4.0	us	1

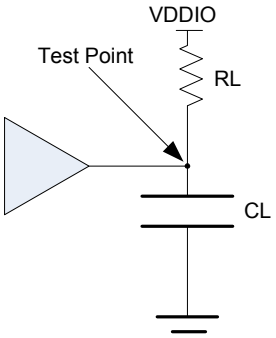
Notes:

General comment: All values referred to VIH(min) and VIL(max) levels, unless otherwise specified.

1. For all signals, the load is CL = 100 pF, and RL value can be 500 ohm to 8 kilohm.
2. Rise time measured from VIL(max) to VIH(min), fall time measured from VIH(min) to VIL(max).

9.7.14.2 I²C Test Circuit

Figure 45: I²C Test Circuit



9.7.14.3 I²C AC Timing Diagrams

Figure 46: I²C Output Delay AC Timing Diagram

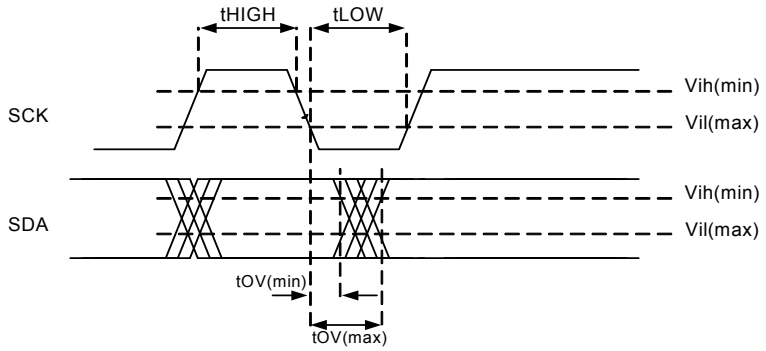
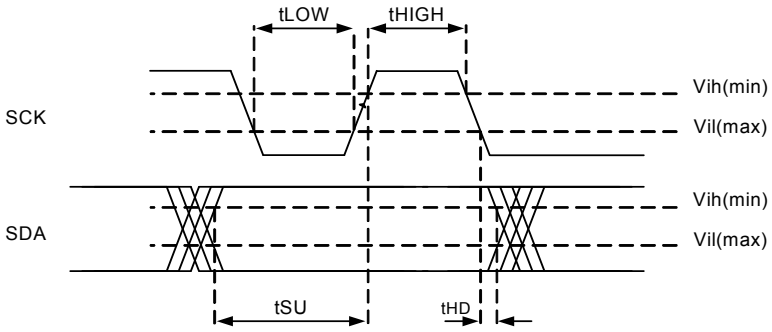


Figure 47: I²C Input AC Timing Diagram



9.7.15 JTAG Interface AC Timing

9.7.15.1 JTAG Interface AC Timing Table

Table 73: JTAG Interface AC Timing Table

Description	Symbol	Min	Max	Units	Notes
JTClk frequency	fCK	See Note 3		MHz	-
JTClk minimum pulse w idth	Tpw	0.45	0.55	tCK	-
JTClk rise/fall slew rate	Sr/Sf	0.5	-	V/ns	2
JTRSTn active time	Trst	1.0	-	ms	-
TMS, TDI input setup relative to JTClk rising edge	Tsetup	0.2*tCK	-	ns	-
TMS, TDI input hold relative to JTClk rising edge	Thold	0.4*tCK	-	ns	-
JTClk falling edge to TDO output delay	Tprop	1.0	0.25*tCK	ns	1

Notes:

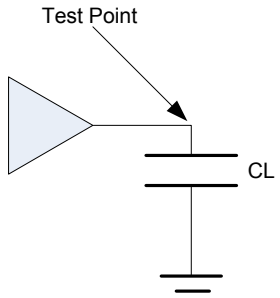
General comment: All values w ere measured from vddio/2 to vddio/2, unless otherw ise specified.

General comment: tCK = 1/fCK.

1. For TDO signal, the load is CL = 10 pF.
2. Defined from VIL to VIH for rise time, and from VIH to VIL for fall time.
3. See "Reference Clocks" table for more details.

9.7.15.2 JTAG Interface Test Circuit

Figure 48: JTAG Interface Test Circuit



9.7.15.3 JTAG Interface AC Timing Diagrams

Figure 49: JTAG Interface Output Delay AC Timing Diagram

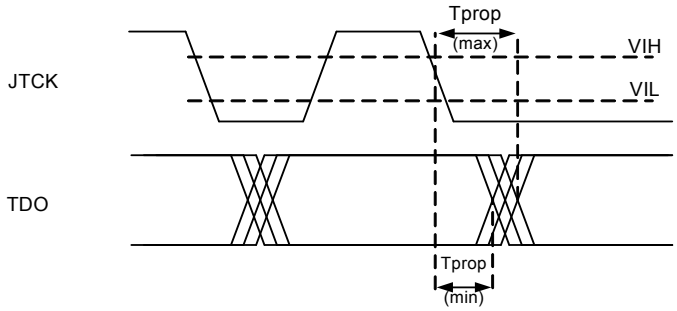
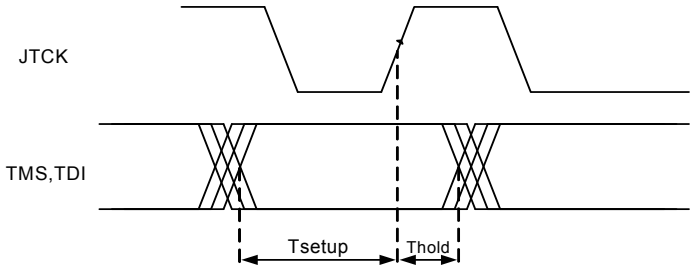


Figure 50: JTAG Interface Input AC Timing Diagram



9.7.16 NAND Flash Interface AC Timing

9.7.16.1 NAND Flash AC Timing Table

Table 74: NAND Flash AC Timing Table

Description	Symbol	Min	Max	Units	Notes
WEn cycle time	tWC	35	-	ns	1
WEn minimum low pulse width	tWP	15	-	ns	1, 2
WEn minimum high pulse width	tWH	17	-	ns	1, 2
ALE to WEn skew factor	tASK	-3.5	3.5	ns	2, 3
CLE to WEn skew factor	tCLSK	-3.5	3.5	ns	2, 3
CEn to WEn skew factor	tCSK	-3.5	3.5	ns	2, 3
Data output bus to WEn skew factor	tDSK	-3.5	3.5	ns	2, 3
REn cycle time	tRC	35	-	ns	1
REn minimum low pulse width	tRP	15	-	ns	1, 2
REn minimum high pulse width	tREH	17	-	ns	1, 2
Data input to REn rising edge skew factor	tISK	-3.5	3.5	ns	2, 3

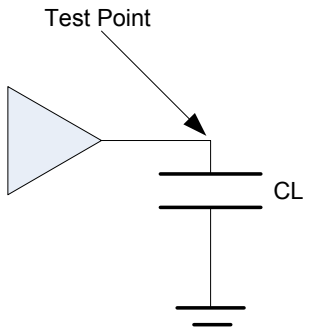
Notes:

General comment: All values were measured from VIL(max) to VIH(min), unless otherwise specified.

1. See functional specifications for configuration options.
2. For all signals, the load is CL = 10 pF.
3. Skew factor should be taken into consideration as a timing degradation in addition to register settings. Refer to functional specifications for more information about timing adjustment possibilities.

9.7.16.2 NAND Flash Test Circuit

Figure 51: NAND Flash Test Circuit



9.7.16.3 NAND Flash AC Timing Diagrams

Figure 52: NAND Flash Input AC Timing Diagram

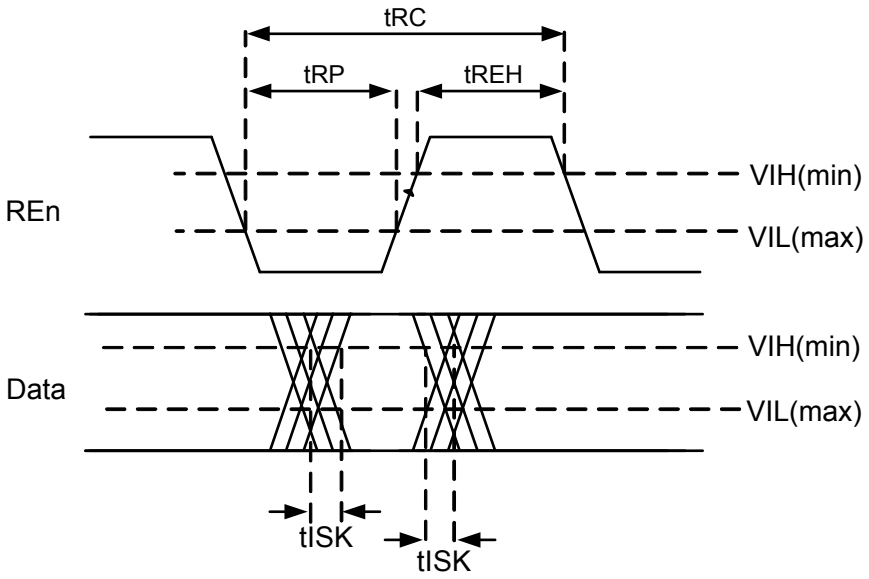
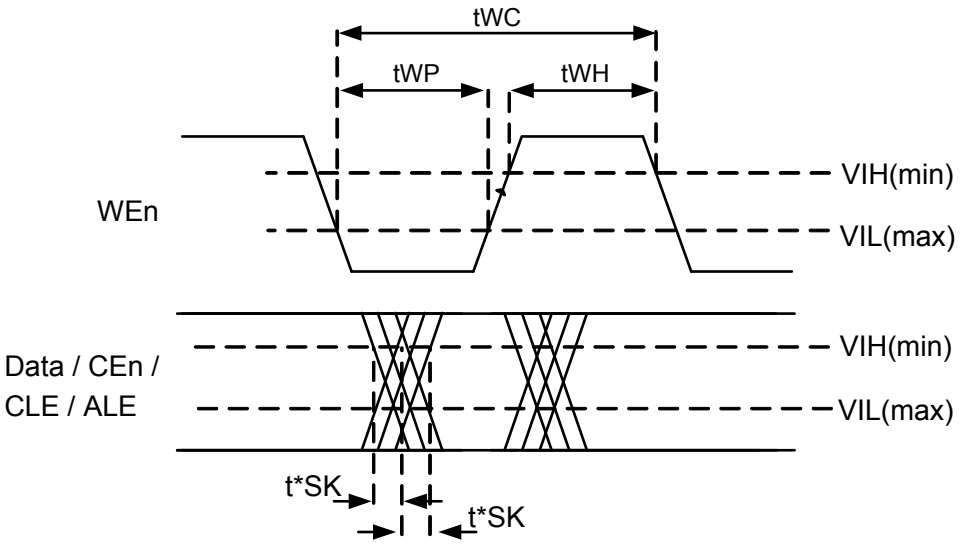


Figure 53: NAND Flash Output AC Timing Diagram



9.8 Differential Interface Electrical Characteristics

This section provides the reference clock, AC, and DC characteristics for the following differential interfaces:

- PCI Express (PCIe) Interface Electrical Characteristics
- SATA Interface Electrical Characteristics
- USB Electrical Characteristics
- Serial Gigabit Media Independent Interface (SGMII) Interface Electrical Characteristics
- Double Rated-SGMII (DR-SGMII) Electrical Characteristics
- Quad Serial Gigabit Media Independent Interface (QSGMII) Electrical Characteristics
- Serial Embedded Trace Macrocell (sETM) Interface Electrical Characteristics

Note

The Tx and Rx timing parameters are defined with the relevant reference clock specifications as specified in the Hardware Specifications.

9.8.1 Differential Interface Reference Clock Characteristics

9.8.1.1 PCI Express Interface Differential Reference Clock Characteristics

Note

Table 75 is relevant for PEX0_CLK_P/N and PEX1_CLK_P/N.

Table 75: PCI Express Interface Differential Reference Clock Characteristics

Description	Symbol	Min	Max	Units	Notes
Clock frequency	fCK	100		MHz	-
Clock duty cycle	DCrefclk	0.4	0.6	tCK	-
Differential rising/falling slew rate	SRrefclk	0.6	4	V/ns	3
Differential high voltage	VIHrefclk	150	-	mV	-
Differential low voltage	VILrefclk	-	-150	mV	-
Absolute crossing point voltage	Vcross	250	550	mV	1
Variation of Vcross over all rising clock edges	Vcrs_dlta	-	140	mV	1
Rise-Fall matching	dTRrefclk	-	20	%	1
Average differential clock period accuracy	Tperavg	-300	2800	ppm	-
Absolute differential clock period	Tperabs	9.8	10.2	ns	2
Differential clock cycle-to-cycle jitter	Tccjit	-	150	ps	-
Clock high frequency RMS jitter	Thfrms	-	3.1	ps RMS	4
Clock low frequency RMS jitter	Tlfrms	-	3	ps RMS	4

Notes:

General Comment: The reference clock timings are based on 100 ohm test circuit.

General Comment: Refer to the PCI Express Card Electromechanical Specification, Revision 2.0, April 2007, section 2.1.3 for more information.

1. Defined on a single-ended signal.
2. Including jitter and spread spectrum.

Table 76: PCI Express Interface Spread Spectrum Requirements

Symbol	Min	Max	Units	Notes
Fmod	0.0	33.0	kHz	1
Fspread	-0.5	0.0	%	1

Notes:

1. Defined on linear sweep or “Hershey’s Kiss” (US Patent 5,631,920) modulations.

Note

The PCIe Spread-Spectrum Clocking (SSC) only works with a PCIe reference clock input.

9.8.2 PCI Express (PCIe) Interface Electrical Characteristics

9.8.2.1 PCI Express Interface Driver and Receiver Characteristics

Table 77: PCI Express 1.1 Interface Driver and Receiver Characteristics

Description	Symbol	Min	Max	Units	Notes
Baud rate	BR	2.5		Gbps	-
Unit interval	UI	400		ps	-
Baud rate tolerance	Bppm	-300	300	ppm	2
Driver parameters					
Differential peak to peak output voltage	VTXpp	0.8	1.2	V	-
Minimum TX eye width	TTXeye	0.75	-	UI	-
Differential return loss	TRLdiff	10	-	dB	1
Common mode return loss	TRLcm	6	-	dB	1
DC differential TX impedance	ZTXdiff	80	120	Ohm	-
Receiver parameters					
Differential input peak to peak voltage	VRXpp	0.175	1.2	V	-
Minimum receiver eye width	TRXeye	0.4	-	UI	-
Differential return loss	RRLdiff	10	-	dB	1
Common mode return loss	RRLcm	6	-	dB	1
DC differential RX impedance	ZRXdiff	80	120	Ohm	-
DC single-ended input impedance	ZRXcm	40	60	Ohm	-

Notes:

General Comment: For more information, refer to the PCI Express Base Specification, Revision 1.1, March, 2005.

1. Defined from 50 MHz to 1.25 GHz.
   Return loss includes contributions from on-chip circuitry, chip packaging,
   and off-chip optimized components related to the driver/receiver breakout.
2. Does not account for SSC dictated variations.

Table 78: PCI Express 2 Interface Driver and Receiver Characteristics

Description	Symbol	Min	Max	Units	Notes
Baud rate	BR	5		Gbps	-
Unit interval	UI	200		ps	-
Baud rate tolerance	Bppm	-300	300	ppm	1
Driver parameters					
Differential peak to peak output voltage	VTXpp	0.8	1.2	V	-
Minimum TX eye width	TTXeye	0.75	-	UI	-
Differential return loss [50 MHz to 1.25 GHz]	TRLdiff	10	-	dB	-
Differential return loss [1.25 GHz to 2.5 GHz]	TRLdiff	8	-	dB	-
Common mode return loss	TRLcm	6	-	dB	2
DC differential TX impedance	ZTXdiff	-	120	Ohm	-
Receiver parameters					
Differential input peak to peak voltage	VRXpp	0.1	1.2	V	-
Minimum receiver eye width	TRXeye	0.4	-	UI	-
Differential return loss [50 MHz to 1.25 GHz]	RRLdiff	10	-	dB	-
Differential return loss [1.25 GHz to 2.5 GHz]	RRLdiff	8	-	dB	-
Common mode return loss	RRLcm	6	-	dB	2
DC single-ended input impedance	ZRXcm	40	60	Ohm	-

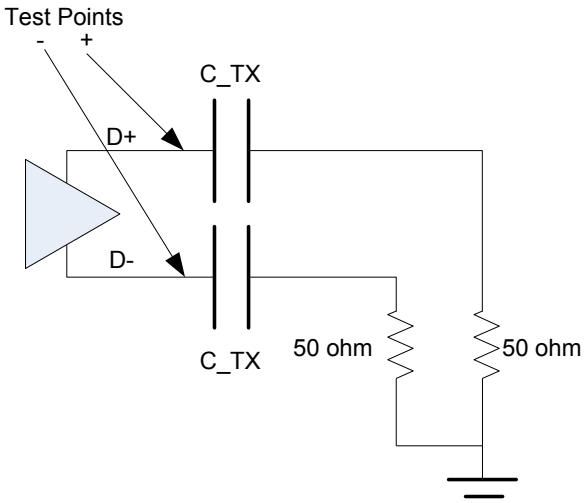
Notes:

General Comment: For more information, refer to the PCI Express Base Specification, Revision 2.0, December 2007.

1. Does not account for SSC dictated variations.
2. Defined from 50 MHz to 2.5 GHz.
   Return loss includes contributions from on-chip circuitry, chip packaging,
   and off-chip optimized components related to the driver/receiver breakout.

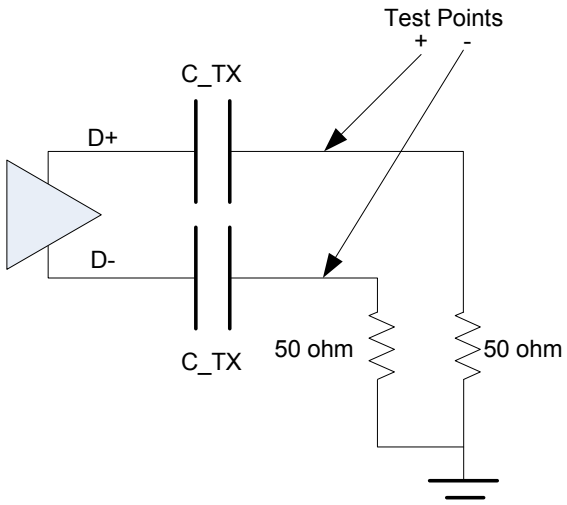
9.8.2.2 PCI Express Interface Test Circuit

Figure 54: PCI Express Interface 1.1 Test Circuit



When measuring Transmitter output parameters, C_TX is an optional portion of the Test/Measurement load. When used, the value of C_TX must be in the range of 75 nF to 200 nF. C_TX must not be used when the Test/Measurement load is placed in the Receiver package reference plane.

Figure 55: PCI Express Interface 2.0 Test Circuit



When measuring Transmitter output parameters, C_TX is an optional portion of the Test/Measurement load. When used, the value of C_TX must be in the range of 75 nF to 200 nF. C_TX must not be used when the Test/Measurement load is placed in the Receiver package reference plane.

9.8.3 SATA Interface Electrical Characteristics

Note The tables below specify the SATA electrical characteristics at the SATA connector. Refer to the device design guide for connectivity and layout guidelines of the SATA interface.

9.8.3.1 SATA I Interface Gen1 Mode Driver and Receiver Characteristics

Table 79: SATA I Interface Gen1i Mode Driver and Receiver Characteristics

Description	Symbol	Min	Max	Units	Notes
Baud Rate	BR	1.5		Gbps	-
Baud rate tolerance	Bppm	-350.0	350.0	ppm	-
Spread spectrum modulation frequency	Fssc	30.0	33.0	kHz	-
Spread spectrum modulation Deviation	SSCtol	-5000.0	0.0	ppm	-
Unit Interval	UI	666.67		ps	-
Driver Parameters					
Differential impedance	Zdifftx	85.0	115.0	Ohm	-
Single ended impedance	Zsetx	40.0	-	Ohm	-
Differential return loss (75 MHz-150 MHz)	RLOD	14.0	-	dB	-
Differential return loss (150 MHz-300 MHz)	RLOD	8.0	-	dB	-
Differential return loss (300 MHz-1.2 GHz)	RLOD	6.0	-	dB	-
Differential return loss (1.2 GHz-2.4 GHz)	RLOD	3.0	-	dB	-
Differential return loss (2.4 GHz-3.0 GHz)	RLOD	1.0	-	dB	-
Output differential voltage	Vdifftx	400.0	600.0	mV	2
Total jitter at connector data-data, 5UI	TJ5	-	0.355	UI	1, 3
Deterministic jitter at connector data-data, 5UI	DJ5	-	0.175	UI	3
Total jitter at connector data-data, 250UI	TJ250	-	0.470	UI	1, 3
Deterministic jitter at connector data-data, 250UI	DJ250	-	0.220	UI	3
Receiver Parameters					
Differential impedance	Zdiffrx	85.0	115.0	Ohm	-
Single ended impedance	Zsetx	40.0	-	Ohm	-
Differential return loss (75 MHz-150 MHz)	RLID	18.0	-	dB	-
Differential return loss (150 MHz-300 MHz)	RLID	14.0	-	dB	-
Differential return loss (300 MHz-600 MHz)	RLID	10.0	-	dB	-
Differential return loss (600 MHz-1.2 GHz)	RLID	8.0	-	dB	-
Differential return loss (1.2 GHz-2.4 GHz)	RLID	3.0	-	dB	-
Differential return loss (2.4 GHz-3.0 GHz)	RLID	1.0	-	dB	-
Input differential voltage	Vdiffrx	325.0	600.0	mV	-
Total jitter at connector data-data, 5UI	TJ5	-	0.430	UI	1, 3
Deterministic jitter at connector data-data, 5UI	DJ5	-	0.250	UI	3
Total jitter at connector data-data, 250UI	TJ250	-	0.600	UI	1, 3
Deterministic jitter at connector data-data, 250UI	DJ250	-	0.350	UI	3

Notes:

General Comment: For more information, refer to SATA II Revision 2.6 Specification, February, 2007.

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

General Comment: To comply with the values presented in this table, refer to your local Marvell representative for register settings.

1. Total jitter is defined as TJ = (14 * RJσ) + DJ where Rjσ is random jitter.
2. Output Differential Amplitude and Pre-Emphasis are configurabile. See the functional register description for more details.
3. The value is informative only, and it can be achieved by using a proper board layout. Refer to the hardware design guidelines for more information.

9.8.3.2 SATA II Interface Gen2 Mode Driver and Receiver Characteristics

Table 80: SATA II Interface Gen2i Mode Driver and Receiver Characteristics

Description	Symbol	Min	Max	Units	Notes
Baud Rate	BR	3.0		Gbps	-
Baud rate tolerance	Bppm	-350.0	350.0	ppm	-
Spread spectrum modulation frequency	Fssc	30.0	33.0	kHz	-
Spread spectrum modulation deviation	SSCtol	-5000.0	0.0	ppm	-
Unit Interval	UI	333.33		ps	-
Driver Parameters					
Output differential voltage	Vdifftx	400.0	700.0	mV	1 , 2
Differential return loss (150 MHz-300 MHz)	RLOD	14.0	-	dB	-
Differential return loss (300 MHz-600 MHz)	RLOD	8.0	-	dB	-
Differential return loss (600 MHz-2.4 GHz)	RLOD	6.0	-	dB	-
Differential return loss (2.4 GHz-3.0 GHz)	RLOD	3.0	-	dB	-
Differential return loss (3.0 GHz-5.0 GHz)	RLOD	1.0	-	dB	-
Total jitter at connector clock-data	TJ	-	0.37	UI	4, 5
Deterministic jitter at connector clock-data	DJ	-	0.19	UI	5
Receiver Parameters					
Input differential voltage	Vdiffrx	275.0	750.0	mV	3
Differential return loss (150 MHz-300 MHz)	RLID	18.0	-	dB	-
Differential return loss (300 MHz-600 MHz)	RLID	14.0	-	dB	-
Differential return loss (600 MHz-1.2 GHz)	RLID	10.0	-	dB	-
Differential return loss (1.2 GHz-2.4 GHz)	RLID	8.0	-	dB	-
Differential return loss (2.4 GHz-3.0 GHz)	RLID	3.0	-	dB	-
Differential return loss (3.0 GHz-5.0 GHz)	RLID	1.0	-	dB	-
Total jitter at connector clock-data	TJ	-	0.60	UI	4, 5
Deterministic jitter at connector clock-data	DJ	-	0.42	UI	5

Notes:

General Comment: For more information, refer to SATA II Revision 2.6 Specification, February, 2007.

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

General Comment: To comply with the values presented in this table, refer to your local Marvell representative for register settings.

1. 0.45-0.55 UI is the range where the signal meets the minimum level.
2. Output Differential Amplitude and Pre-Emphasis are configurabile. See the functional register description for more details.
3. 0.5 UI is the point where the signal meets the minimum level.
4. The jitter is defined using a recovered clock with characteristics that meet the desired Jitter Transfer Function (JTF). The JTF is the ratio between the jitter defined using the recovered clock and the jitter defined using an ideal clock. It should have a high pass function with the following characteristics:
   - The -3 dB corner frequency of the JTF shall be 2.1 MHz +/- 1 MHz.
   - The magnitude peaking of the JTF shall be 3.5 dB maximum.
   - The attenuation at 30 kHz +/- 1% shall be 72 dB +/- 3 dB.
5. The value is informative only, and it can be achieved by using a proper board layout. Refer to the hardware design guidelines for more information.

Table 81: SATA II Interface Gen2m Mode Driver and Receiver Characteristics

Description	Symbol	Min	Max	Units	Notes
Baud Rate	BR	3.0		Gbps	-
Baud rate tolerance	Bppm	-350.0	350.0	ppm	-
Spread spectrum modulation frequency	Fssc	30.0	33.0	kHz	-
Spread spectrum modulation deviation	SSCtol	-5000.0	0.0	ppm	-
Unit Interval	UI	333.33		ps	-
Driver Parameters					
Output differential voltage	Vdifftx	400.0	700.0	mV	1 , 2
Differential return loss (150 MHz-300 MHz)	RLOD	14.0	-	dB	-
Differential return loss (300 MHz-600 MHz)	RLOD	8.0	-	dB	-
Differential return loss (600 MHz-2.4 GHz)	RLOD	6.0	-	dB	-
Differential return loss (2.4 GHz-3.0 GHz)	RLOD	3.0	-	dB	-
Total jitter at connector clock-data	TJ	-	0.37	UI	4, 5
Deterministic jitter at connector clock-data	DJ	-	0.19	UI	5
Receiver Parameters					
Input differential voltage	Vdiffrx	240.0	750.0	mV	3
Differential return loss (150 MHz-300 MHz)	RLID	18.0	-	dB	-
Differential return loss (300 MHz-600 MHz)	RLID	14.0	-	dB	-
Differential return loss (600 MHz-1.2 GHz)	RLID	10.0	-	dB	-
Differential return loss (1.2 GHz-2.4 GHz)	RLID	8.0	-	dB	-
Differential return loss (2.4 GHz-3.0 GHz)	RLID	3.0	-	dB	-
Total jitter at connector clock-data	TJ	-	0.60	UI	4, 5
Deterministic jitter at connector clock-data	DJ	-	0.42	UI	5

Notes:

General Comment: For more information, refer to SATA II Revision 2.6 Specification, February, 2007.

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

General Comment: To comply with the values presented in this table, refer to your local Marvell representative for register settings.

1. 0.45-0.55 UI is the range where the signal meets the minimum level.
2. Output Differential Amplitude and Pre-Emphasis are configurabile. See the functional register description for more details.
3. 0.5 UI is the point where the signal meets the minimum level.
4. The jitter is defined using a recovered clock with characteristics that meet the desired Jitter Transfer Function (JTF). The JTF is the ratio between the jitter defined using the recovered clock and the jitter defined using an ideal clock. It should have a high pass function with the following characteristics:
   - The -3 dB corner frequency of the JTF shall be 2.1 MHz +/- 1 MHz.
   - The magnitude peaking of the JTF shall be 3.5 dB maximum.
   - The attenuation at 30 kHz +/- 1% shall be 72 dB +/- 3 dB.
5. The value is informative only, and it can be achieved by using a proper board layout. Refer to the hardware design guidelines for more information.

9.8.4 USB Electrical Characteristics

9.8.4.1 USB Driver and Receiver Characteristics

Table 82: USB Low Speed Driver and Receiver Characteristics

Description	Symbol	Low Speed		Units	Notes
		Min	Max		
Baud Rate	BR	1.5		Mbps	-
Baud rate tolerance	Bppm	-15000.0	15000.0	ppm	-
Driver Parameters					
Ouput single ended high	VOH	2.8	3.6	V	1
Ouput single ended low	VOL	0.0	0.3	V	2
Output signal crossover voltage	VCRS	1.3	2.0	V	3
Data fall time	TLR	75.0	300.0	ns	3, 4
Data rise time	TLF	75.0	300.0	ns	3, 4
Rise and fall time matching	TLRFM	80.0	125.0	%	-
Source jitter total: to next transition	TUDJ1	-95.0	95.0	ns	5
Source jitter total: for paired transitions	TUDJ2	-150.0	150.0	ns	5
Receiver Parameters					
Input single ended high	VIH	2.0	-	V	-
Input single ended low	VIL	-	0.8	V	-
Differential input sensitivity	VDI	0.2	-	V	-

Notes:

General Comment: For more information, refer to Universal Serial Bus Specification, Revision 2.0, April 2000.

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

General Comment: To comply with the values presented in this table, refer to your local Marvell representative for register settings.

1. Defined with 1.425 kilohm pull-up resistor to 3.6V.
2. Defined with 14.25 kilohm pull-down resistor to ground.
3. See "Data Signal Rise and Fall Time" waveform.
4. Defined from 10% to 90% for rise time and 90% to 10% for fall time.
5. Including frequency tolerance. Timing difference between the differential data signals.

   Defined at crossover point of differential data signals.

Table 83: USB Full Speed Driver and Receiver Characteristics

Description	Symbol	Full Speed		Units	Notes
		Min	Max		
Baud Rate	BR	12.0		Mbps	-
Baud rate tolerance	Bppm	-2500.0	2500.0	ppm	-
Driver Parameters					
Ouput single ended high	VOH	2.8	3.6	V	1
Ouput single ended low	VOL	0.0	0.3	V	2
Output signal crossover voltage	VCRS	1.3	2.0	V	4
Output rise time	TFR	4.0	20.0	ns	3, 4
Output fall time	TFL	4.0	20.0	ns	3, 4
Source jitter total: to next transition	TDJ1	-3.5	3.5	ns	5, 6
Source jitter total: for paired transitions	TDJ2	-4.0	4.0	ns	5, 6
Source jitter for differential transition to SE0 transition	TFDEOP	-2.0	5.0	ns	6
Receiver Parameters					
Input single ended high	VIH	2.0	-	V	-
Input single ended low	VIL	-	0.8	V	-
Differential input sensitivity	VDI	0.2	-	V	-
Receiver jitter : to next transition	tJR1	-18.5	18.5	ns	6
Receiver jitter: for paired transitions	tJR2	-9.0	9.0	ns	6

Notes:

General Comment: For more information, refer to Universal Serial Bus Specification, Revision 2.0, April 2000.

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

General Comment: To comply with the values presented in this table, refer to your local Marvell representative for register settings.

1. Defined with 1.425 kilohm pull-up resistor to 3.6V.
2. Defined with 14.25 kilohm pull-down resistor to ground.
3. Defined from 10% to 90% for rise time and 90% to 10% for fall time.
4. See "Data Signal Rise and Fall Time" waveform.
5. Including frequency tolerance. Timing difference between the differential data signals.
6. Defined at crossover point of differential data signals.

Table 84: USB High Speed Driver and Receiver Characteristics

Description	Symbol	High Speed		Units	Notes
		Min	Max		
Baud Rate	BR	480.0		Mbps	-
Baud rate tolerance	Bppm	-500.0	500.0	ppm	-
Driver Parameters					
Data signaling high	VHSOH	360.0	440.0	mV	-
Data signaling low	VHSOL	-10.0	10.0	mV	-
Data rise time	THSR	500.0	-	ps	1
Data fall time	THSF	500.0	-	ps	1
Data source jitter		See note 2			2
Receiver Parameters					
Differential input signaling levels		See note 3			3
Data signaling common mode voltage range	VHSCM	-50.0	500.0	mV	-
Receiver jitter tolerance		See note 3			3

Notes:

General Comment: For more information, refer to Universal Serial Bus Specification, Revision 2.0, April 2000.

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

General Comment: To comply with the values presented in this table, refer to your local Marvell representative for register settings.

1. Defined from 10% to 90% for rise time and 90% to 10% for fall time.
2. Source jitter specified by the "TX eye diagram pattern template" figure.
3. Receiver jitter specified by the "RX eye diagram pattern template" figure.

9.8.4.2 USB Interface Driver Waveforms

Figure 56: Low/Full Speed Data Signal Rise and Fall Time

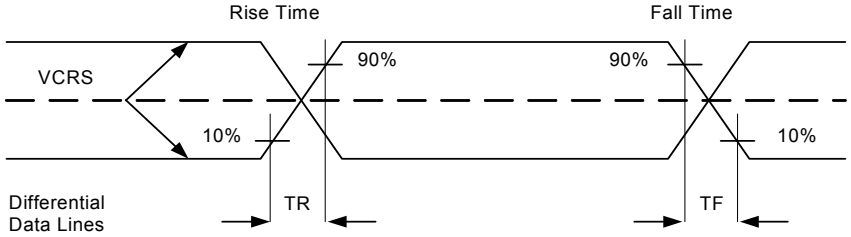


Figure 57: High Speed TX Eye Diagram Pattern Template

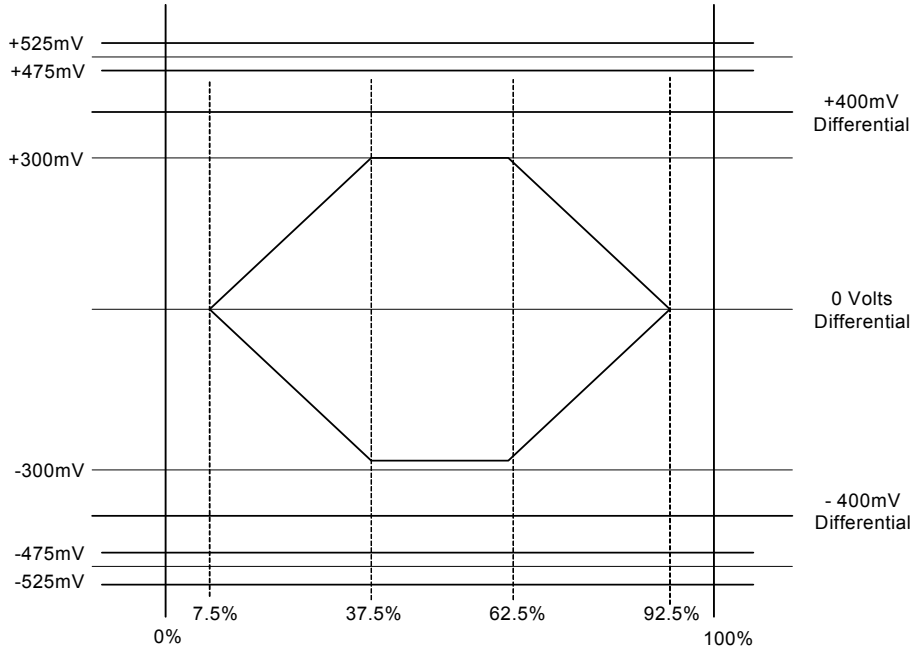
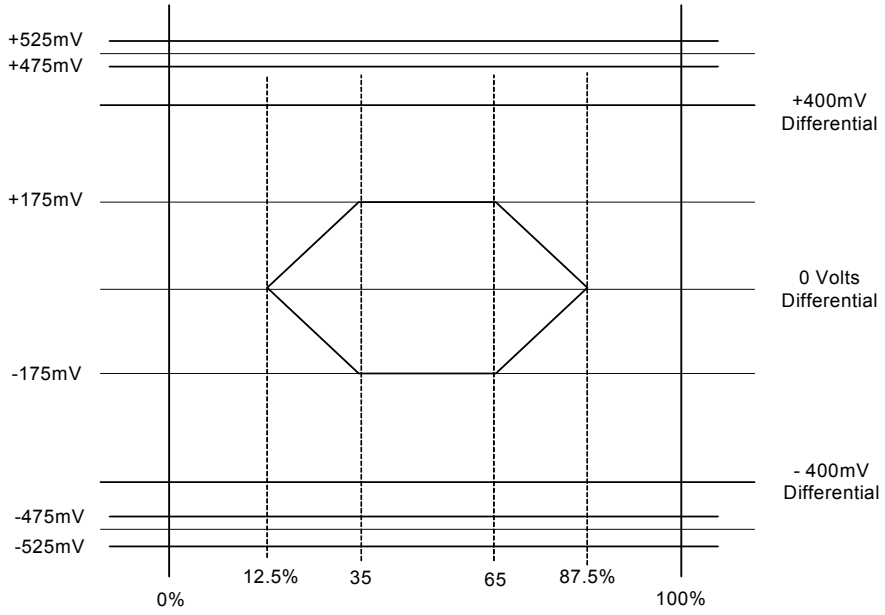


Figure 58: High Speed RX Eye Diagram Pattern Template



9.8.5 Serial Gigabit Media Independent Interface (SGMII) Interface Electrical Characteristics

9.8.5.1 SGMII Driver and Receiver Characteristics

Table 85: SGMII Interface Driver and Receiver Characteristics (1000BASE-X)

Description	Symbol	Min	Max	Units	Notes
Baud rate	BR	1.25		Gbps	-
Baud rate tolerance	Bppm	-100	100	ppm	1
Unit interval	UI	800		ps	-
Driver parameters for 1000BASE-X Backplane Mode					
Output differential minimum eye opening	Vodppe	850	-	mV	-
Output differential maximum peak-to-peak	Vodpp	-	1350	mV	-
Absolute output limits	Vos	-0.4	1.6	V	-
Output differential skew	Tosk	-	20	ps	2
Return loss differential output	RLOD	10	-	dB	3, 9
Output jitter - deterministic, peak-to-peak	Jttx	-	0.1	UI	4
Output jitter - total, peak-to-peak	Jttxpp	-	0.24	UI	6
Receiver parameters for 1000BASE-X Backplane Mode					
Input differential sensitivity	Vidppe	180	-	mV	8
Input differential voltage	Vidpp	-	2000	mV	8
Input differential skew	Tisk	-	180	ps	5
Return loss differential input	RLID	10	-	dB	3, 9
Return loss common mode input	RLIC	6	-	dB	7, 9
Input jitter - deterministic, peak-to-peak	Jtrx	-	0.462	UI	4
Input jitter - total, peak-to-peak	Jtrxpp	-	0.749	UI	6

Notes:

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

1. Defines the allowable reference clock difference from nominal.
2. This is a single ended parameter and is defined at the 50% point on the signal swing.
3. Defined from 50 MHz to 625 MHz.
   For 650 MHz - 1.25 GHz: -10dB+10log(Freq/625) (Freq defined in MHz).
4. Jitter specifications include all but 10^-12 of the jitter population.
5. This value assumes total eye jitter budget is still maintained.
6. Total jitter is composed of both deterministic and random components.
   The allowed random jitter equals the allowed total jitter minus the actual deterministic at that point.
7. Defined from 50 MHz to 625 MHz.
   For 650 MHz - 1.25 GHz: -6dB+10log(Freq/625) (Freq defined in MHz).
8. Vidppe refers to the internal eye opening while Vidpp refers to the peak-to-peak.
9. Return loss includes contributions from on-chip circuitry, chip packaging,
   and off-chip optimized components related to the driver/receiver breakout.

9.8.5.2 SGMII Interface Driver Waveforms

Figure 59: Tri-Speed Interface Driver Output Voltage Limits And Definitions

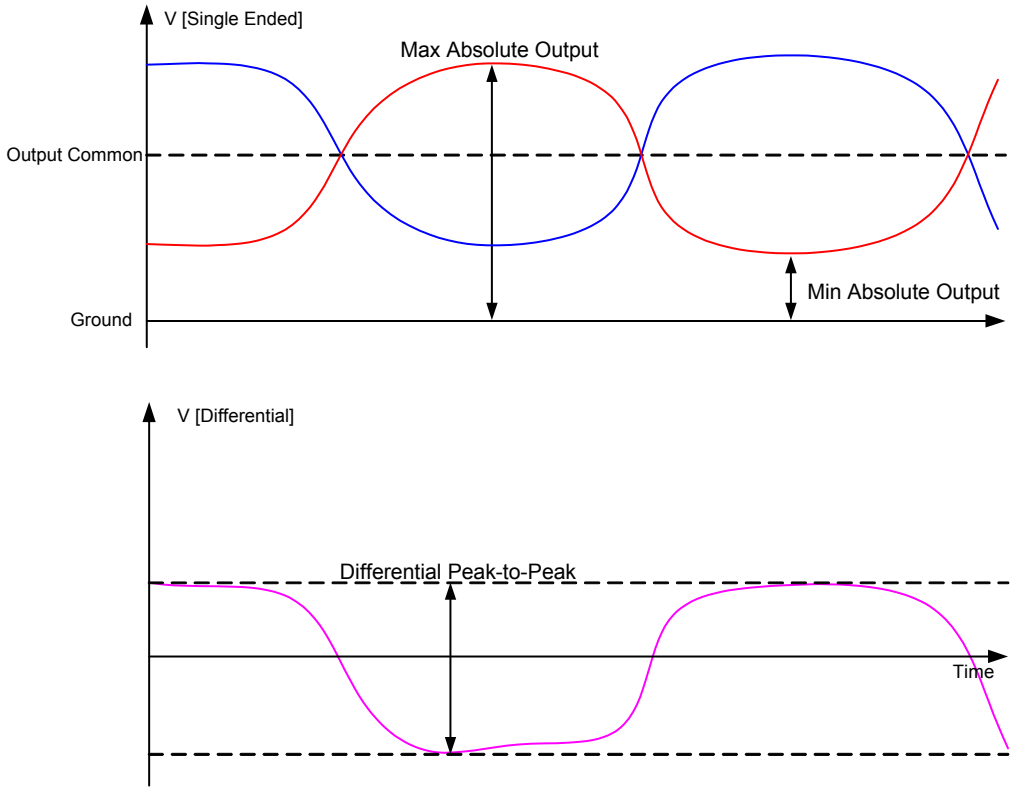
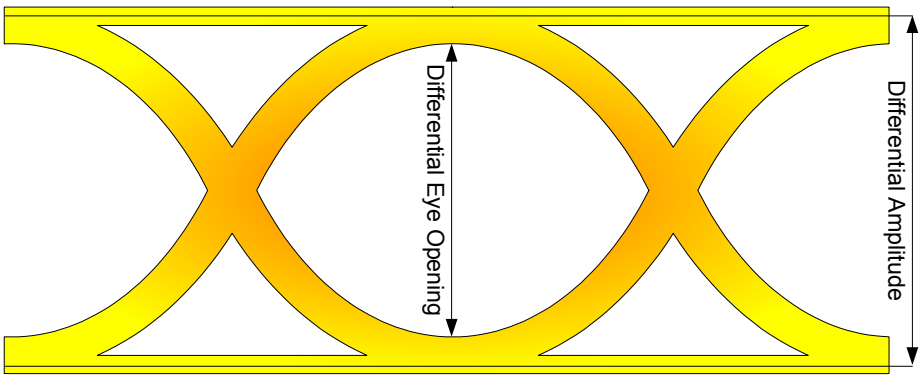


Figure 60: Driver Output Differential Amplitude and Eye Opening



9.8.6 Double Rated-SGMII (DR-SGMII) Electrical Characteristics

9.8.6.1 DR-SGMII Short Reach (SR) Driver and Receiver Characteristics

Table 86: DR-SGMII Short Reach (SR) Driver and Receiver Characteristics

Description	Symbol	Min	Max	Units	Notes
Baud Rate	BR	3.125		Gbps	-
Baud rate tolerance	Bppm	-100	100	ppm	1
Unit Interval	UI	320		ps	-
Driver parameters					
Output differential minimum eye opening	Vodppe	800	-	mV	-
Output differential maximum peak-to-peak	Vodpp	-	1600	mV	-
Absolute output limits	Vos	-0.4	2.3	V	-
Output differential skew	Tosk	-	15	ps	2
Output differential transition time	Tr/Tf	-	130	ps	3
Return loss differential output	RLOD	10	-	dB	4
Output jitter - Deterministic, peak-to-peak	Jttx	-	0.17	UI	-
Output jitter - Total, peak-to-peak	Jttxpp	-	0.35	UI	5, 8
Receiver parameters					
Input differential sensitivity	Vidpps	200	-	mV	9
Input differential voltage	Vidpp	-	1600	mV	9
Input differential skew	Tisk	-	75	ps	6
Return loss differential input	RLID	10	-	dB	7
Return loss common mode input	RLIC	6	-	dB	7
Input jitter - Deterministic, peak-to-peak	Jtrx	-	0.47	UI	10
Input jitter - Sinusoidal, low frequency	Jtrlsx	-	8.5	UI	11
Input jitter - Sinusoidal, high frequency	Jtrsx	-	0.1	UI	12
Input jitter - Total, peak-to-peak	Jtrxpp	-	0.65	UI	5, 8

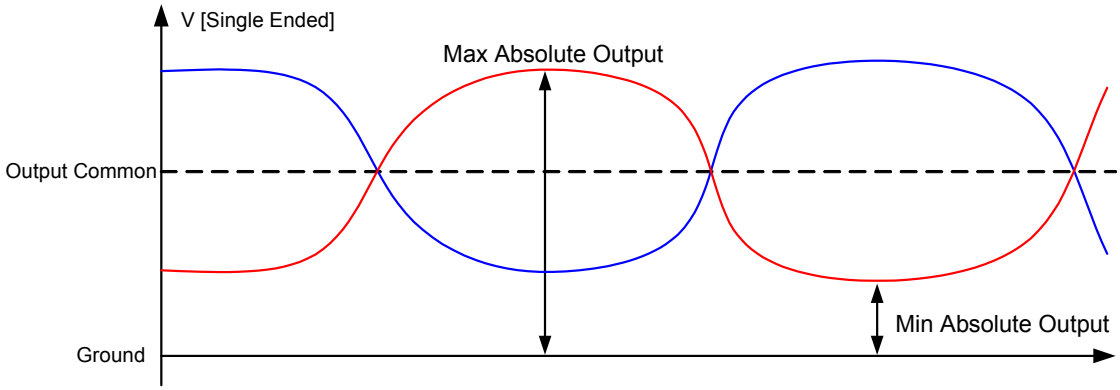
Notes:

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

1. Defines the allowable reference clock difference from nominal.
2. This is a single ended parameter and is defined at the 50% point on the signal swing.
3. Defined from 20% to 80% of the signal's voltage levels.
4. Defined from 312.5 MHz to 625 MHz.
5. Defined with a BER of 10^-12.
6. This value assumes total eye jitter budget is still maintained.
7. Relative to 100 ohm differential and 25 ohm common mode. Defined from 100 MHz to 2.5 GHz.
   Return loss includes contributions from on-chip circuitry, chip packaging,
   and off-chip optimized components related to the driver/receiver breakout.
8. Total jitter is composed of both deterministic and random components.
   The allowed random jitter equals the allowed total jitter minus the actual deterministic at that point.
9. Vidpps refers to the internal eye opening while Vidpp refers to the peak-to-peak.
10. Deterministic jitter includes sinusoidal, high frequency (Jtrsx), component.
11. Defined below 22.1 kHz.
12. Defined from 1.875 MHz to 20 MHz.

9.8.6.2 DR-SGMII Driver Output Waveforms

Figure 61: DR-SGMII Driver Output Voltage Limits and Definitions



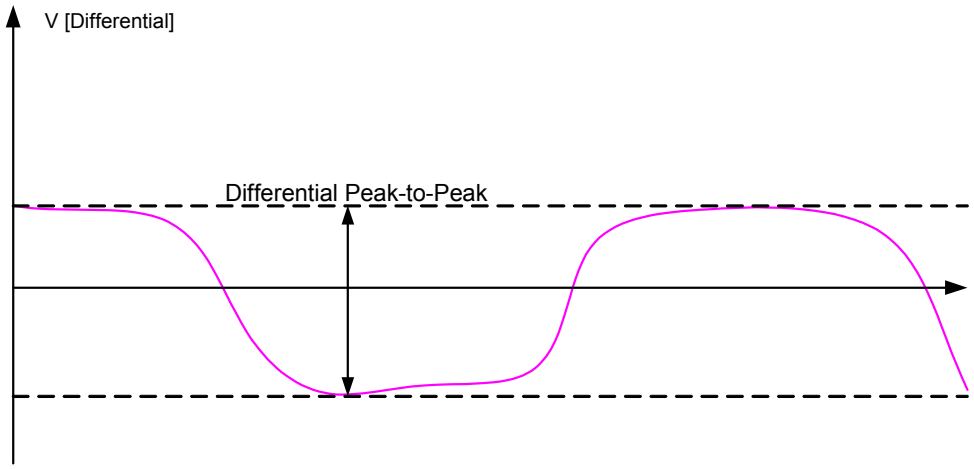


Figure 62: DR-SGMII Driver Output Differential Voltage under Pre-emphasis

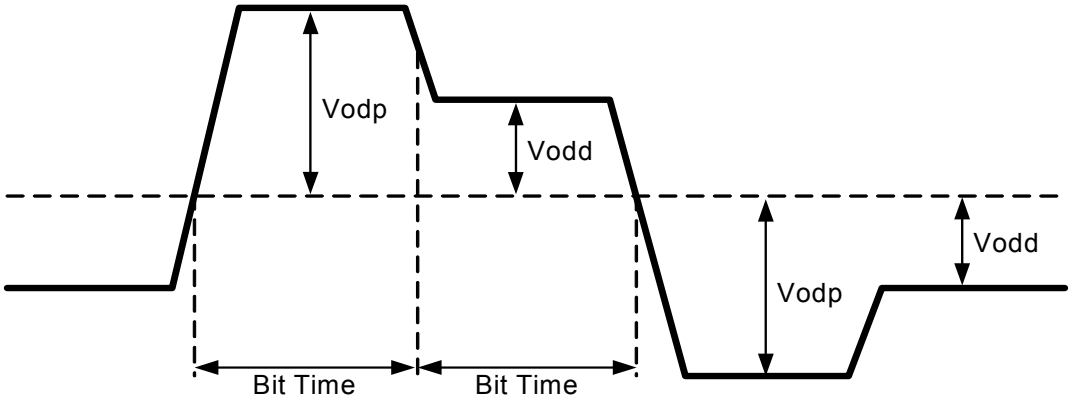
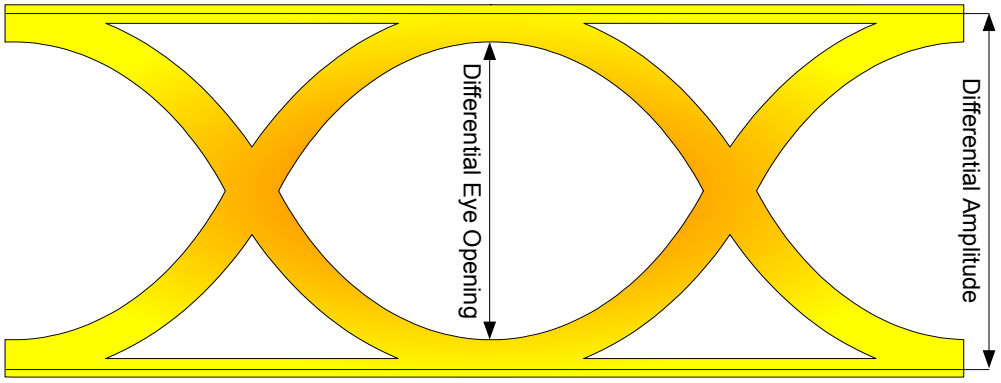


Figure 63: DR-SGMII Driver Output Differential Amplitude and Eye Opening



9.8.7 Quad Serial Gigabit Media Independent Interface (QSGMII) Electrical Characteristics

9.8.7.1 QSGMII Driver and Receiver Characteristics

Table 87: QSGMII Driver and Receiver Characteristics

Description	Symbol	Min	Max	Units	Notes
Baud rate	BR	5.0		Gbps	-
Baud rate tolerance	Bppm	-100.0	100.0	ppm	1
Unit Interval	UI	200.0		ps	-
Driver parameters					
Output differential minimum eye opening	Vodppe	400.0	-	mV	-
Output differential maximum peak-to-peak	Vodpp	-	900.0	mV	-
Output emphasis	Emph	3.0	4.0	dB	-
Output differential resistance	Rdo	80.0	120.0	Ohm	-
Absolute output limits	Vos	-0.1	1.9	V	-
Output differential transition time	Tr/Tf	30.0	-	ps	2
Return loss differential output	RLOD	8.0	-	dB	3, 4
Return loss common mode output	RLOC	6.0	-	dB	3, 4
Output jitter - Deterministic, peak-to-peak	Jttx	-	0.15	UI	17
Output duty cycle distortion	Jdcdtx	-	0.05	UI	-
Output jitter - Total, peak-to-peak	Jttxpp	-	0.30	UI	5, 6, 13
Interconnect parameters (Informative only)					
Interconnect differential insertion loss: 50 MHz	ILOD	-	1.0	dB	7, 8
Interconnect differential insertion loss: 500 MHz	ILOD	-	2.0	dB	7, 8
Interconnect differential insertion loss: 2500 MHz	ILOD	-	6.6	dB	7, 8
Interconnect differential insertion loss: 5000 MHz	ILOD	-	12.3	dB	7, 8
Receiver parameters					
Input differential sensitivity	Vidpps	100.0	-	mV	9
Input differential voltage	Vidpp	-	900.0	mV	9
Input differential resistance	Rdi	80.0	120.0	Ohm	-
Return loss differential input	RLID	8.0	-	dB	3, 4
Return loss common mode input	RLIC	6.0	-	dB	3, 4
Input sinusoidal jitter, low frequency	Js	-	5.0	UI	14
Input sinusodial jitter, high frequency	Jshf	-	0.05	UI	15
Input jitter - Deterministic, peak-to-peak	Jtrx	-	0.45	UI	12
Input uncorrelated bounded high probability jitter	Jtrxuc	-	0.15	UI	10
Input correlated bounded high probability jitter	Jtrxisi	-	0.30	UI	11
Input jitter - Total, peak-to-peak	Jtrxpp	-	0.60	UI	5, 16

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.
General Comment: DC blocker is mandatory since the TX and RX common mode voltage differs.
1. Defines the allowable reference clock difference from nominal.
2. Defined from 20% to 80% of the signal's voltage levels.
3. Defined from 100 MHz to 2.5 GHz.
   For 2.5 GHz -5.0 GHz RLOD> 8dB-16.6log(Freq/2.5) (Freq defined in GHz).
4. Relative to 100 ohm differential and 25 ohm common mode.
   Return loss includes contributions from on-chip circuitry, chip packaging,
   and off-chip optimized components related to the driver/receiver breakout.
5. Defined with a Bit Error Rate (BER) of 10^-15.
6. Total jitter is composed of both deterministic and random components.
   The allowed random jitter equals the allowed total jitter minus the actual deterministic jitter
   and duty cycle distortion at that point.
7. The interconnect insertion loss specification is defined from the TX pins (with zero pre-emphasis) to the RX pins.
   The interconnect value between the frequencies should be extrapolated using
   linear extrapolation on a logarithmic loss scale.
8. The interconnect definition was determined to allow a maximum insertion loss value at
   a frequency equal to half the bit rate.
   The insertion loss value must vary without notch-like behavior up to a maximum frequency
   as defined by the interconnect definition.
9. Vidpps refers to the internal eye opening while Vidpp refers to the peak-to-peak.
10. Jitter distribution where the value of the jitter shows no correlation to any signal level being transmitted.
11. Jitter distribution where the value of the jitter shows a strong correlation to the signal level being transmitted.
    This jitter may be considered as being equalizable due to its correlation to the signal level (ISI).
12. This is the sum of Jtrxuc and Jtrxisi.
13. The clock for output TX jitter is generated using a golden PLL.
    The PLL loop bandwidth is BR/1667 with a 20 dB/dec rolloff.
14. Defined up to f = 30 kHz.
15. Defined between f = BR/1667 to f = 20 MHz.
16. Does not include sinusoidal jitter.
17. Driver jitter does not include correlated bounded jitter created by the driver emphasis.

9.8.7.2 QSGMII Interface Driver Waveforms

Figure 64: QSGMII Driver Output Voltage Limits and Definitions

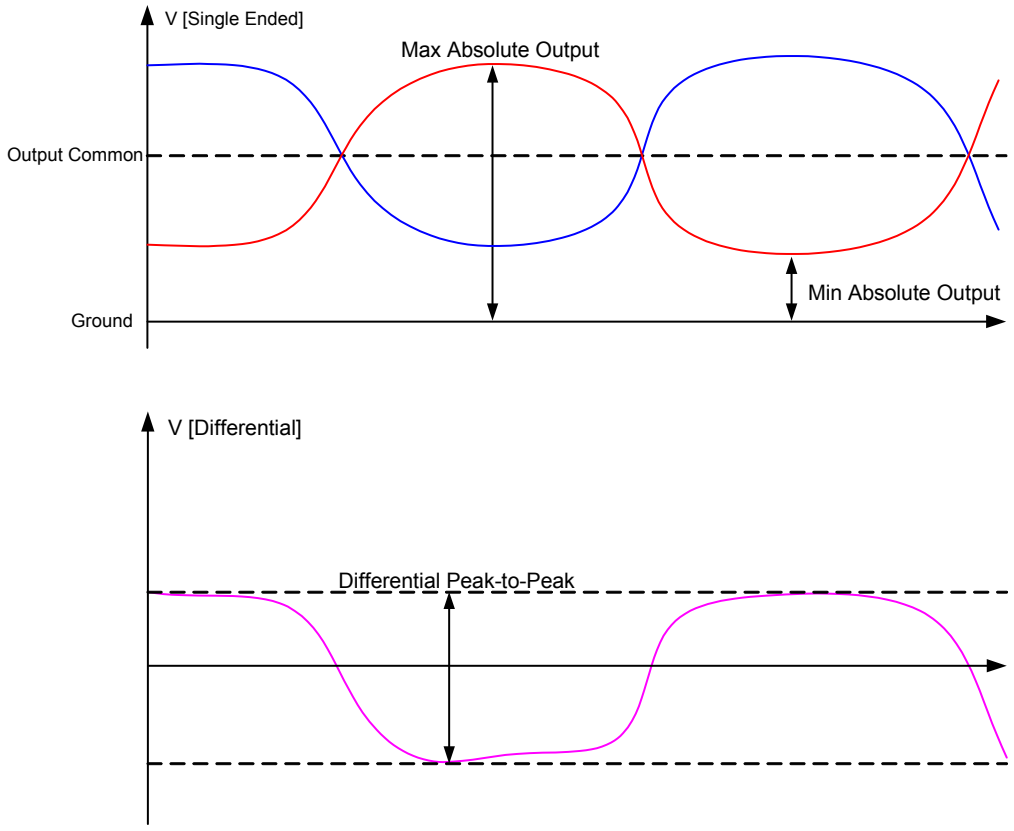


Figure 65: Interconnect Insertion Loss

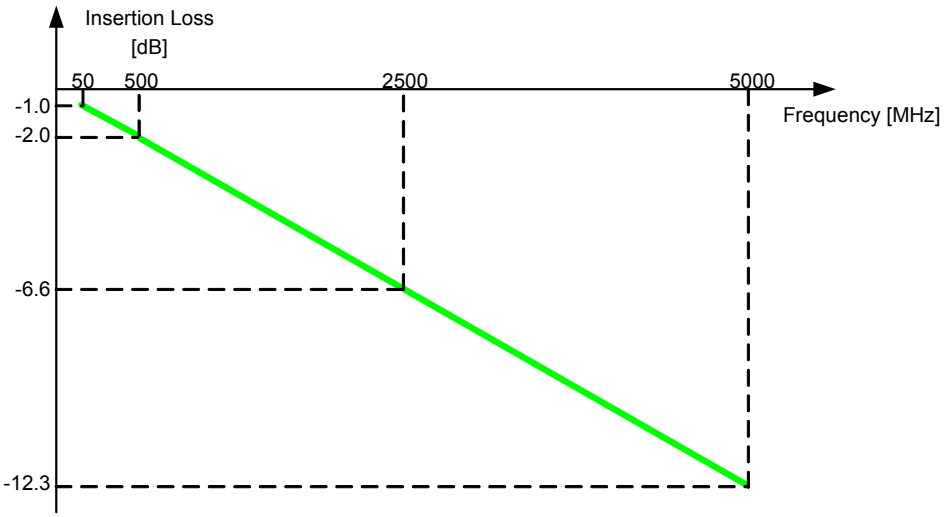
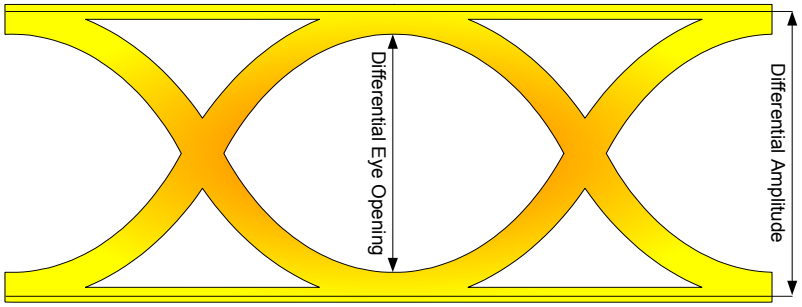


Figure 66: Driver Output Differential Amplitude and Eye Opening



9.8.8 Serial Embedded Trace Macrocell (sETM) Interface Electrical Characteristics

9.8.8.1 sETM Interface Driver and Receiver Characteristics

Table 88: sETM Interface Driver and Receiver Characteristics

Description	Symbol	Min	Max	Units	Notes
Baud Rate	BR	-	6	Gbps	-
Baud rate tolerance	Bppm	-100	100	ppm	1
Unit Interval	UI	166.667	-	ps	-
Driver parameters					
Output differential minimum eye opening	Vodppe	400	-	mV	-
Output differential maximum peak-to-peak	Vodpp	-	1200	mV	-
Absolute output limits	Vos	-0.4	1.9	V	-
Output common mode voltage	Vcm	1.45	1.55	V	-
Output de-emphasis voltage range	Emph	0.0	50	%	5
Output de-emphasis voltage accuracy	Empha	-	10	%	-
Output differential resistance	Rdo	85	115	Ohm	-
Output differential skew	Tosk	-	15	ps	2
Output differential transition time	Tr/Tf	46	64	ps	3
Output lane to lane skew	Tlskew	-	5	UI	-
Output jitter - Total, peak-to-peak	Jttxpp	-	0.26	UI	4

Notes:

General Comment: The load is 100 ohm differential for these parameters, unless otherwise specified.

1. Defines the allowable reference clock difference from nominal.
2. This is a single ended parameter and is defined at the 50% point on the signal swing.
3. Defined from 20% to 80% of the signal's voltage levels.
4. Defined with a BER of 10^-12 and PRBS7 pattern.
5. Precent reduced from the TX differential peak-to-peak voltage.

9.8.8.2 sETM Interface Driver Output Waveforms

Figure 67: Driver Output Voltage Limits and Definitions

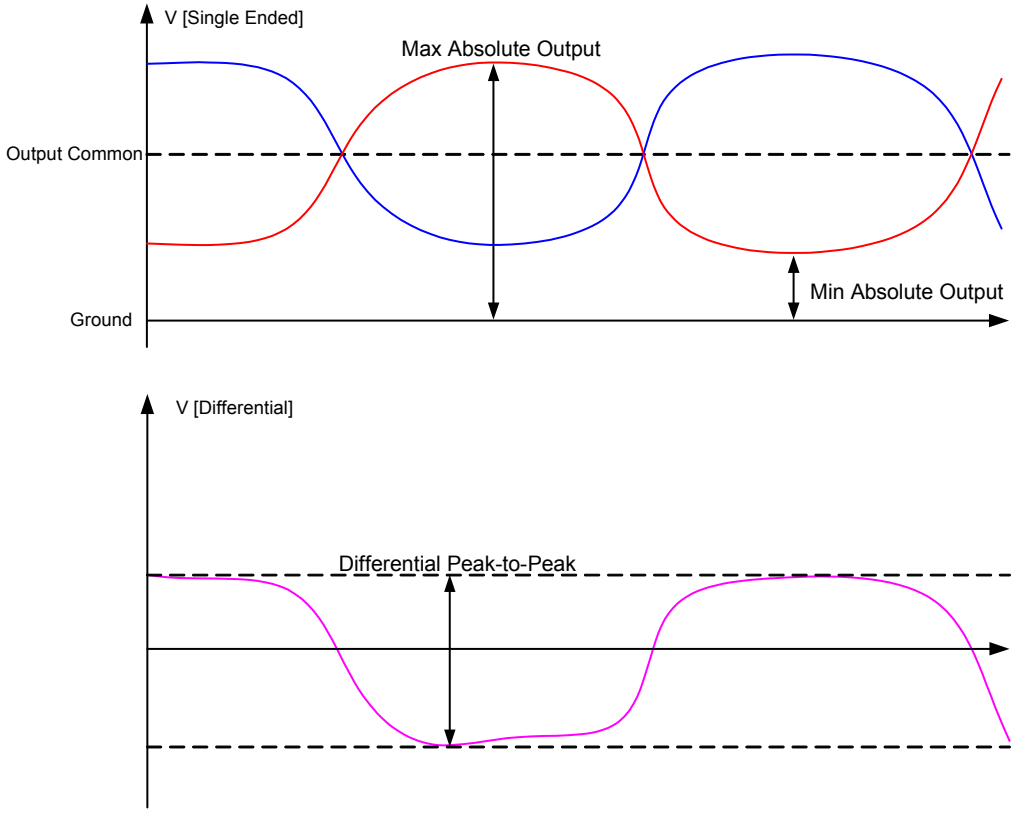
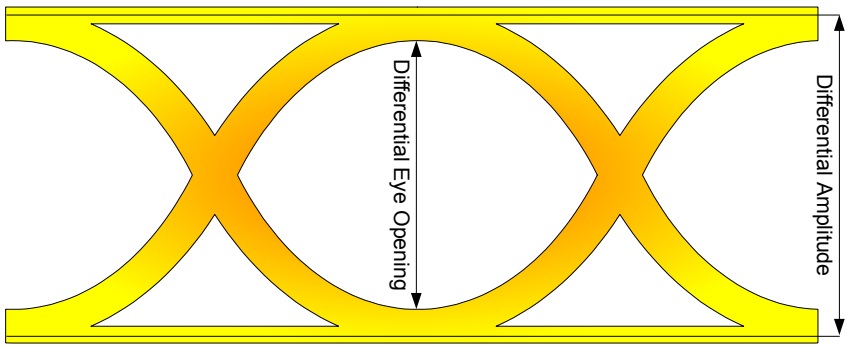


Figure 68: Driver Output Differential Amplitude and Eye Opening



10 Thermal Data

Table 89provides the package thermal data for the MV78230. This data is derived from simulations that were run according to the JEDEC standard.

The documents listed below provide a basic understanding of thermal management of integrated circuits (ICs) and guidelines to ensure optimal operating conditions for Marvell products. Before designing a system, it is recommended to refer to these documents:

- Application Note, *AN-63 Thermal Management for Selected Marvell® Products,* Document Number MV-S300281-00
- White Paper, *ThetaJC, ThetaJA, and Temperature Calculations,* Document Number MV-S700019-00

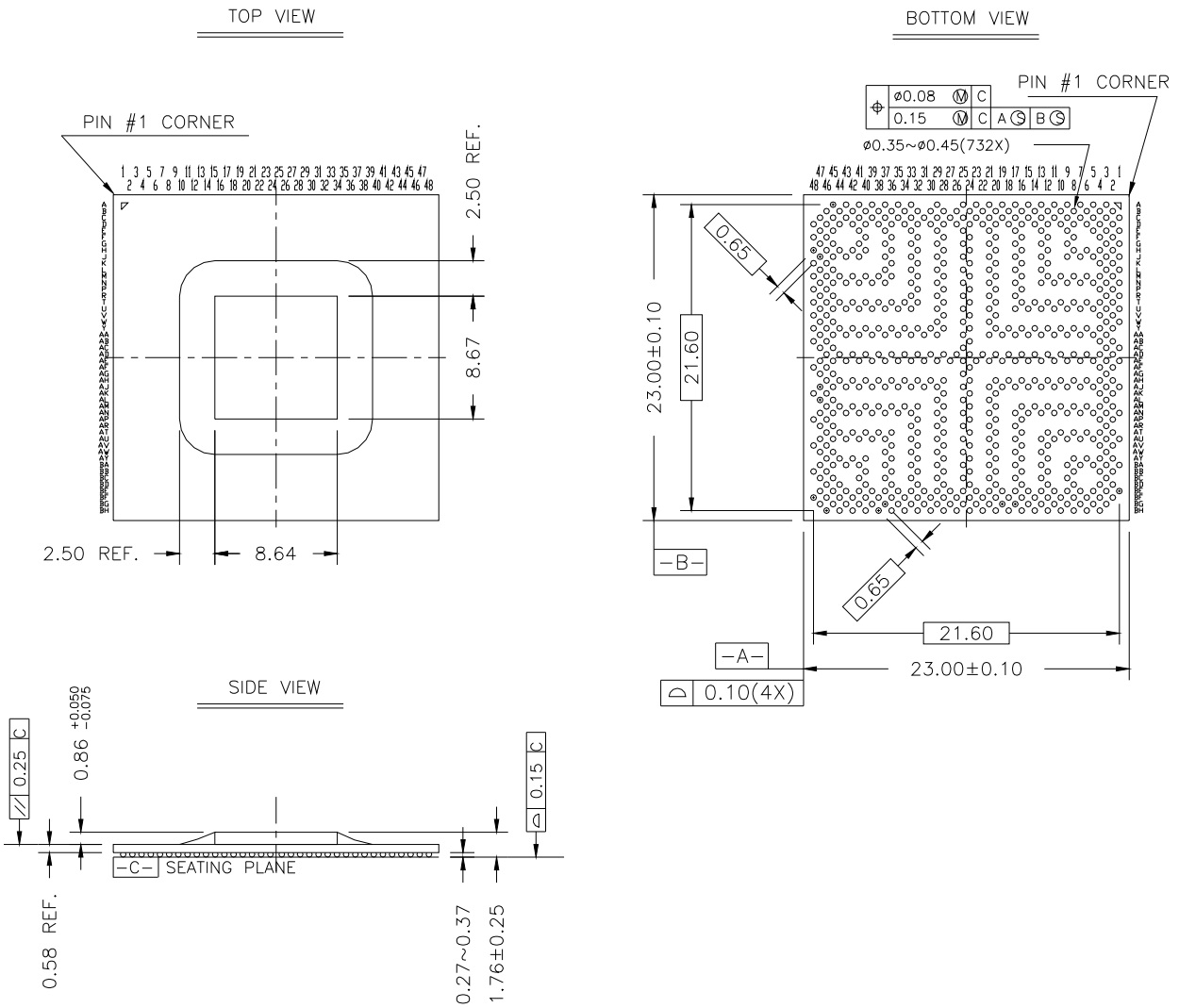
Table 89: Thermal Data for the MV78230 in FCBGA Package

Symbol	Definition	Airflow Value (°C/W)		
		0[m/s]	1[m/s]	2[m/s]
θ_{JA}	Thermal resistance: junction to ambient	14.66	12.54	11.66
Ψ_{JT}	Thermal characterization parameter: junction to top center	0.77	0.67	0.67
Ψ_{JB}	Thermal characterization parameter: junction to board	6.77	6.13	5.92
θ_{JC}	Thermal resistance: junction to case (not air-flow dependent)	0.5		
θ_{JB}	Thermal resistance: junction to board (not air-flow dependent)	6.7		

11 Package Mechanical Dimensions

The ARMADA® XP Highly Integrated Multi-Core ARMv7 Based System-on-Chip Processors use a 732-pin 23 mm x 23 mm FCBGA package with a 0.65 mm pitch.

Figure 69: 732-Pin FCBGA Package and Dimensions



12 Part Order Numbering/Package Marking

12.1 Part Order Numbering

Figure 70 shows the part order numbering scheme for the MV78230. Refer to Marvell Field Application Engineers (FAEs) or representatives for further information when ordering parts.

Figure 70: Sample Part Number

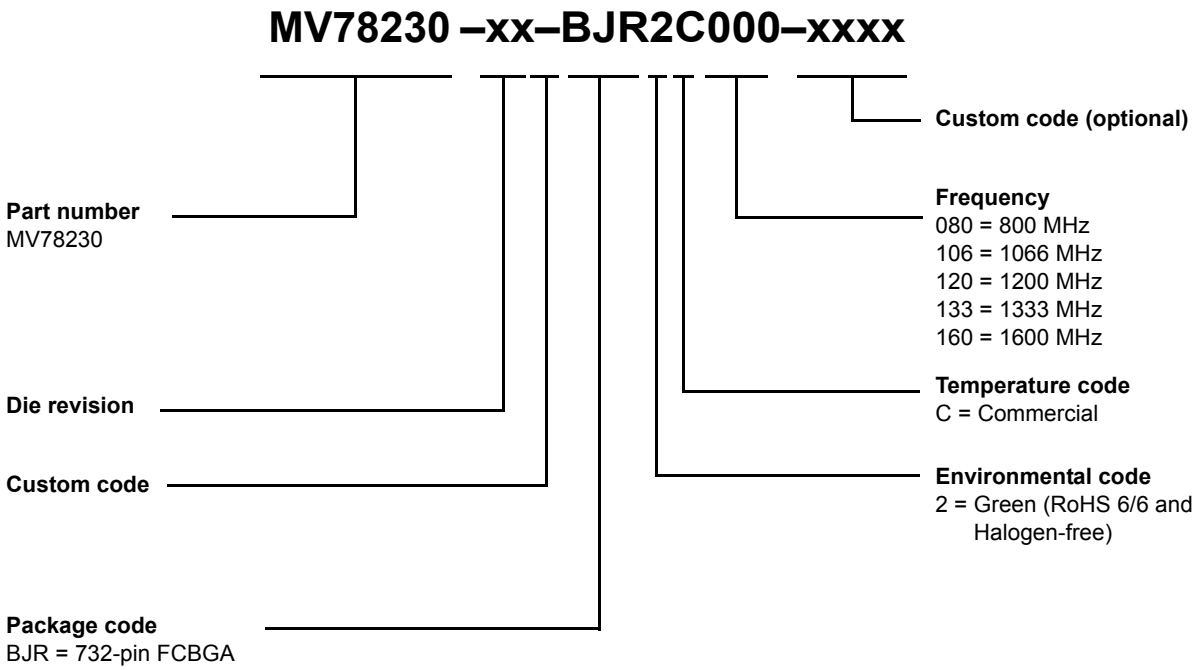


Table 90: MV78230 Part Order Options

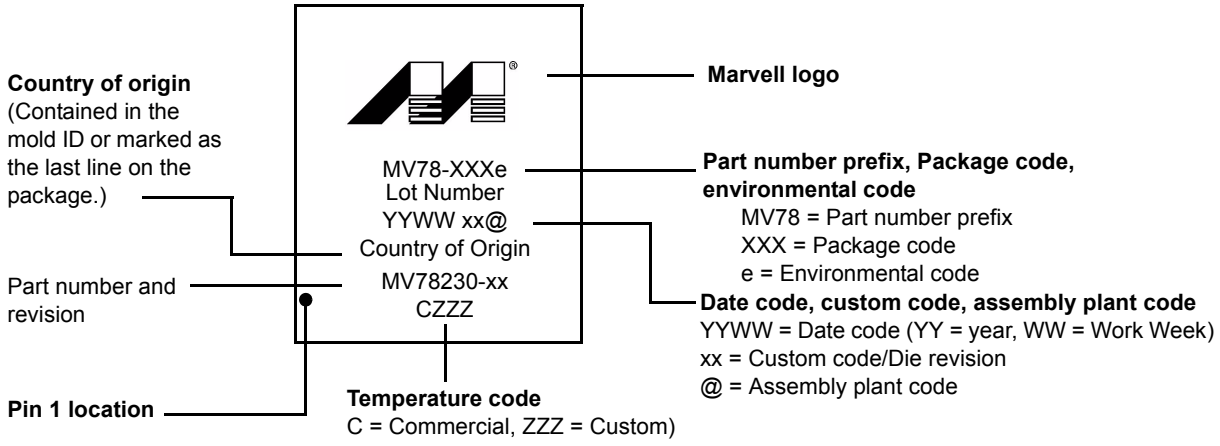
Package Type	Part Order Number
732-pin FCBGA	MV78230-xx-BJR2C080 (Green, RoHS 6/6 and Halogen-free package, 800 MHz)
732-pin FCBGA	MV78230-xx-BJR2C106 (Green, RoHS 6/6 and Halogen-free package, 1066 MHz)
732-pin FCBGA	MV78230-xx-BJR2C120 (Green, RoHS 6/6 and Halogen-free package, 1200 MHz)
732-pin FCBGA	MV78230-xx-BJR2C133 (Green, RoHS 6/6 and Halogen-free package, 1333 MHz)
732-pin FCBGA	MV78230-xx-BJR2C160 (Green, RoHS 6/6 and Halogen-free package, 1600 MHz)

12.2 Package Marking

This section provides the package markings for the MV78230 FCBGA package.

Figure 71 shows a sample flip chip die marking and pin 1 location for the FCBGA package.

Figure 71: Package Marking and Pin 1 Location (Top View)



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