Product Brief

Marvell® Alaska® C 88X5123

Dual 100G/40G, Quad 50G, Octal 25G/10G Ethernet Transceiver

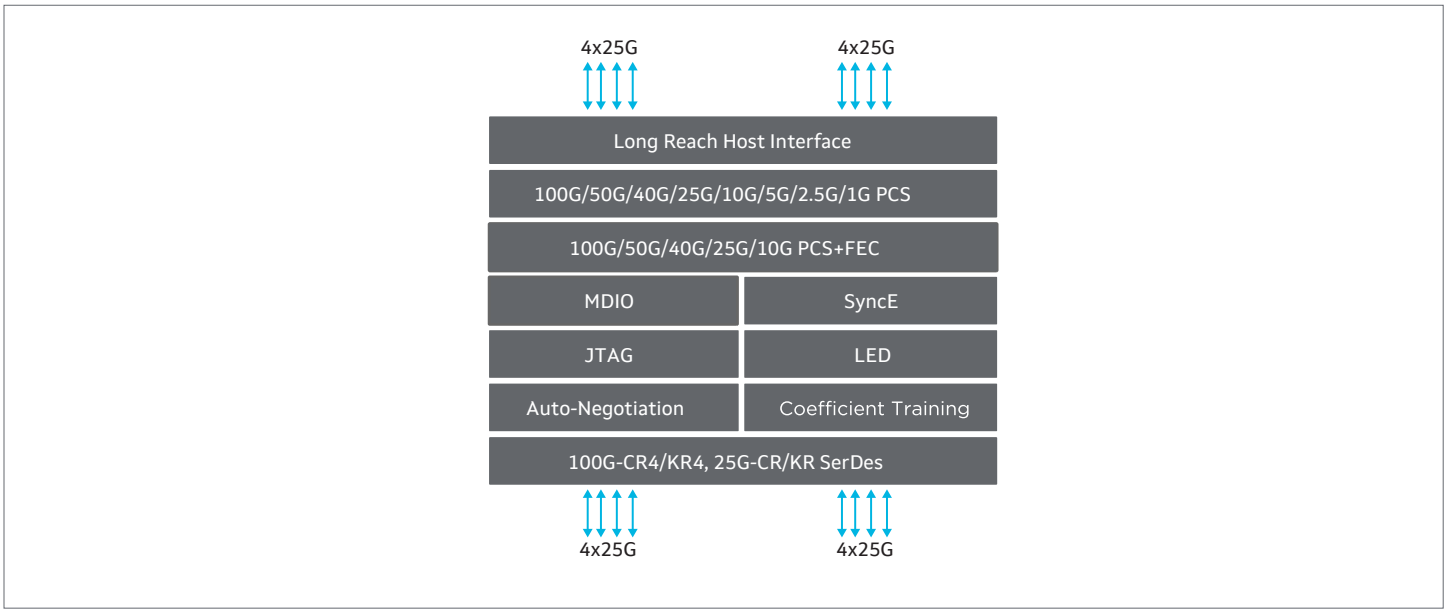
Overview

The Marvell® Alaska® C 88X5123 is a fully integrated device that performs all physical layer functions required to drive 100G, 50G, 40G, 25G, 10G, 5G, 2.5G and 1G Ethernet over a variety of media including; optics, backplanes and passive copper cables. Manufactured with 28 nanometer (nm) lithography, in a small 17mmx17mm 256 pin FCBGA package footprint, the Alaska C 88X5123 enables low-power dissipation, high density 100GbE, 50GbE, and 25GbE line card designs.

The line interface and host interfaces of the 88X5123 are fully compliant to the IEEE 802.3bj and IEEE 802.3by standards 100Gb and 25Gb Ethernet operation. The device supports all the FEC configurations specified by IEEE 802.3bj, and 802.3by standards as well as the 25/50G Ethernet consortium. The device also supports auto-negotiation and coefficient training protocol required by the IEEE 802.3 and 25/50G consortium specifications for twinaxial cable and backplane applications.

The device supports 40GBase-R2 to 40GBase-R4 gearboxing functionality to enable high-density 40GbE applications on switch ASICs with native 25G I/Os. For applications not requiring the FEC functionality, the device also supports a low latency retimer mode where the functionalities associated with the PCS and FEC are bypassed. In this mode, the 88X5123 supports a hole free operation from 1.25Gbps to 28.05Gbps to support a wide variety of standards and rates. The device includes internal PRBS generators and loopbacks to assist with test and debug. In addition, nondestructive eye monitoring is supported on all high speed I/Os.

Block Diagram



Marvell Alaska C 88X1523 Transceiver

Key Features

Features	Benefits
Fully compliant to IEEE 802.3by standard for 25GbE	· Enables 25G Ethernet products and applications fully compliant to IEEE specifications
Fully compliant to IEEE 802.3j standard for 100GbE	· Enables IEEE compliant 100GbE designs
Support for 25G/Consortium mode of operation	· Seamless interoperability with 25G consortium compliant legacy systems
Long Reach Host and Line serdes	· Supports no-FEC operation for low latency applications
Integrated 100G/25G FEC on both host and line interfaces	· Fully symmetric architecture to enable flexible system designs
Integrated IEEE Auto-negotiation and Training protocol	· Seamless interoperability with IEEE compliant devices from other vendors
Low latency retimer mode	· For low latency retiming applications, and non-Ethernet applications such as Fibre Channel
Programmable lane swap capability	· Provides flexibility for board design and layout
Two separate reference clock inputs with independent clock divide ratios	· Enables simultaneous support of multiple standards
Non-destructive eye monitoring capability on all high speed lanes	· Allows for link quality monitoring during mission mode

Target Applications

- 100GbE/50GbE/25GbE data center switches
- High density 40GbE switch designs
- 100G-KR4/25G-KR backplanes

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