88SE917X/88SE918X
One- or Two-Lane PCI Express 2.0 to Two-Port 6 Gbps SATA Host Bus Adapter

Preliminary Datasheet

MV-S106864-00 Rev. A

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Document Classification: Proprietary Information

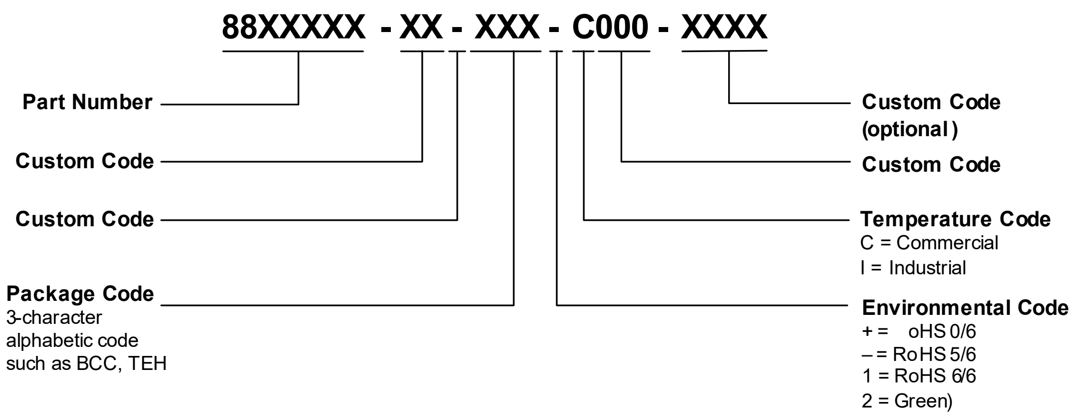
CONFIDENTIAL

ORDERING INFORMATION

Ordering Part Numbers and Package Markings

The following figure shows the ordering part numbering scheme for the 88SE917X/88SE918X part. For complete ordering information, contact your Marvell FAE or sales representative.

Sample Ordering Part Number



The standard ordering part numbers for the respective solutions are indicated in the following table.

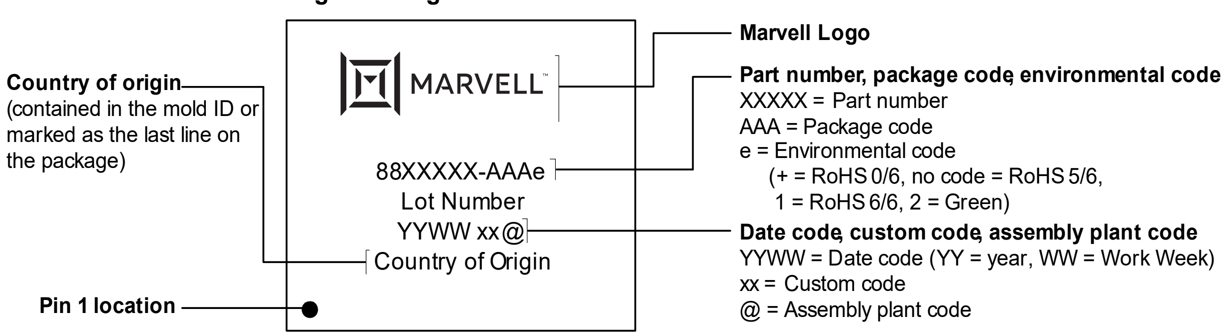
Ordering Part Numbers

88SE9172A1-NNX2C000	56-pin QFN 7 mm x 7 mm, one PCI-Express R2.0, and two 6 Gbps SATA ports.
88SE9182A1-NNX2C000	56-pin QFN 7 mm x 7 mm, two PCI-Express R2.0, and two 6 Gbps SATA ports.

Note: 88SE9130 does not support PATA.

The next figure shows a typical Marvell package marking.

88SE917X/88SE918X Package Marking and Pin 1 Location



Note: The above drawing is not drawn to scale. The location of markings is approximate. Add-on marks are not represented. Flip chips vary widely in their markings and flipchip examples are not shown here. For flip chips, the markings may be omitted per customer requirement.

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CHANGE HISTORY

The following table identifies the document change history for Rev. A.

Document Changes *

Location	Type	Description	Date
Page -iii	Update	Changed Ordering Information as follows: From • 88SE9172A0-NNX2C000 • 88SE9182A0-NNX2C000 To: • 88SE9172A1-NNX2C000 • 88SE9182A1-NNX2C000	23-Dec-10
Page 2-4	Update	Updated section 2.3, SATA Controller. Removed support for AES-256.	23-Sep-10
Page -iii	Update	Changed Ordering Information as follows: From • 88SE9172A0-NNX2C000 • 88SE9182A0-NNX2C000 To: • 88SE9172A1-NNX2C000 • 88SE9182A1-NNX2C000	23-Dec-10
Page 2-4	Update	Updated section 2.3, SATA Controller. Removed support for AES-256.	23-Sep-10
Page 5-4	Parameter	Updated Table 5-3, Power Requirements as follows: • Changed the Analog Power for PCI-E Phy Transmitter (I_{AVDD0})from 70 mA maximum to 55 mA maximum. • Changed the Analog Power for PCI-E Phy Transmitter (I_{AVDD1})from 70 mA maximum to 55 mA maximum. • Changed the Analog Power for SATA Phy (I_{VAA2_0}) from 70 mA maximum to 55 mA maximum. • Changed the Analog Power for SATA Phy (I_{VAA2_1}) from 70 mA maximum to 55 mA maximum. • Changed Digital Core Power from 600 mA maximum to 900 mA maximum.	23-Sep-10

* The type of change is categorized as: Parameter, Revision, or Update. A Parameter change is a change to a spec value, a Revision change is one that originates from the chip Revision Notice, and an Update change includes all other document updates.

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CONTENTS

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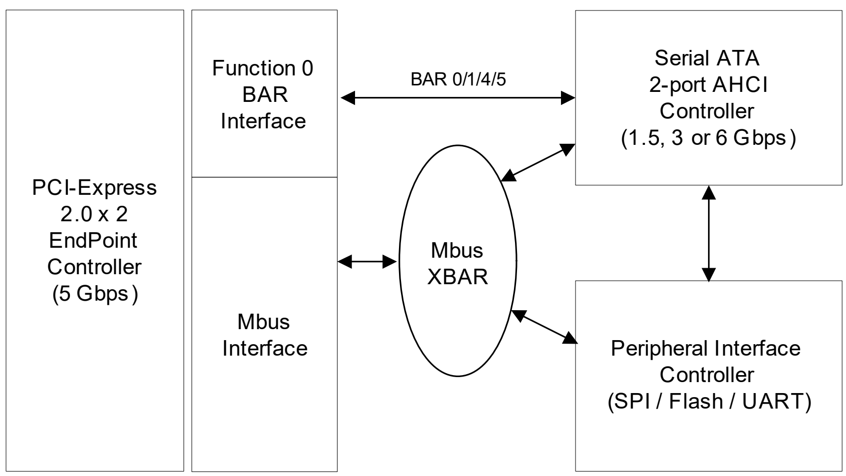
1 OVERVIEW

The 88SE917X/88SE918X is a 2-port, 3 or 6 Gbps SATA controller with a 2-lane PCI Express 2.0 interface.

The 88SE917X/88SE918X controller brings a high-performance 3 or 6 Gbps SATA to desktop/consumer storage applications utilizing a 2-lane PCI Express 2.0 interface. The 88SE917X/88SE918X supports devices compliant with the Serial ATA International Organization: Serial ATA Revision 3.0 specification. Figure 1-1 shows the system block diagram.

Figure 1-1 88SE917X/88SE918X Block Diagram



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2 FEATURES

This chapter contains the following sections:

- General
- PCI Express
- SATA Controller
- SPI Interface Controller
- Peripheral Interface Controller

2.1 General

- 55 nm CMOS process, 1.0V digital core, 1.8V analog, and 3.3V I/O power supplies
- An optional on-die regulator can be used with an external PNP bipolar device to generate a 1.0V supply to the chip from an 1.8V power source
- Reference clock frequency of 25 MHz, provided by an external clock source or generated by an external crystal oscillator

2.2 PCI Express

- PCI Express 2.0 endpoint device
- Supports one lane or two lanes.
- Compliant with PCI Express 2.0 specifications
- Supports communication speed of 2.5 Gbps and 5.0 Gbps
- Supports IDE programming interface registers for the SATA controller.
- Supports AHCI programming interface registers for the SATA controller
- Supports aggressive power management
- Supports error reporting, recovery and correction
- Supports Message Signaled Interrupt (MSI)

2.3 SATA Controller

- Compliant with Serial ATA Specification 3.0
- Supports communication speeds of 6.0 Gbps, 3.0 Gbps, and 1.5 Gbps
- Supports programmable transmitter signal levels
- Supports Gen 1i, Gen 1x, Gen 2i, Gen 2m, Gen 2x, and Gen 3i
- Supports two SATA Ports
- Supports AHCI 1.0 and IDE programming interface
- Supports Native Command Queuing (NCQ)
- Supports Port Multiplier FIS based switching or command based switching
- Supports Partial and Slumber Power Management states
- Supports Staggered Spin-up

2.4 SPI Interface Controller

- A 4-pin interface provides read and write access to an external SPI flash or SPI ROM device
- Vendor specific information stored in the external device is read by the controller during the chip power-up
- PCI BootROM can be stored in the external SPI device and read through the Expansion ROM BAR and the SPI interface controller

2.5 Peripheral Interface Controller

- Six General Purpose I/O (GPIO) ports
  - Each of the 6 GPIO pins can be assigned to act as a general input or output pin
  - Each of the GPIO inputs can be programmed to generate an edge-sensitive or a level-sensitive maskable interrupt
  - Each of the GPIO outputs can be programmed for a connected LED to blink at a user-defined fixed rate. The default rate is 100 ms.

3 PACKAGE

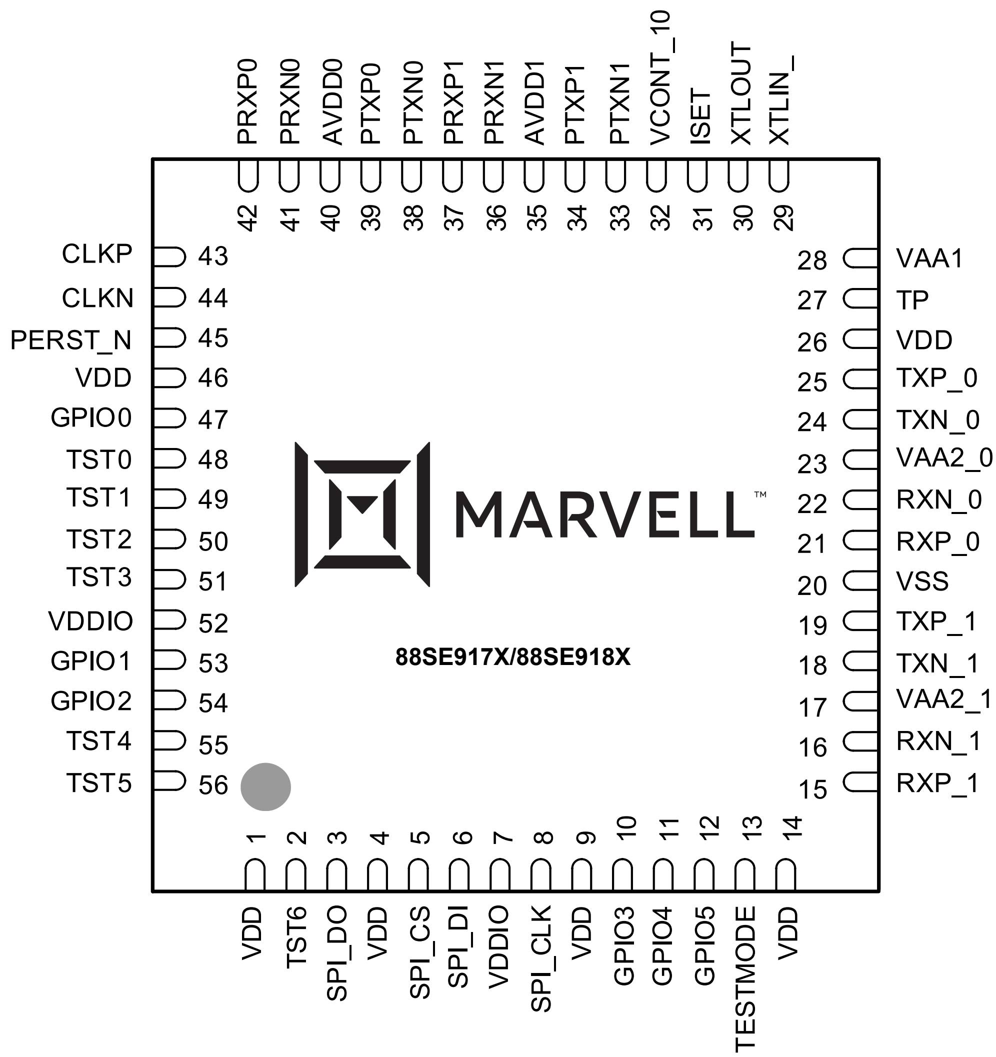
This chapter contains the following sections:

- Pin Diagram
- Mechanical Dimensions
- Signal Descriptions

3.1 Pin Diagram

The 56-pin QFN pin diagram is illustrated in Figure 3-1.

Figure 3-1 Pin Diagram

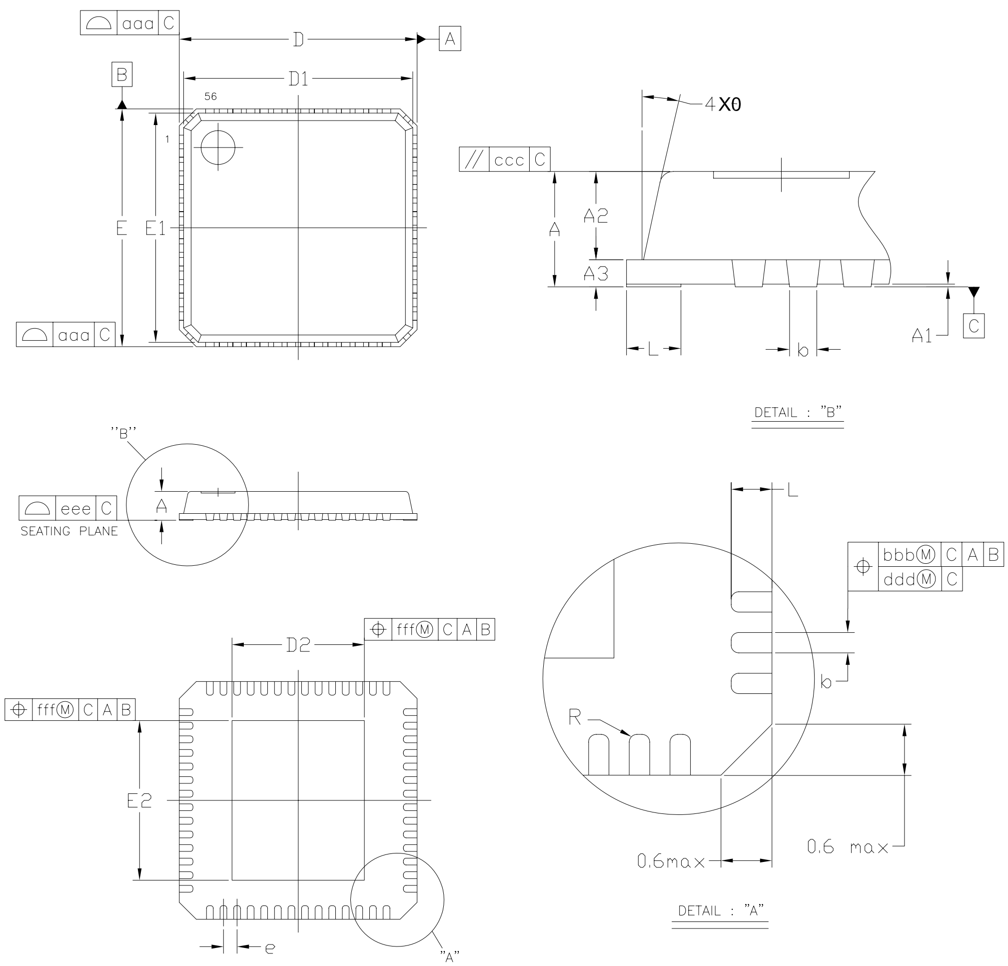


Note: The center area beneath the chip is the Exposed Die Pad (Epad). When designing the PCB, create a solder pad for the Epad and connect the Epad to ground.

3.2 Mechanical Dimensions

The package mechanical drawing is shown in Figure 3-2.

Figure 3-2 Package Mechanical Diagram



The package mechanical dimensions are shown in Figure 3-3.

Figure 3-3 Package Mechanical Dimensions

Symbol				Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
			0.05	0.000	0.001	0.002
A2	0.60	0.65	0.70	0.024	0.026	0.028
A3		0.20 REF			0.008 REF	
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E		7.00 BSC			0.276 BSC	
D1/E1		6.75 BSC			0.266 BSC	
e		0.40 BSC			0.016 BSC	
			0.50	0.012	0.016	0.020
θ	0°	---	14°	0°	---	14°
R	0.075	---	---	0.003	---	---
c	---	---	0.10	---	---	0.004
	---	---	0.07	---	---	0.003
	---	---	0.10	---	---	0.004
	---	---	0.05	---	---	0.002
eee	---	---	0.08	---	---	0.003
fff	---	---	0.10	---	---	0.004

Die Pad Size Options				Shape Option
Option	Symbol	Dimension in mm	Dimension in inch	
	D_2	3.50 ± 0.20	0.138 ± 0.008	Rectangular
	E_2	3.80 ± 0.20	0.150 ± 0.008	

3.3 Signal Descriptions

This section contains the pin types and signal descriptions for the 88SE917X/88SE918X package.

3.3.1 Pin Type Definitions

Pin type definitions are shown in Table 3-1.

Table 3-1 Pin Type Definitions

Pin Type	Definition
I/O	Input and output
I	Input only
O	Output only
mA	DC sink capability (All GPIO and TST pins are 12 mA)
5	5V tolerance (All GPIO and TST pins are 5V tolerance)
A	Analog
PU	Internal pull-up when input
PD	Internal pull-down when input
OD	Open-drain pad

3.3.2 Signal Descriptions

This section outlines the 88SE917X/88SE918X pin descriptions. All signals ending with the letter N indicate an active-low signal.

Table 3-2 PCI Express Interface Signals

Signal Name	Signal Number	Type	Description
PERST_N	45	5, I, PU	PCI Platform Reset. Active low, indicates when the applied power is within thespecified tolerance and stable.
CLKP CLKN	43 44	I, A	Reference Clock. Low voltage differential signals. The clock frequency has to be 100 MHz. ***Note:*** *Both pins are high impedance inputs. A proper termination with 40 to 60 Ohm resistors to ground is needed.*

Table 3-2 PCI Express Interface Signals (continued)

Signal Name	Signal Number	Type	Description
PRXP0 PRXP1 PRXN0 PRXN1	42 37 41 36	I, A	PCI Express differential signals to the controller's receiver.
PTXP0 PTXP1 PTXN0 PTXN1	39 34 38 33	O, A	PCI Express differential signals from the controller's transmitter.

Table 3-3 Serial ATA Interface Signals

Signal Name	Signal Number	Type	Description
TXN_0 TXP_0 TXN_1 TXP_1	24 25 18 19	O, A	Serial ATA Transmitter Differential Outputs.
RXP_1 RXN_1 RXP_0 RXN_0	15 16 21 22	I, A	Serial ATA Receiver Differential Inputs.

Table 3-4 Reference Signals

Signal Name	Signal Number	Type	Description
ISET	31	I/O, A	Reference Current for Crystal Oscillator and PLL. This pin has to be connected to an external 6.04 kΩ 1% resistor to Ground.
XTLOUT	30	O, A	Crystal Output.
XTLIN_OSC	29	I, A	Reference Clock Input. This signal can be from an oscillator, or connected to a crystal with the XTLOUT pin. The clock frequency must be 25 MHz ± 80 ppm.

Table 3-5 General Purpose I/O Signals

Signal Name	Signal Number	Type	Description
GPIO0	47	5, I/O, 12 mA, PU	General Purpose I/O.
GPIO1	53		
GPIO2	54		
GPIO3	10		
GPIO4	11		
GPIO5	12		

Table 3-6 SPI Flash Interface Signals

Signal Name	Signal Number	Type	Description
SPI_CLK	8	5, O, 12 mA	SPI Interface Clock.
SPI_DI	6	5, I, PU	Serial Data In. Connect to the serial flash device’s serial data output (DO).
SPI_CS	5	5, O, 12 mA	SPI Interface Chip Select.
SPI_DO	3	5, O, 12 mA	Serial Data Out. Connect to the serial flash device’s serial data input (DI).

Table 3-7 Test Pins

Signal Name	Signal Number	Type	Description
TST0	48	5, I/O, 12 mA, PU	Digital Test Pins.
TST1	49		
TST2	50		
TST3	51		
TST4	55		
TST5	56		
TST6	2		

Table 3-8 Test Mode Interface Signals

Signal Name	Signal Number	Type	Description
TP	27	I/O, A	Analog Test Point for PCI Express PHY, SATA PHY, crystal oscillator, and PLL.
TESTMODE	13	5, I, PD	Test Mode. Enables chip test modes.

Table 3-9 Power and Ground Pins

Signal Name	Signal Number	Type	Description
VCONT_10	32	O, A	Voltage Control. Output signal which is connected to the base of an external BJT component to generate a 1.0V supply from 1.8V.
VAA2_0 VAA2_1	23 17	Power	Analog power. 1.8V analog power supply for SATA PHY.
VAA1	28	Power	Analog power 1.8V analog power for crystal oscillator, reference current generator, PLL, and internal voltage regulator.
AVDD0 AVDD1	40 35	Power	Analog power. 1.8V analog power supply for PCIe PHY.
VDDIO	7 52	Power	I/O Power. 3.3V analog power supply for digital I/Os.
VDD	1 4 9 14 26 46	Power	1.0V Core Digital Power.
VSS	20	Power	Ground. The main ground is the exposed die-pad (ePad) on the bottom side of the package.

4 LAYOUT GUIDELINES

This chapter describes the system recommendations from the Marvell Semiconductor design and application engineers who work with the 88SE917X/88SE918X. It is written for those who are designing schematics and printed circuit boards for an 88SE917X/88SE918X-based system. Whenever possible, the PCB designer should try to follow the suggestions provided in this chapter.

The information in this chapter is preliminary. Please consult with Marvell Semiconductor design and application engineers before starting your PCB design.

The chapter contains the following sections:

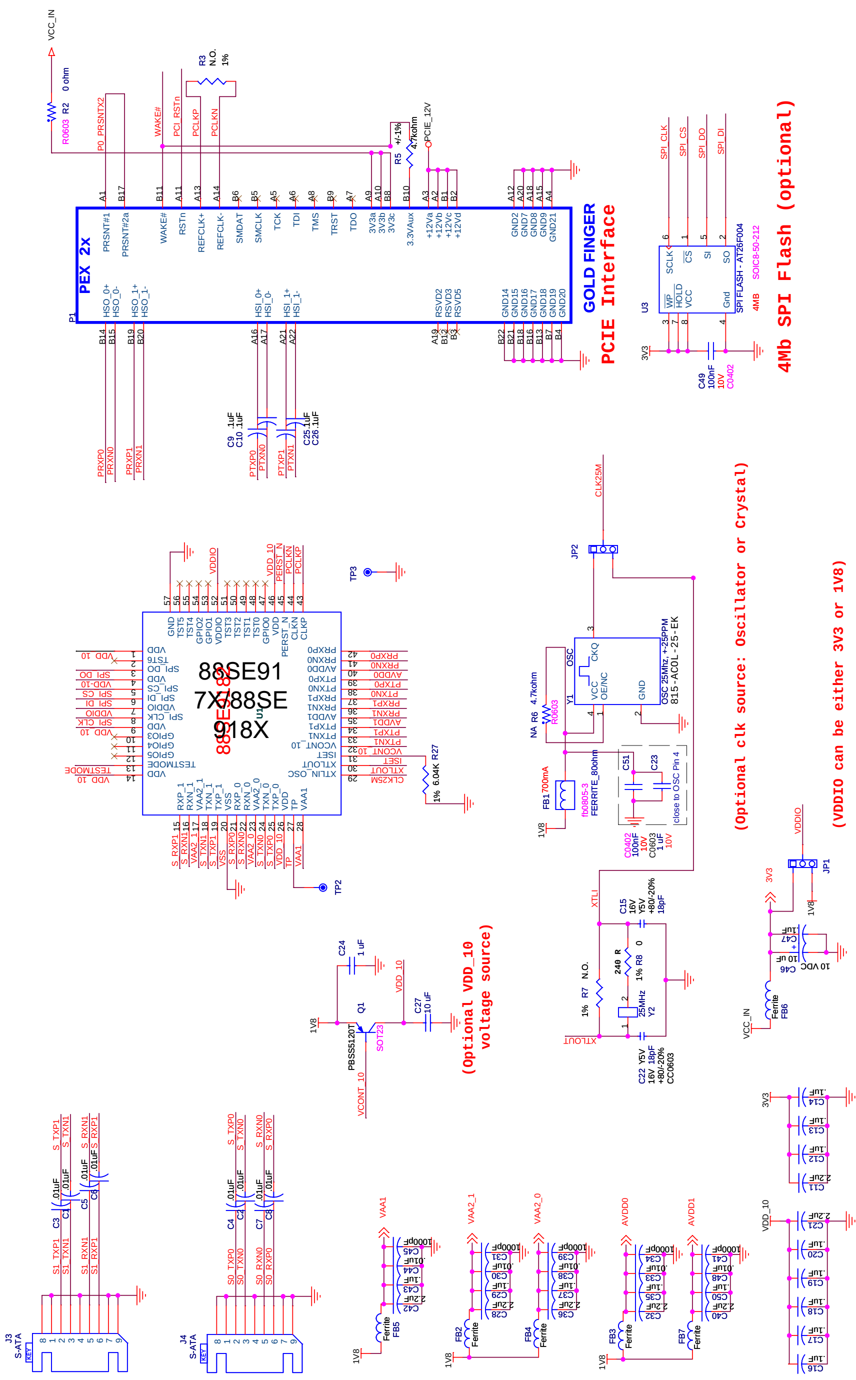
- Board Schematic Example
- External Voltage Regulator
- Layer Stack-up
- Power Supply
- PCB Trace Routing
- Recommended Layout

Refer to Chapter 3, Package, for package information.

4.1 Board Schematic Example

The board schematic consists of the major interfaces of the 88SE917X/88SE918X including SATA and PCI Express. Figure 4-1 shows an example board schematic.

Figure 4-1 88SE917X/88SE918X Example Board Schematic

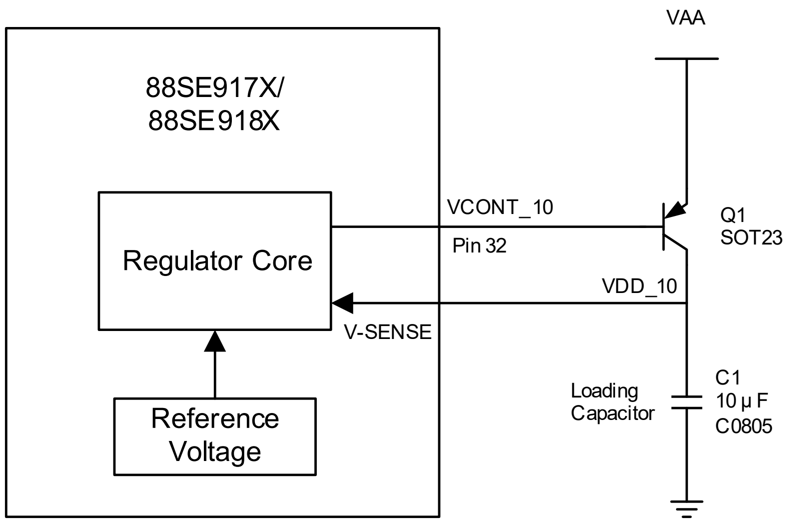


Note: Please contact your Marvell field applications engineer for the latest schematics.

4.2 External Voltage Regulator

The external voltage regulator consists of an external Bipolar Junction Transistor (BJT). The voltage level is on the VCONT_10 voltage control pin and it supplies VDD_10 to the core power. The collector of the BJT provides a stable voltage source and sufficient current to drive the 88SE917X/88SE918X. Figure 4-2 shows a block diagram of the voltage regulator loop.

Figure 4-2 Voltage Regulator Loop Block Diagram



The BJT's supply voltage, VAA, can use the same source as the 88SE917X/88SE918X's VAA1 or VAA2. The BJT and the internal regulator core forms a closed feedback loop to provide a stable voltage for VDD_10.

4.2.1 Recommended Components

For stability reasons, the loading capacitor on the collector output has a low Effective Series Resistance (ESR). The ESR is inversely proportional to the zero location. Table 4-1 describes the recommended components for the reference design.

Table 4-1 Component List

Symbol	Manufacturer	Part Number	Description
C1	Johansen Dialectrics	6R3R15X106KV4E	10 µF Tanceram Capacitor. • ESR of 20–50 mΩ at 1 MHz UGBW • High DC breakdown • Low DC leakage ***Note:*** *The second pole must be kept away from the UGBW because of parasitic RC inside the BJT.*
Q1	Phillips Semiconductor	PBSS5120T	Low V_{CESAT} PNP transistor.

4.2.2 External BJT Requirements

An h_{FE} of 200–400 is required when the BJT output current (IC) reaches its maximum, and low V_{CESAT} (about 200 mV at ICmax). The trace length between the BJT and the VCONT_10 pin of the 88SE917X/88SE918X should be less than 0.5 in. The control signal VCONT_10 connects to the base of the BJT. The PCB trace for the BJT and the load capacitor should be about 10 mils wide.

Regarding thermal characteristics, the mounting pad for the collector should be at least 1 cm^2 tin plated with single-sided copper. The typical power dissipation is approximately 0.5W for this BJT. Electrical requirements for the BJT are listed in Table 5-4, External BJT Requirements.

4.3 Layer Stack-up

The following layer stack up is recommended:

- Layer 1–Topside, Parts, Slow and High Speed Signal Routes, and Power Routes
- Layer 2–Solid Ground Plane
- Layer 3–Power Plane
- Layer 4–Bottom Layer, Slow and High-Speed Signal Routes, and Power Routes

5 mil traces and 5 mil spacing are the recommended minimum requirements.

4.3.1 Layer 1–Topside, Parts, Slow and High Speed Signal Routes, and Power Routes

All active parts are to be placed on the topside. Some of the differential pairs for SATA and PCI Express are routed on the top layer, differential 100 ohm impedance needs to be maintained for those high speed signals.

4.3.2 Layer 2–Solid Ground Plane

A solid ground plane should be located directly below the top layer of the PCB. This layer should be a minimum distance below the top layer in order to reduce the amount of crosstalk and EMI. There should be no cutouts in the ground plane. Use of 1 ounce copper is recommended.

4.3.3 Layer 3–Power Plane

Use solid planes on layer 3 to supply power to the ICs on the PCB. Avoid narrow traces and necks on this plane.

4.3.4 Layer 4–Bottom Layer, Slow and High-Speed Signal Routes, and Power Routes

Some of the differential pairs for SATA and PCI Express are routed on the top layer, differential 100Ω impedance needs to be maintained for those high speed signals. The high speed signals have the return current on the third layer, which is the power plane. Make sure there is no cut-out under the signal path.

4.4 Power Supply

The 88SE917X/88SE918X operates using the following power supplies:

- VDD Power (1.0V) for the digital core
- Analog Power Supply (1.8V)

4.4.1 VDD Power (1.0V)

All digital power pins (VDD pins) must be connected directly to a VDD plane in the power layer with short and wide traces to minimize digital power-trace inductances.

Use vias close to the VDD pins to connect to this plane and avoid using the traces on the top layer. Marvell recommends placing capacitors around the three sides of the PCB near VDD pins with the following dimensions:

- 1 nF (1 capacitor)
- 0.1 µF (2 capacitors)
- 2.2 µF (1 ceramic capacitor)

The 2.2 µF ceramicdecoupling capacitor is needed to filter thelower frequency power-supply noise.

To reduce system noise, the use of high-frequency surface-mount monolithic ceramic bypass capacitors should be placed as close as possible to the channel VDD pins. At least one decoupling capacitor should be placed on each side of the IC package.

Short and wide copper traces should be used to minimize parasitic inductances. Low-value capacitors (1,000–10,000 pF) are preferable over higher values because they are more effective at higher frequencies.

4.4.2 Analog Power Supply (1.8V)

The PCI Express analog supply provides power for the PCI Express link's high speed serial signals. To ensure high speed link operation, use a series of bypass capacitors for the supplies. A typical capacitor value combination is 1 nF, 0.1µF, and 2.2 µF.

4.4.3 Bias Current Resistor (RSET)

Connect a 6.04KΩ (1%) resistor between the ISET pin and the adjacent top ground plane. This resistor should lie as close as possible to the ISET pin.

4.5 PCB Trace Routing

The stack-up parameters for the reference board are shown in Table 4-2.

Table 4-2 PCB Board Stack-up Parameters

Layer	Layer Description	Copper Weight (oz)	Target Impedance (±10%)
1	Signal	0.5	50
2	GND	1	N/A
3	Power	1	N/A
4	Signal	1	50

4.6 Recommended Layout

Solid ground planes are recommended. However, special care should be taken when routing VAA and VSS pins.

The following general tips describe what should be considered when determining your stack-up and board routing. These tips are not meant to substitute for consulting with a signal-integrity expert or doing your own simulations.

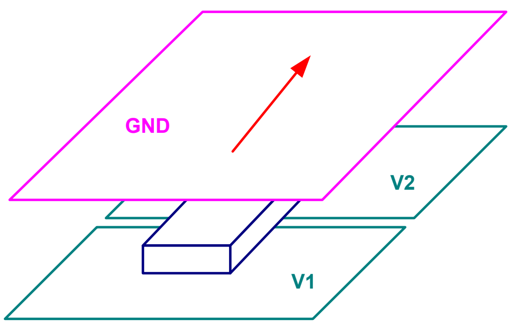
Note: Specific numbers or rules-of-thumb are not used here because they might not be applicable in every situation.

- Do not split ground planes.

  Keep good spacing between possible sensitive analog circuitry on your board and the digital signals to sufficiently isolate noise. A solid ground plane is necessary to provide a good return path for routing layers. Try to provide at least one ground plane adjacent to all routing layers (see Figure 4-3).
- Keep trace layers as close as possible to the adjacent ground or power planes.

  This helps minimize crosstalk and improve noise control on the planes.

Figure 4-3 Trace Has At Least One Solid Plane For Return Path



- When routing adjacent to only a power plane, do not cross splits.

  Route traces only over the power plane that supplies both the driver and the load. Otherwise, provide a decoupling capacitor near the trace at the end that is not supplied by the adjacent power plane.
- Critical signals should avoid running parallel and close to or directly over a gap.

  This would change the impedance of the trace.
- Separate analog powers onto opposing planes.

  This helps minimize the coupling area that an analog plane has with an adjacent digital plane.
- For dual strip-line routing, traces should only cross at 90 degrees.

  Avoid more than two routing layers in a row to minimize tandem crosstalk and to better control impedance.
- Planes should be evenly distributed in order to minimize warping.
- Calculating or modeling impedance should be made prior to routing.

  This helps ensure that a reasonable trace thickness is used and that the desired board thickness is available. Consult with your board fabricator for accurate impedance.

- Allow good separation between fast signals to avoid crosstalk.

  Crosstalk increases as the parallel traces get longer.

- When packages become smaller, route traces over a split power plane

  Smaller packages force vias to become smaller, thereby reducing board thickness and layer counts, which might create the need to route traces over a split power plane. Some alternatives to provide return path for these signals are listed below.

  Caution must be used when applying these techniques. Digital traces should not cross over analog planes, and vice-versa. All of these rules must be followed closely to prevent noise contamination problems that might arise due to routing over the wrong plane.

  By tightly controlling the return path, control noise on the power and ground planes can be controlled.

  - Place a ground layer close enough to the split power plane in order to couple enough to provide buried capacitance, such as SIG-PWR-GND (see Figure 4-4). Return signals that encounter splits in thissituation simply jumps to the ground plane, over the split, and back to the other power plane. Buried capacitance provides the benefit of adding low inductance decoupling to your board. Your fabricator may charge for a special license fee and special materials. To determine the amount of capacitance your planes provide, use the following equation:

    $$C = 1.249 \bullet 10^{-13} \bullet E_r \bullet L \bullet W / H$$

    Where E_R is the dielectric coefficient, L • W represents the area of copper, and H is the separation between planes.

  - Provide return-path capacitors that connect to both power planes and jumps the split. Place them close to the traces so that there is one capacitor for every four or five traces. The capacitors would then provide the return path (see Figure 4-5).
  - Allow only static or slow signals on layers where they are adjacent to split planes.

Figure 4-4 shows the ground layer close to the split power plane.

Figure 4-4 Close Power and Ground Planes Provide Coupling For Good Return Path

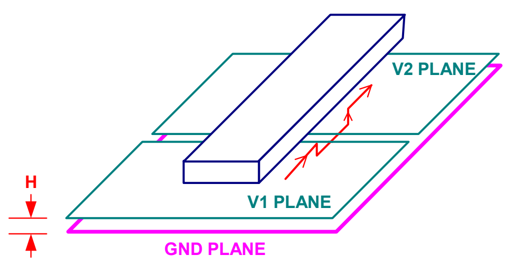
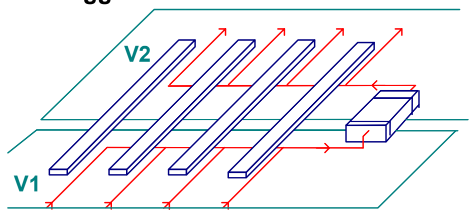


Figure 4-5 shows the thermal ground plane in relation to the return-path capacitor.

Figure 4-5 Suggested Thermal Ground Plane On Opposite Side of Chip



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5 ELECTRICAL SPECS

This chapter contains the following sections:

- Absolute Maximum Ratings
- Recommended Operating Conditions
- Power Requirements
- Voltage Regulator Requirements
- DC Electrical Characteristics
- Thermal Data

5.1 Absolute Maximum Ratings

Table 5-1 defines the absolute maximum ratings for the 88SE917X/88SE918X.

Table 5-1 Absolute Maximum Ratings*

Parameter	Symbol	Min	Typ	Max	Units
Absolute Analog Power for PCI-E Phy	$AVDD0_{abs}$	-0.5		1.98	
Absolute Analog Power for PCI-E Phy	$AVDD1_{abs}$	-0.5		1.98	
Absolute Analog Power for Crystal Oscillator and PLL	$VAA1_{abs}$	-0.5		1.98	V
Absolute Analog Power for SATA Phy	$VAA2\_0_{abs}$	-0.5		1.98	V
Absolute Analog Power for SATA Phy	$VAA2\_1_{abs}$	-0.5		1.98	V
Absolute Digital Core Power	VDD_{abs}	-0.5		1.10	V
Absolute Digital I/O Power (3.3V)	$VDDIO_{abs}$	-0.5		3.63	V
Absolute Digital I/O Power (1.8V)	$VDDIO_{abs}$	-0.5		1.98	V

* Estimated values are provided until characterization is complete.

5.2 Recommended Operating Conditions

Table 5-2 defines the recommended operating conditions for the 88SE917X/88SE918X.

Table 5-2 Recommended Operating Conditions*

Parameter	Symbol	Min	Typ	Max	Units
Analog Power for PCI-E Phy	$AVDD0_{op}$	1.71	1.8	1.98	V
Analog Power for PCI-E Phy	$AVDD1_{op}$	1.71	1.8	1.98	V
Analog Power for Crystal Oscillator and PLL	$VAA1_{op}$	1.71	1.8	1.98	V
Analog Power for SATA Phy	$VAA2\_0_{op}$	1.71	1.8	1.98	V
Analog Power for SATA Phy	$VAA2\_1_{op}$	1.71	1.8	1.98	
Digital Core Power	VDD_{op}	0.95	1.0	1.10	V
Digital I/O Power (3.3V)	$VDDIO_{op}$	3.135	3.3	3.63	V
Digital I/O Power (1.8V)	$VDDIO_{op}$	1.71	1.8	1.98	V
Internal Bias Reference	$ISET_{op}$	5.98	6.04	6.10	KΩ
Ambient Operating Temperature, Advanced Commercial		0		85	°C
Ambient Operating Temperature, Industrial		-40		85	°C
Junction Operating Temperature, Advanced Commercial		0		125	°C
Junction Operating Temperature, Industrial		-20		125	°C

* Estimated values are provided until characterization is complete.

† Engineering samples only. Estimated value provided until characterization is complete. Marvell does not have automotive or military qualification for industrial temperature versions of 88SE917X/88SE918X.

5.3 Power Requirements

Table 5-3 defines the power requirements for the 88SE917X/88SE918X.

Table 5-3 Power Requirements*

Parameter	Symbol	Min	Typ	Max	Units
Analog Power for PCI-E Phy Transmitter	I_{AVDD0}			55	mA
Analog Power for PCI-E Phy Transmitter	I_{AVDD1}			55	mA
Analog Power for Crystal Oscillator and PLL	I_{VAA1}			10	mA
Analog Power for SATA Phy	I_{VAA2_0}			55	mA
Analog Power for SATA Phy	I_{VAA2_1}			55	mA
Digital Core Power	I_{VDD}			900	mA
Digital I/O Power (3.3V)†	I_{VDDIO}			50	mA

* Estimated values are provided until characterization is complete.
† The digital I/O power supply can be either 3.3V or 1.8V.

5.4 Voltage Regulator Requirements

Table 5-4 defines the requirements for the external Bipolar Junction Transistor (BJT) used with the regulator core.

Table 5-4 External BJT Requirements*

Parameter	Symbol	Min	Typ	Max	Units
DC Current Gain of the BJT	h_{FE}	200			
Collector-Emitter Saturation Voltage	V_{CEsat}			-200	mV
Power Dissipation of the BJT	P			500	mW
Equivalent series resistance of the capacitor	ESR	20		50	mΩ
Decoupling capacitor (ceramic)	C	10			μF

* Estimated values are provided until characterization is complete.

5.5 DC Electrical Characteristics

Table 5-5 defines the DC electrical characteristics for the 88SE917X/88SE918X.

Table 5-5 DC Electrical Characteristics*

Parameter		Test Condition	Min	Typ	Max	Units
Input Low Level Voltage	V_{IL}		-0.4		0.25 x VDDIO	V
Input High Level Voltage	V_{IH}		0.8 x VDDIO		5.5	V
Output Low Level Current	I_{OL}	V_{PAD} = 0.4V	5			mA
Output High Level Current	I_{OH}	$V_{PAD =}$ VDDIO – 0.4V	5			mA
Pull Up Strength	I_{PU}	$V_{PAD =}$ 0.5 x VDDIO	10			µA
Pull Down Strength	I_{PD}	$V_{PAD =}$ 0.5 x VDDIO	10			µA
Input Leakage Current	I_{LK}	0 < V_{PAD} < VDDIO			10	µA
Input Capacitance	C_{IN}	0 < V_{PAD} < 5.5V			5	pF

* Estimated values are provided until characterization is complete.

5.6 Thermal Data

It is recommended to read application note *AN-63 Thermal Management for Selected Marvell® Products* (Document Number MV-S300281-00) and the *ThetaJC, ThetaJA, and Temperature Calculations White Paper*, available from Marvell, before designing a system. These documents describe the basic understanding of thermal management of integrated circuits (ICs) and guidelines to ensure optimal operating conditions for Marvell products.

Table 5-6 provides the estimated thermal data for the 88SE917X/88SE918X. Actual values are TBD.

Table 5-6 shows the values for the package thermal parameters for the48-lead Quad Flat Non-Lead package (QFN 48) mounted on a 4-layer PCB.

Table 5-6 Package Thermal Data

Parameter	Definition	Airflow Value*			
		0 m/s	**1 m/s**	**2 m/s**	**3 m/s**
θ_{JA}	Thermal resistance: junction to ambient	29.9 C/W	26.6 C/W	25.5 C/W	24.8 C/W
Ψ_{JB}	Thermal characterization parameter: junction to bottom surface center of the package.	15.60 C/W	15.59 C/W	15.58 C/W	15.57 C/W
ψ_{JT}	Thermal characterization parameter: junction to top center	0.63 C/W	0.93 C/W	1.17 C/W	1.34 C/W

* Estimated values are provided until characterization is complete