88SM9602

SATA 6 Gbps 1-to-2 Port Multiplier

Preliminary Specifications

Doc No. MV-S109301-00 Rev. A

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Document Classification: Proprietary

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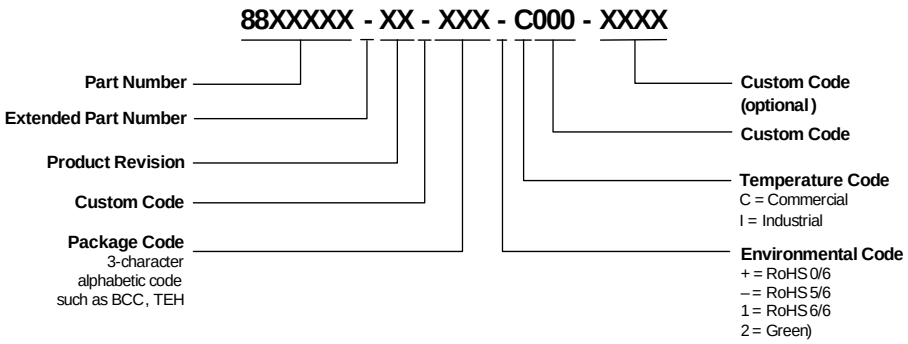
ORDERING INFORMATION

Ordering Part Numbers and Package Markings

The following figure shows the ordering part numbering scheme for the 88SM9602 part. For complete ordering information, contact your Marvell FAE or sales representative.

Figure 0-1 Sample Ordering Part Number



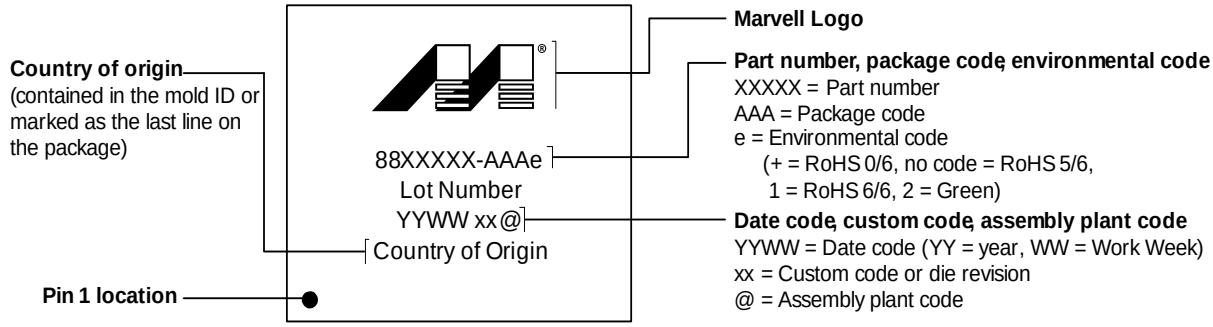
The standard ordering part numbers for the respective solutions are indicated in the following table.

Ordering Part Numbers

Part Number	Description
88SM9602A3-NMD2C000	48-pin 6mm x 6mm Commercial Grade MQFN, SATA 6 Gbps One-to-Two Port Multiplier

The next figure shows a typical Marvell package marking.

Figure 0-2 88SM9602 Package Marking and Pin 1 Location



Note: The above drawing is not drawn to scale. The location of markings is approximate. Add-on marks are not represented. Flip chips vary widely in their markings and flip chip examples are not shown here. For flip chips, the markings may be omitted per customer requirement.

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88SM9602 Revision Notice

This document lists the revisions for 88SM9602

R1.3 (A3)

Item	Component	Type	Summary	Description	Firmware Impact?
1	SATA Transmitter	Fixed Issue	Modified SATA analog design to eliminate SATA transmitter emitting glitch signals.	Modified SATA analog design to eliminate SATA transmitter emitting glitch signals. Turned the PHY PLL and transmitter driver back on after waking up from the Slumber mode. Also, disabled the transmitter driver to high-impedance mode before PLL achieves the lock condition. Disabling the transmitter driver guarantees that the transmitter clock is alive before enabling the transmitter driver and therefore eliminates the glitches. Added to disable the design change by setting this field to 1.	N/A*

* This product does not have firmware.

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R1.2 (A2)

Item	Component	Type	Summary	Description	Firmware Impact?
2	Power	Fixed Issue	Fixed the racing condition between the host-command transmit and single Device Initiated Power Management (DIPM), to wake up the device when data must be sent.	Fixed the racing condition between the host-command transmit and single device DIPM, to wake up the device when data must be sent. The 88SM9602 has a racing window in the interval between when the host command is transmitted to a device port and when the device port enters Power Saving mode. When hitting this window, the Port Multiplier cannot wake up the device port to send the command and cause the command time-out.	N/A*

* This product does not have firmware.

Known Issues Not Fixed in R1.2 (A2)

Item	Component	Type	Summary	Description	Firmware Impact?
1	SATA PHY	Known issue	A TX glitch can be seen during the slumber wake-up or speed change.	A TX glitch can be seen during the slumber wake-up or speed change. The PLL clock may be off for a certain time while the PLL is locking to the target frequency. The off state drives a 0 or 1 to the TXP and TXN, which looks like a glitch in the idle state.	N/A*

* This product does not have firmware.

CHANGE HISTORY

The following table identifies the document change history for Rev. A.

Document Changes *

Location	Type	Description	Date
Page -iii	Update	Changed part number to 88SM9602A3-NMD2C000 from 88SM9602A2-NMD2C000.	May 6, 2015
Global	Update	Updated section 4.1, Board Schematic Example as follows: • Replaced schematic diagrams with updated versions.	April 7, 2015
Global	Update	Added an introduction sentence to all tables in the document.	September 26, 2013
Page 2-2	Update	Removed the following bullet item in section 2.1, General: “Full scan for high-production test coverage and PHY self-test.”	October 21, 2014
Page 2-3	Update	Added the following bullet item for 2.2, Functional: “Supports SATA Port Multiplier Rev. 1.2.”	February 28,2013
Page 7-11	Parameter	Corrected the default value of PORT_NUM (R002h [3:0]) from 5h to Vh.	February 26, 2013

* The type of change is categorized as: Parameter, Revision, or Update. A Parameter change is a change to a spec value, a Revision change is one that originates from the chip Revision Notice, and an Update change includes all other document updates.

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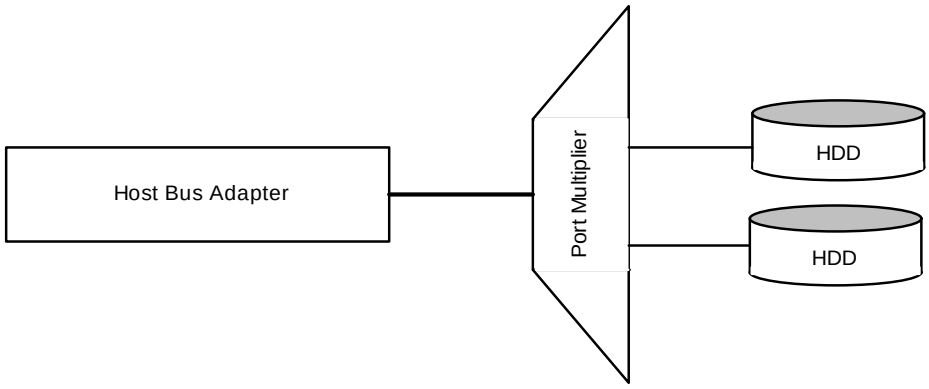
CONTENTS

1 OVERVIEW

The 88SM9602 is a SATA port multiplier that allows an active host connection to communicate with two 6 gbps devices.

Figure 1-1 illustrates a typical port multiplier configuration.

Figure 1-1 Overview (Two Port)



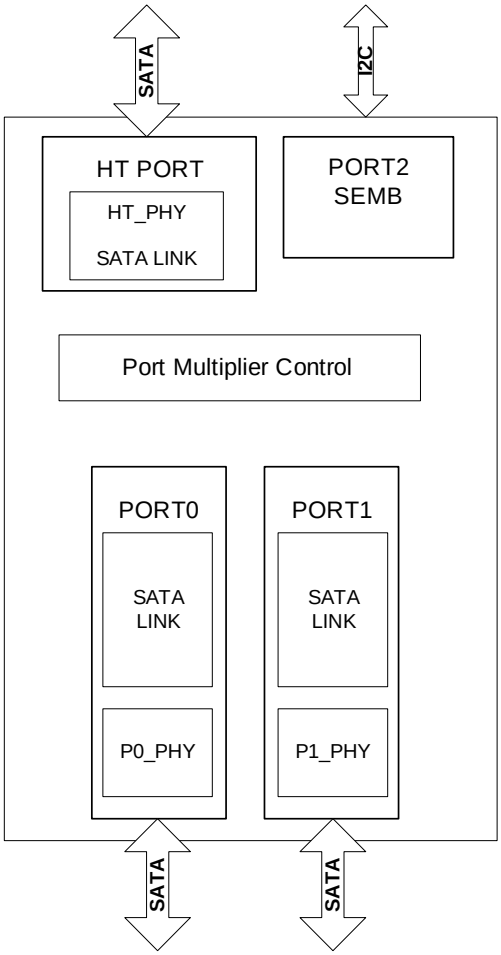
The 88SM9602 port multiplier employs Marvell SATA 6 Gbps Physical Layer (PHY) technology and recognizes the SATA-defined OOB sequence and speed-negotiation sequence on all of its SATA ports.

The 88SM9602 has programmable amplitude and pre-emphasis settings for a range of drive capabilities to support various backplane and cabling environments.

All device ports and the host port can be set up through the host port or UART interface to perform SATA self-tests at the same time.

Figure 1-2 shows the 88SM9602 blocks.

Figure 1-2 88SM9602 Blocks



2 FEATURES

This chapter contains the following sections:

2.1 General

- 55 nm CMOS technology.
- Supports Serial ATA Revision 3.1 Specification, with communication speeds of 1.5 Gbps, 3 Gbps, and 6 Gbps on host and device ports.
- 1.0V, 1.8V, and 3.3V power.
- 48-pin MQFN ePad package.
- PHY test mode.
- One host port.
- Two
- Supports 25 MHz reference clock.

2.2 Functional

- 115200 bps UART access.
- Spread-spectrum clocking transmission.
- SATA BIST over host and device links.
- SAF-TE (Enclosure Management).
- FIS-based switching.
- One SEMB port/SM bus port (optional).
- SPI interface for internal register programming.
- Supports SATA Port Multiplier Rev. 1.2.

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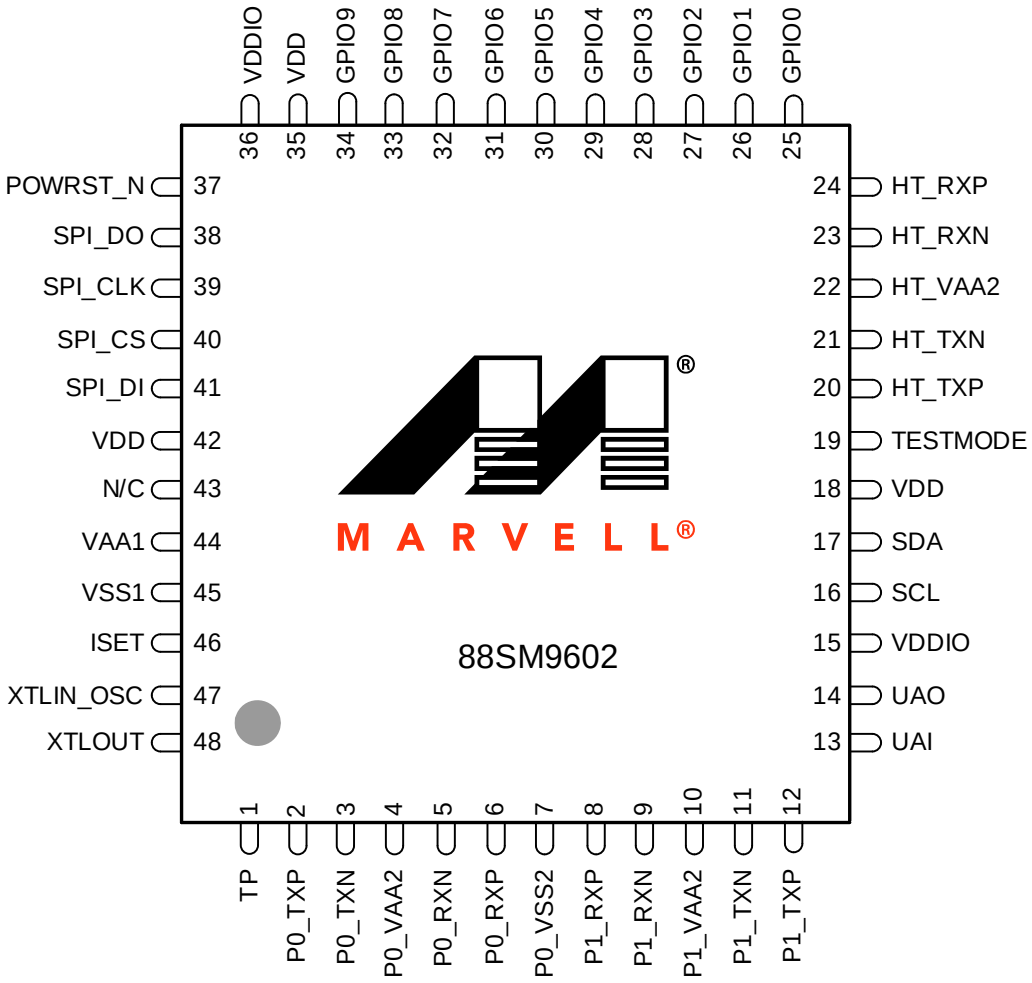
3 PACKAGE

This chapter contains the following sections:

3.1 Package Pin-Out

Figure 3.2 illustrates the package pin-out:

Figure 3-1 Package Pin-Out 48-Pin MQFN



3.2 Package Dimensions

Figure 3-2 shows the mechanical drawing.

Figure 3-2 Mechanical Drawing

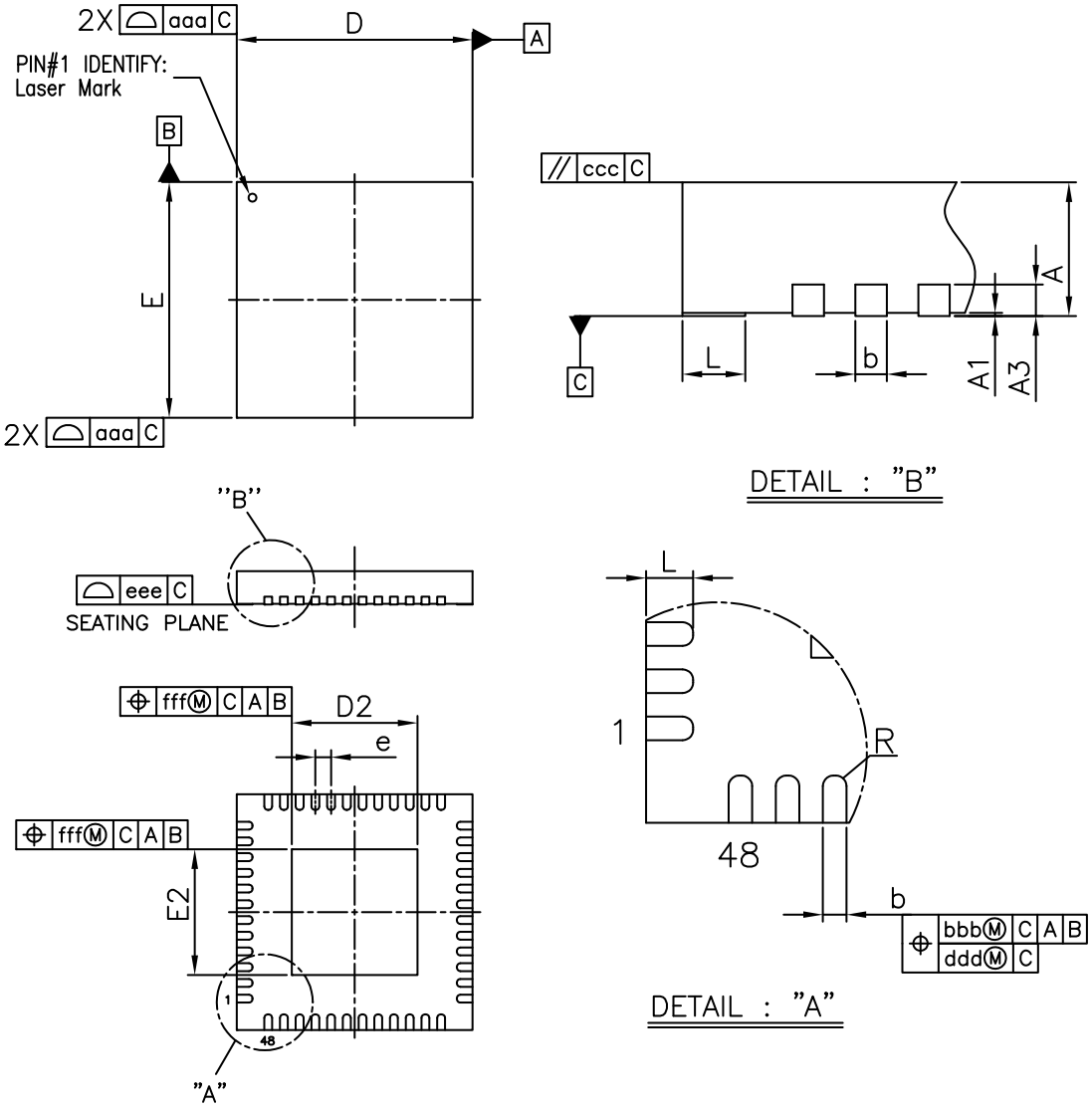


Figure 3-3 shows the mechanical dimensions.

Figure 3-3 Mechanical Dimensions

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	5.90	6.00	6.10	0.232	0.236	0.240
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
R	0.075	---	---	0.003	---	---
aaa	---	---	0.10	---	---	0.004
bbb	---	---	0.07	---	---	0.003
ccc	---	---	0.10	---	---	0.004
ddd	---	---	0.05	---	---	0.002
eee	---	---	0.08	---	---	0.003
fff	---	---	0.10	---	---	0.004

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER

2. REFERENCE DOCUMENT : JEDEC MO-220.

Die Pad Size Options			Shape
Symbol	Dimension in mm	Dimension in inch	
D_2	2.90 ± 0.15	0.114 ± 0.006	Square
E_2	2.90 ± 0.15	0.114 ± 0.006	

3.3 Pin Descriptions

This section contains the following subsections:

- Pin Type Definitions
- Pin List

3.3.1 Pin Type Definitions

This section outlines the 88SM9602 pin descriptions. All signals ending with the letter _N indicate an active-low signal. Table 3-1 shows the pin type definitions.

Table 3-1 Pin Type Definitions

Pin Type	Definition
I/O	Input and output
I	Input only
O	Output only
PD	Internal pull-down resistor (50 kΩ)
PU	Internal pull-up resistor (50 kΩ)
mA	DC sink capability
5	5V tolerance

3.3.2 Pin List

This section lists the 88SM9602 signals.

Table 3-2 Serial ATA Interface Signals

Signal Name	Signal Number	Type	Description
P0_TXP	2	O	Serial ATA Transmitter Differential Outputs.
P0_TXN	3	O	
P1_TXP	12	O	
P1_TXN	11	O	
HT_TXP	20	O	
HT_TXN	21	O	
P0_RXN	5	I	Serial ATA Receiver Differential Inputs.
P0_RXP	6	I	
P1_RXN	9	I	
P1_RXP	8	I	
HT_RXN	23	I	
HT_RXP	24	I	

Table 3-3 Chip Power-On Reset Signal

Signal Name	Signal Number	Type	Description
POWRST_N	81	I	Power on Reset. Active Low.

Table 3-4 UART Two-Wire Serial Interface Signals

Signal Name	Signal Number	Type	Description
UAO	14	O	UART Data Output.
UAI	13	I	UART Data Input.
SCL	16	I/O	Serial Clock.
SDA	17	I/O	Serial Data.

Table 3-5 Configuration and Test Pins Signals

Signal Name	Signal Number	Type	Description
GPIO9	34	I/O	General Purpose I/O.
GPIO8	33	I/O	General Purpose I/O.
GPIO7	32	I/O	General Purpose I/O.
GPIO6	31	I/O	General Purpose I/O.
GPIO5	30	I/O	General Purpose I/O.
GPIO4	29	I/O	General Purpose I/O.
GPIO3	28	I/O	General Purpose I/O
GPIO2	27	I/O	General Purpose I/O.
GPIO1	26	I/O	General Purpose I/O.
GPIO0	25	I/O	General Purpose I/O.

Table 3-6 Reference Signals

Signal Name	Signal Number	Type	Description
ISET	46	I	Reference Current for Analog Circuits. This pin must be connected from an external 6.04 kΩ 1% resistor to the Ground.
XTLOUT	48	O	Crystal Output.
XTLIN_OSC	47	I	Reference Clock Input. This pin can be connected from a crystal or an oscillator.

Table 3-7 Power Pin Signals

Signal Name	Signal Number	Type	Description
HT_VAA2	22	I	1.8V Power Source for Host Port SATA PHY.
P0_VAA2	4	I	1.8V Power Source for Device Port 0 SATA PHY.
P1_VAA2	10	I	1.8V Power Source for Device Port 1 SATA PHY.
VAA1	44	I	1.8V Power Source for Analog Logic.
VSS1	45	I	Ground for Analog Logic.
P0_VSS2	7	I	Ground for SATA PHY.
VDDIO	15, 36	I	3.3V Power Source for Digital IO.
VDD	18, 35, 42	I	1.0V Power Source for Digital.

Table 3-8 SPI Flash Interface Signals

Signal Name	Signal Number	Type	Description
SPI_DO	38	O	Data Output of SPI Flash Interface.
SPI_CLK	39	O	Clock Output of SPI Flash Interface.
SPI_CS	40	O	Mode Select of SPI Flash Interface ***Note:***
SPI_DI	41	I	Data Input of SPI Flash Interface.

Table 3-9 Test Mode Interface Signals

Signal Name	Signal Number	Type	Description
TESTMODE	19	I	Chip Test Mode.
TP	1	O	Analog Test Point.

Table 3-10 Not Connected

Signal Name	Signal Number	Type	Description
N/C	43	N/A	Not connected.

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4 LAYOUT GUIDELINES

This chapter describes the system recommendations from the Marvell Semiconductor design and application engineers who work with the 88SM9602. It is written for those who are designing schematics and printed circuit boards for an 88SM9602-based system. Whenever possible, the PCB designer must try to follow the suggestions provided in this chapter.

The information in this chapter is preliminary. Consult with Marvell Semiconductor design and application engineers before starting your PCB design.

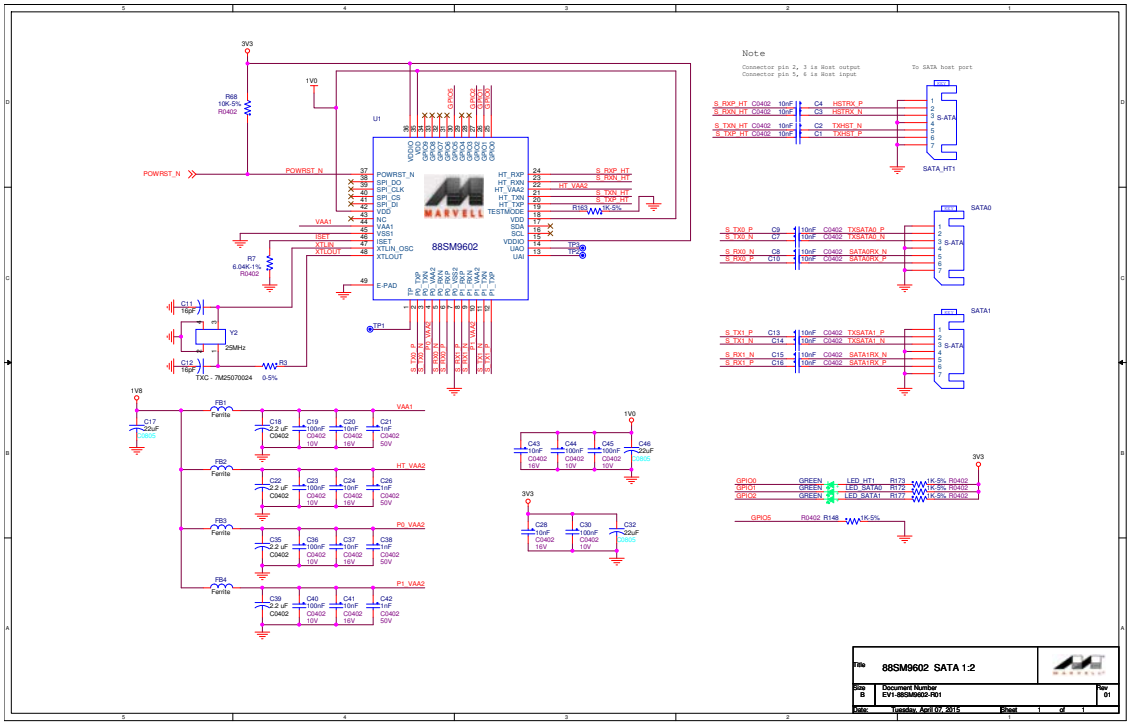
The chapter contains the following sections:

See Chapter 3, Package, for package information.

4.1 Board Schematic Example

The board schematic consists of the major interfaces of the 88SM9602. Figure 4-1 shows an example board schematic.

Figure 4-1 88SM9602 Example Board Schematic



Note: This diagram is for reference only. Contact your Marvell field applications engineer for the latest schematics.

4.2 Layer Stack-Up

The recommended minimum requirements are 5-mil traces and 5-mil spacing.The following layer stack up is recommended:

- Layer 1–Topside, Parts, Slow and High Speed Signal Routes, and Power Routes
- Layer 2–Solid Ground Plane
- Layer 3–Power Plane
- Layer 4–Bottom Layer, Slow and High-Speed Signal Routes, and Power Routes

4.2.1 Layer 1–Topside, Parts, Slow and High Speed Signal Routes, and Power Routes

All active parts are to be placed on the topside. Some of the differential pairs for SATA are routed on the top layer, differential 100Ω impedance must be maintained for those high speed signals.

4.2.2 Layer 2–Solid Ground Plane

A solid ground plane must be located directly below the top layer of the PCB. This layer must be a minimum distance below the top layer to reduce the amount of crosstalk and EMI. No cutouts must exist in the ground plane. It is recommended to use 1 ounce copper.

4.2.3 Layer 3–Power Plane

Use solid planes on layer 3 to supply power to the ICs on the PCB. Avoid narrow traces and necks on this plane.

4.2.4 Layer 4–Bottom Layer, Slow and High-Speed Signal Routes, and Power Routes

Some of the differential pairs for SATA are routed on the top layer, differential 100Ω impedance must be maintained for those high speed signals. The high speed signals have the return current on the third layer, which is the power plane. No cut-out must exist under the signal path.

4.3 Power Supply

The 88SM9602 operates using the following power supplies:

- VDD Power (1.0V)
- Analog Power Supply (1.8V)
- VDDIO Power (3.3V)
- Power-on-Reset Timing Requirement
- Bias Current Resistor (RSET)

4.3.1 VDD Power (1.0V)

All digital power pins (VDD pins) must be connected directly to a VDD plane in the power layer with short and wide traces to minimize digital power-trace inductances.

Use vias close to the VDD pins to connect to this plane and avoid using the traces on the top layer. Marvell recommends placing capacitors around the three sides of the PCB near VDD pins with the following dimensions:

- 1 nF (1 capacitor)
- 0.1 µF (2 capacitors)
- 2.2 µF (1 ceramic capacitor)

The 2.2 µF ceramic decoupling capacitor is needed to filter the lower frequency power-supply noise.

To reduce system noise, the use of high-frequency surface-mount monolithic ceramic bypass capacitors must be placed as close as possible to the channel VDD pins. At least one decoupling capacitor must be placed on each side of the IC package.

Short and wide copper traces must be used to minimize parasitic inductances. Low-value capacitors (1,000–10,000 pF) are preferable over higher values because they are more effective at higher frequencies.

4.3.2 Analog Power Supply (1.8V)

The 1.8V power is for analog design of the chip.

4.3.3 VDDIO Power (3.3V)

The digital power (3.3V) is the power supply for the digital pad.

4.3.4 Power-on-Reset Timing Requirement

The minimum timing requirement for power on reset is 50 µs after all power supplies are stable and before the power-on-reset signal is released.

4.3.5 Bias Current Resistor (RSET)

This resistor must connect a 6.04 KΩ (1%) resistor to the ISET pin and the adjacent top ground plane. It must lie as close as possible to the ISET pin.

4.4 PCB Trace Routing

The stack-up parameters for the reference board are shown in Table 4-1.

Table 4-1 PCB Board Stack-up Parameters

Layer	Layer Description	Copper Weight (oz)	Target Impedance (±10%)
1	Signal	0.5	50
2	GND	1	N/A
3	Power	1	N/A
4	Signal	0.5	50

4.5 Recommended Layout

Solid ground planes are recommended. However, special care must be taken when routing VAA and VSS pins.

The following general tips describe what must be considered when determining your stack-up and board routing. These tips are not meant to substitute for consulting with a signal-integrity expert or doing your own simulations.

Note: Specific numbers or rules-of-thumb are not used here because they might not be applicable in every situation.

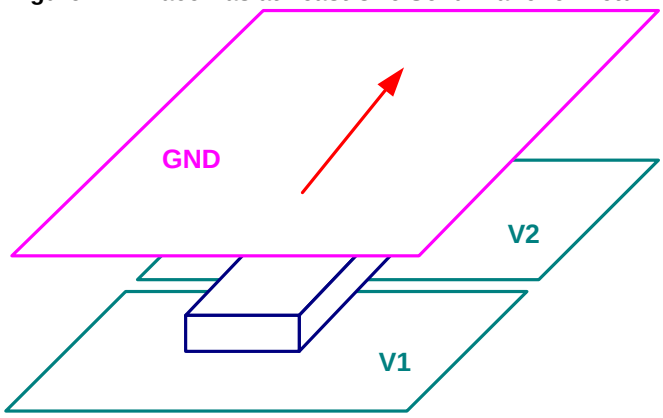
- Do not split ground planes.

  Keep good spacing between possible sensitive analog circuitry on your board and the digital signals to sufficiently isolate noise. A solid ground plane is necessary to provide a good return path for routing layers. Try to provide at least one ground plane adjacent to all routing layers (see Figure 4-2).

- Keep trace layers as close as possible to the adjacent ground or power planes.

  This helps minimize crosstalk and improve noise control on the planes.

Figure 4-2 Trace Has at Least One Solid Plane for Return Path



- When routing adjacent to only a power plane, do not cross splits.

  Route traces only over the power plane that supplies both the driver and the load. Otherwise, provide a decoupling capacitor near the trace at the end that is not supplied by the adjacent power plane.

- Critical signals must avoid running parallel and close to or directly over a gap.

  This would change the impedance of the trace.

- Separate analog powers onto opposing planes.

  This helps minimize the coupling area that an analog plane has with an adjacent digital plane.

- For dual strip-line routing, traces must only cross at 90 degrees.

  Avoid more than two routing layers in a row to minimize tandem crosstalk and to better control impedance.

- Planes must be evenly distributed in order to minimize warping.

- Calculating or modeling impedance must be made prior to routing.

  This helps ensure that a reasonable trace thickness is used and that the desired board thickness is available. Consult with your board fabricator for accurate impedance.

- Allow good separation between fast signals to avoid crosstalk.

  Crosstalk increases as the parallel traces get longer.

- When packages become smaller, route traces over a split power plane

  Smaller packages force vias to become smaller, thereby reducing board thickness and layer counts, which might create the need to route traces over a split power plane. Some alternatives to provide return path for these signals are listed below.

  Caution must be used when applying these techniques. Digital traces must not cross over analog planes, and vice-versa. All of these rules must be followed closely to prevent noise contamination problems that might arise due to routing over the wrong plane.

  By tightly controlling the return path, control noise on the power and ground planes can be controlled.

  - Place a ground layer close enough to the split power plane in order to couple enough to provide buried capacitance, such as SIG-PWR-GND (see Figure 4-3). Return signals that encounter splits in this situation simply jumps to the ground plane, over the split, and back to the other power plane. Buried capacitance provides the benefit of adding low inductance decoupling to your board. Your fabricator may charge for a special license fee and special materials. To determine the amount of capacitance your planes provide, use the following equation:

    $$C = 1.249 \bullet 10^{-13} \bullet E_r \bullet L \bullet W / H$$

    Where E_R is the dielectric coefficient, L • W represents the area of copper, and H is the separation between planes.
  - Provide return-path capacitors that connect to both power planes and jumps the split. Place them close to the traces so that there is one capacitor for every four or five traces. The capacitors would then provide the return path (see Figure 4-4).
  - Allow only static or slow signals on layers where they are adjacent to split planes.

Figure 4-3 shows the ground layer close to the split power plane.

Figure 4-3 Close Power and Ground Planes Provide Coupling for Good Return Path

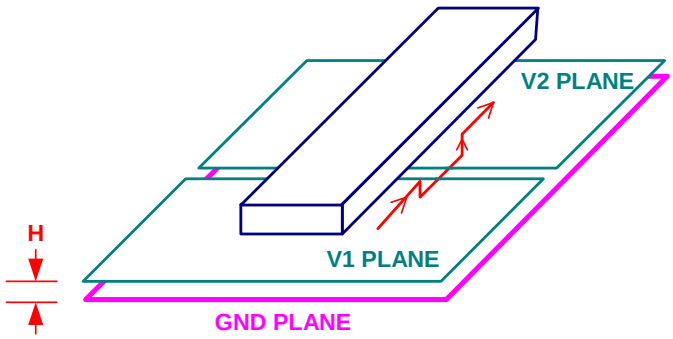
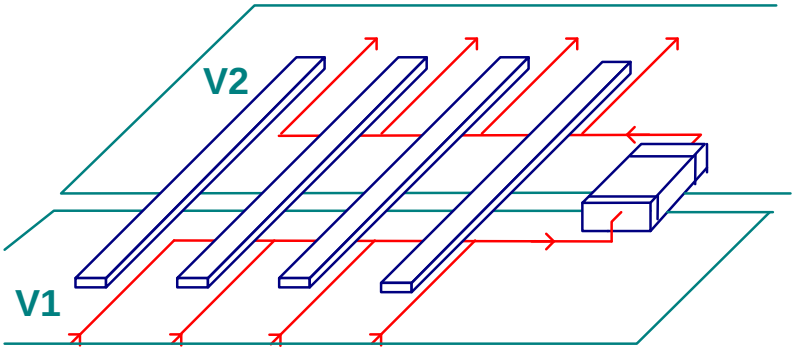


Figure 4-4 shows the thermal ground plane in relation to the return-path capacitor.

Figure 4-4 Suggested Thermal Ground Plane on Opposite Side of Chip



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5 GENERAL PURPOSE I/O PORT INTERFACE

This chapter contains the following sections:

5.1 Overview

The 88SM9602 contains a General Purpose Port Input/Output (GPIO) interface. The GPIO interface provides the following features:

- Each of the GPIO pins can be assigned to act as a general purpose input or output pin.
- A dedicated register provides the GPIO input value.
- A dedicated register provides the GPIO output value.
- Each of the GPIO outputs can be programmed for the LED to blink approximately every 100 ms.

5.2 GPIO Normal Mode

Table 5-1 describes the function of the GPIO pins

Table 5-1 GPIO Pin Default Functions

Pin Name	Default Setting	Default Function	Capable Function	Source	Description
GPIO0	PU	Host port link-up and activity LED.*	LED blink by register	Selectable	Multiple blink frequency
GPIO1	PU	Device 0 port link-up and activity LED.*	LED blink by register	Selectable	Multiple blink frequency
GPIO2	PU	Device 1 port link-up and activity LED.*	LED blink by register	Selectable	Multiple blink frequency
GPIO3	PU	General purpose I/O.	LED blink by register	Selectable	Multiple blink frequency
GPIO4	PU	General purpose I/O.	LED blink by register	Selectable	Multiple blink frequency
GPIO5	PU	General purpose I/O.	LED blink by register	Selectable	Multiple blink frequency
GPIO6	PU	General purpose I/O.	LED blink by register	Selectable	Multiple blink frequency
GPIO7	PU	General purpose I/O.	LED blink by register	Selectable	Multiple blink frequency
GPIO8	PU	General purpose I/O.	LED blink by register	Selectable	Multiple blink frequency
GPIO9	PD	General purpose I/O.	LED blink by register	Selectable	Multiple blink frequency

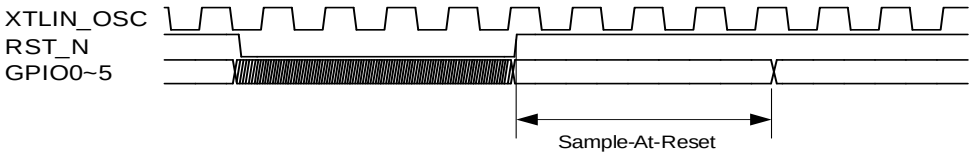
* The link-up and activity can be separated and selectable for the blink source.

5.3 GPIO Sample-at-Reset Pins

During chip reset, the method of using the GPIO pins to set the chip operation to the normal functional mode is called sample at reset. This method is activated when the RST_N input rises from low to high and is deactivated four reference cycles later. For example, if the reference cycle is 40 ns, the total time for deactivation is 4 x 40 ns = 160 ns.

Figure 5-1 shows the sample-at-reset timing.

Figure 5-1 Sample-at-Reset Timing



During sample at reset, the signal levels of the GPIO pins must be kept stable so the chip can reliably sample the values. After the sample at reset is deactivated, the GPIO pins can switch to other functions and the chip stops sampling GPIO pins. The sampled values are stored in the internal signals as shown in Table 5-2.

Table 5-2 Sample-at-Reset Signal Descriptions

Pin Name	Function
GPIO0	Reserved.
GPIO1	Reserved.
GPIO2	Reserved.
GPIO3	
GPIO4	PLL SSC Disable. **0h:** System PLL SSC is enabled. **1h:** The system PLL SSC is disabled.
GPIO5	8K FIFO Disable. **0h:** Device port 8K FIFO is enabled. **1h:** Device port 8K FIFO is disabled.
GPIO6	
GPIO7	.
GPIO8	.
GPIO9	

6 UART INTERFACE

This chapter contains the following sections:

6.1 UART Interface Overview

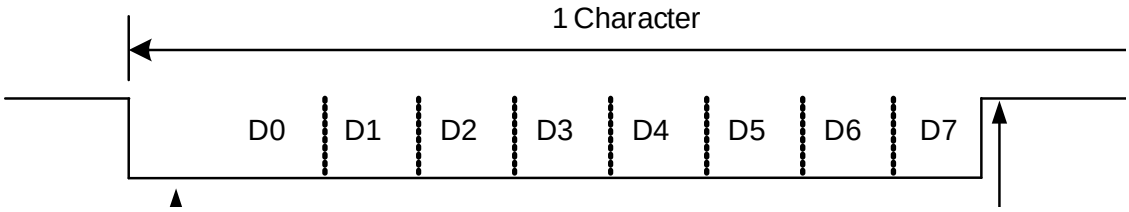
The 88SM9602 has one 115200 bps UART interface.

The UART interface is used to access internal registers, including those for the SATA status and SATA debug registers of each port. The UART interface is not required for normal operation. At the fixed baud rate of 115200 bps, the UART interface block is used mostly for debugging purposes. If the UART pins are not used, then all UAI pins must be left high for normal operation.

6.2 UART Interface Timing

Figure 6-1 illustrates an example of UART signal timing.

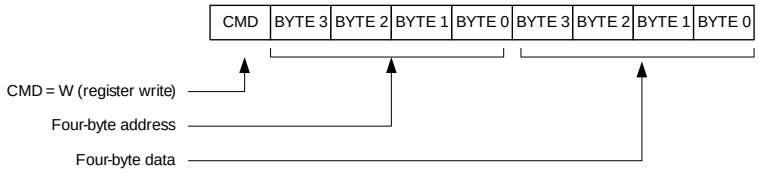
Figure 6-1 UART Signal Timing Example



6.3 Register Access Sequence Through UART

This section describes the register access sequence through the UART. Figure 6.2 shows the write command format.

Figure 6-2 Write Command Format

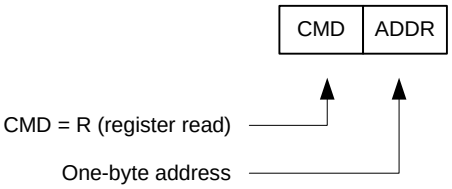


Following are the parameters of the write command format:

- A carriage return (CR) character and a line feed (LF) character are required after a WRITE command for command execution.
- A zero, a carriage return, and a line feed are returned if the command executes correctly.
- A question mark (“?”), a carriage return, and a line feed are returned if an error is encountered.

All alphabetic characters must be in upper case. The backspace character is not recognized. For example: W12AD34DF23 + CR + LF means write the value of AS34DF23h to the location R12h. If the UART returns 0 + CR + LF, then the command executed properly. If the UART returns ? + CR + LF, then the command did not execute properly. Figure 6.3 shows the read command format.

Figure 6-3 Read Command Format



Following are the parameters of the READ command format:

- The carriage return and line feed characters are required after a READ command.
- The register value, carriage return, and line feed characters are returned if the command executes correctly.
- A question mark (“?”), carriage return, and line feed characters are returned if an error is encountered.

All alphabetic characters must be in upper case. The backspace character is not recognized. For example, R12h + CR + LF means read from R12h. If the register value + CR + LF is returned, then the read command executed properly. If ? + CR + LF is returned from the UART, then the command did not execute properly.

6.3.1 UART Read/Write Command Sequences

Each UART sequence includes the parity bit in the last bit. Table 6-1 through Table 6-4, Write Command, Error detail the register Read/Write sequences for Read and Write commands, with and without errors.

Table 6-1 describes the registers read command sequence when no errors are returned.

Table 6-1 Read Command, No Error

Byte	Master	Slave	Value
1	CMD(R)	-	52h
2	ADDR[31:24]	-	ASCII (ADDR[31:28])
3			ASCII (ADDR[27:24])
4	ADDR[23:16]	-	ASCII (ADDR[23:20])
5			ASCII (ADDR[19:16])
6	ADDR[15:8]	-	ASCII (ADDR[15:12])
7			ASCII (ADDR[11:8])
8	ADDR[7:0]	-	ASCII (ADDR[7:4])
9			ASCII (ADDR[3:0])
10	CR	-	0Dh
11	LF	-	0Ah
12	-	DATA[31:24]	ASCII (DATA[31:28])
13			ASCII (DATA[27:24])
14	-	DATA[23:16]	ASCII (DATA[23:20])
15			ASCII (DATA[19:16])
16	-	DATA[15:8]	ASCII (DATA[15:12])
17			ASCII (DATA[11:8])
18	-	DATA[7:0]	ASCII (DATA[7:4])
19			ASCII (DATA[3:0])
20	-	CR	0Dh
21	-	LF	0Ah

Table 6-2 describes the registers read command sequence when errors are returned.

Table 6-2 Read Command, Error

Byte	Master	Slave	Value
1	CMD(R)	-	52h
2	ADDR[31:24]	-	ASCII (ADDR[31:28])
3			ASCII (ADDR[27:24])
4	ADDR[23:16]	-	ASCII (ADDR[23:20])
5			ASCII (ADDR[19:16])
6	ADDR[15:8]	-	ASCII (ADDR[15:12])
7			ASCII (ADDR[11:8])

Table 6-2 Read Command, Error (continued)

Byte	Master	Slave	Value
8	ADDR[7:0]	-	ASCII (ADDR[7:4])
9			ASCII (ADDR[3:0])
10	CR	-	0Dh
11	LF	-	0Ah
12		?	3Fh
13	-	CR	0Dh
14	-	LF	0Ah

Table 6-3 describes the registers write command sequence when no errors are returned.

Table 6-3 Write Command, No Error

Byte	Master	Slave	Value
1	CMD(W)	-	57h
2	ADDR[31:24]	-	ASCII (ADDR[31:28])
3			ASCII (ADDR[27:24])
4	ADDR[23:16]	-	ASCII (ADDR[23:20])
5			ASCII (ADDR[19:16])
6	ADDR[15:8]	-	ASCII (ADDR[15:12])
7			ASCII (ADDR[11:8])
8	ADDR[7:0]	-	ASCII (ADDR[7:4])
9			ASCII (ADDR[3:0])
10	DATA[31:24]	-	ASCII (DATA[31:28])
11			ASCII (DATA[27:24])
12	DATA[23:16]	-	ASCII (DATA[23:20])
13			ASCII (DATA[19:16])
14	DATA[15:8]	-	ASCII (DATA[15:12])
15			ASCII (DATA[11:8])
16	DATA[7:0]	-	ASCII (DATA[7:4])
17			ASCII (DATA[3:0])
18	CR	-	0Dh
19	LF	-	0Ah
20	-	0	30h
21	-	CR	0Dh
22	-	LF	0Ah

Table 6-4 describes the registers write command sequence when errors are returned.

Table 6-4 Write Command, Error

Byte	Master	Slave	Value
1	CMD(W)	-	57h
2	ADDR[31:24]	-	ASCII (ADDR[31:28])
3			ASCII (ADDR[27:24])
4	ADDR[23:16]	-	ASCII (ADDR[23:20])
5			ASCII (ADDR[19:16])
6	ADDR[15:8]	-	ASCII (ADDR[15:12])
7			ASCII (ADDR[11:8])
8	ADDR[7:0]	-	ASCII (ADDR[7:4])
9			ASCII (ADDR[3:0])
10	DATA3	-	ASCII (BYTE3 [7:4])
11			ASCII (BYTE3[3:0])
12	DATA2	-	ASCII (BYTE2 [7:4])
13			ASCII (BYTE2[3:0])
14	DATA1	-	ASCII (BYTE1 [7:4])
15			ASCII (BYTE1[3:0])
16	DATA0	-	ASCII (BYTE0 [7:4])
17			ASCII (BYTE0[3:0])
18	CR	-	0Dh
19	LF	-	0Ah
20	-	?	3Fh
21	-	CR	0Dh
22	-	LF	0Ah

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7 REGISTERS

This chapter contains the following sections:

7.1 Register Summary

This section contains the following subsections:

7.1.1 Register Access from SATA Host and UART

Registers can be accessed from either the SATA host or the UART.

7.1.1.1 Accessing from the SATA Host

All registers can be accessed from the SATA host by defining a port number and a register offset in the FIS. The combination of port number and offset is described in Table 7-1

Table 7-1 Access Registers from SATA Host

Port Number	Host/Device	Address Range	Register Description
F	Host	00h–7Fh	General Purpose Status and Control
F	Host	80h–FFh	Vendor Specific
F	Host	100h–1FFh	Host Port PHY Event
F	Host	200h–2FFh	Host Port
F	Host	300h–3FFh	GPIO
0	Device 0	00h–FFh	Device 0 Port
0	Device 0	100h–1FFh	Device 0 Port PHY Event
1	Device 1	00h–FFh	Device 1 Port
1	Device 1	100h–1FFh	Device 1 Port PHY Event
2	Device 2	00h–FFh	SEMB

Example: Port Multiplier Register Read

To read device port 1 register 01h, a port multiplier READ command (E4h) is issued to the port multiplier, as shown in Table 7-2.

Table 7-2 Port Multiplier Read Register

DWORD	[31:24]	[23:16]	[15:8]		[7:0]
DW0	Feature[7:0]	Command	C R R R	PM Port	FIS Type
	Reg address[7:0] = 01h	E4h	8	0	27h

Table 7-2 Port Multiplier Read Register (continued)

DWORD	[31:24]	[23:16]	[15:8]	[7:0]
DW1	Device	LBA[23:16]	LBA[15:8]	LBA[7:0]
	Port = F	Reserved	Reserved	Reserved
DW2	Feature[15:8]	LBA[47:40]	LBA[39:32]	LBA[31:24]
	Reg address[15:8] = 00h	Reserved	Reserved	Reserved
DW3	Control	ICC	Count[15:8]	Count[7:0]
	Reserved	Reserved	Port Num = 1	Reserved
DW4	Auxiliary[31:24]	Auxiliary[23:16]	Auxiliary[15:8]	Auxiliary[7:0]
	Reserved	Reserved	Reserved	Reserved

Note: FIS is the read Port Multiplier command.

Table 7-3 indicates that the port multiplier returns the read value of the specific register (04050000h).

Table 7-3 Port Multiplier Read Register Return

DWORD	[31:24]	[23:16]	[15:8]		[7:0]
DW0	Error	Status	R I R R	PM Port	FIS Type
	00h	50h	4	0	34h
DW1	Device	LBA[23:16]	LBA[15:8]		LBA[7:0]
	Reserved	Value[31:24] = 04h	Value[23:16] = 05h		Value[15:8] = 00h
DW2	Reserved	LBA[47:40]	LBA[39:32]		LBA[31:24]
	Reserved	Reserved	Reserved		Reserved
DW3	Reserved	Reserved	Count[15:8]		Count[7:0]
	Reserved	Reserved	Reserved		Value[7:0] = 00h
DW4	Reserved	Reserved	Reserved		Reserved
	Reserved	Reserved	Reserved		Reserved

Note: Register D2H FIS from Port Multiplier.

Example: Port Multiplier Register Write

To write to control port register 90h with a value of CAFE1F1Fh, a PM WRITE command (E8h) is issued to the PM as shown in Table 7-4.

Table 7-4 Port Multiplier Write Register

DWORD	[31:24]	[23:16]	[15:8]	[7:0]
DW0	Feature[7:0]	Command	C R R R PM Port	FIS Type
	Reg address[7:0] = 90h	E8h	8 F	27h
DW1	Device	LBA[23:16]	LBA[15:8]	LBA[7:0]
	Port = F	Value[31:24] = CAh	Value[23:16] = FEh	Value[15:8] = 1Fh
DW2	Feature[15:8]	LBA[47:40]	LBA[39:32]	LBA[31:24]
	Reg address[15:8] = 00h	Reserved	Reserved	Reserved
DW3	Control	ICC	Count[15:8]	Count[7:0]
	Reserved	Reserved	Port Num = F	Value[7:0] = 1Fh
DW4	Auxiliary[31:24]	Auxiliary[23:16]	Auxiliary[15:8]	Auxiliary[7:0]
	Reserved	Reserved	Reserved	Reserved

Note: FIS is the write Port Multiplier command.

7.1.1.2 Accessing from UART

All registers are accessed from the UART with a base address of R00020xxxh.

The following items show read and write examples of accessing a General Purpose register with offset 58h:

- Read—R00020058h
- Write—W00020058A5A5A5A5 (write A5A5A5A5 to register 58h).

Table 7-5 shows the address offset ranges and descriptions for register access from UART.

Table 7-5 Register Access from UART

Offset Range	Registers Description
R000h–R07Fh	General Status and Control
R080h–R0FFh	Vendor-Specific
R200h–R2FFh	Host Port
R300h–R3FFh	Host Port PHY Event
R400h–R4FFh	Device 0 Port
R500h–R5FFh	Device 0 Port PHY Event
R600h–R6FFh	Device 1 Port
R700h–R7FFh	Device 1 Port PHY Event
R800h–R8FFh	SEMB

7.1.2 General Status and Control Registers

Table 7-6 General Purpose Status and Control Register Summary

Register	Default Value	Register Description	Location
R000h	VVVV1B4Bh	Product Identifier	Page 7-10
R001h	0000A20Eh	Revision Information	Page 7-10
R002h	0000000Vh	Port Information	Page 7-11
R020h	00000000h	Error Information	Page 7-11
R021h	0400FFFFh	Error Information Bit Enable	Page 7-11
R022h	00000000h	PHY Event Counter Control	Page 7-12
R040h	0000001Fh	Port Multiplier Revision 1 X Features Support	Page 7-13
R060h	00000001h	Port Multiplier 1 X Feature Enable	Page 7-13

7.1.3 Vendor-Specific Port Multiplier Control Registers

Table 7-7 Vendor-Specific Port Multiplier Control Register Summary

Register	Default Value	Register Description	Location
R080h	00000000h	PM Control	Page 7-15
R081h	00000000h	Probe Control	Page 7-16
R082h	00000000h	Probe Signal	Page 7-16
R084h	00000000h	PM Lock Status	Page 7-16
R086h	00002C2Bh	SEMB I2C Control	Page 7-16
R087h	00900000h	SEMB Time-out Value	Page 7-17
R088h	0269362Eh	PLL Control 0 (200 MHz with 25 MHz REF_CLK)	Page 7-17
R089h	0000683Ch	PLL Control 1	Page 7-18
R08Ah	96048807h	PLL Control 2	Page 7-19
R092h	00000666h	Memory Control	Page 7-20
R093h	00000888h	SATA Port PHY Control	Page 7-20
R095h	090D01FFh	GPIO Sample-at-Reset Switch	Page 7-21
R096h	00000007h	Auto Partial-to-Slumber Global Control	Page 7-22
R0A0h	00000000h	Side Bank Address	Page 7-23
R0A1h	00000000h	Side Bank Data	Page 7-23

7.1.4 Host Port PHY Event Counter Registers

Table 7-8 Host Port PHY Event Counter Register Summary

Register	Default Value	Register Description	Location
R100h	00000000h	Host Port PHY Event Counter 1	Page 7-24

7.1.5 SATA PHY and Link Registers

This section includes the following sections:

- Link Registers
- SATA PHY—Low-Power SERDES PHY Registers

7.1.5.1 Link Registers

Table 7-9 Link Register Summary

Register Address	Default Value	Register Description	Location
R00Eh	00002001h	PHY Reserved Input Control	Page 7-24

7.1.5.2 SATA PHY—Low-Power SERDES PHY Registers

Table 7-10 SATA PHY—Low Power SERDES PHY Register Summary

Register Address	Default Value	Register Description	Location
R8Dh	C958h	Generation 1 Setting 0	Page 7-25
R8Fh	AA62h	Generation 2 Setting 0	Page 7-25
R91h	0BEBh	Generation 3 Setting 0	Page 7-26

7.1.6 Device Port PHY Event Counter Registers

Table 7-11 Device Port PHY Event Counter Register Summary

Register	Default Value	Register Description	Location
R100h	00000000h	Device Port PHY Event Counter 0	Page 7-28
R101h	00000000h	Device Port PHY Event Counter 2	Page 7-28

7.1.7 SEMB Port Status and Control Registers

Table 7-12 SEMB Port Status and Control Register Summary

Register	Default Value	Register Description	Location
R0000h	00000000h	S-Status	Page 7-28
R0001h	00000000h	S-Error	Page 7-29
R0002h	00000000h	S-Control	Page 7-29

7.2 Register Map Summary

Table 7-13 General Status and Control Register Map Summary

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R000h	DEV_ID																VENDOR_ID															
R001h	RSVD																PM_REV								RSVD				SPT_PM_12	SPT_PM_S1	SPPRT_PM_10	RSVD
R002h	RSVD																												PORT_NUM			

Table 7-13 General Status and Control Register Map Summary (continued)

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R020h	RSVD																											RSVD	RSVD	RSVD	P1_SEL_BIT_PSCR_OR	P0_SEL_BIT_PSCR_OR
R021h	ERR_INFO_BIT_EN																															
R022h	H_PORTH_GLBL_CNT_RST	RSVD										RSVD			RSVD		P1_CNT_RST	P0_CNT_RST	RSVD													PHY_EVENT_CNT_EN
R040h	RSVD																											SPT_PHY_CNT	SPT_NOTIFY	SPT_SSC	SPT_PMREQ	SPT_BIST
R060h	RSVD																												NOTIFY_EN	SSC_EN	PMREQP_EN	BIST_EN

Table 7-14 Vendor-Specific Port Multiplier Control Register Map Summary

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R080h	RSVD		RSVD		RSVD		RSVD		SEMB_MEMBIST_TEST_FAIL		SEMB_MEMBIST_TEST_FIN		PORT_1_MEMBIST_TEST_FAIL		PORT_1_MEMBIST_TEST_FIN		PORT_0_MEMBIST_TEST_FAIL		PORT_0_MEMBIST_TEST_FIN		PM_CTL_MEMBIST_TEST_FAIL		PM_CTL_MEMBIST_TEST_FIN		RSVD					NOP_COM_EN		ALL_DEV_EN		HOST_DEV_INV		I2C_SPEED_SEL
R081h	RSVD																				PROBE_MON_SEL				PROBE_MOD_SEL					PROBE_SIG_SEL			
R082h	RSVD																PROBE_SIG															
R084h	RSVD																											PM_LOCK_VALID	PM_LOCK_PORT_ID			
R086h	RSVD			SEMB_INTR	SEMB_WR	SEMB_ADDR			SEMB_RD_WR_DATA								RSVD	SEP_TWOWIRE_SERIAL_ADD							RSVD	SEMB_TWOWIRE_SERIAL_ADD						
R087h	RSVD								SEMB_TO_VAL																							
R088h	PLL_LOCK	PLL_CAP_SEL			RSVD	PLL_VCOFBST	PLL_VDDM		PLL_VDDL		PLL_INTPI_SEL		PLL_VCO_VRNG		PLL_VCODIV_SEL		PLL_KVCO				PLL_ICP			PLL_FBDIV								
R089h	RSVD	ANA_GROUP_TESTSEL			ANA_GROUP_GAINX2	ANA_GROUP_BYPASS	ANA_GROUP_BG_SEL		PLL_TEST_MON				PLL_SCC_RESET_EXT	PLL_SCC_FREQ_DIV															PLL_SSC_GAINX2	PLL_SSC_MODE	PLL_PU_SSC	PLL_SSC_EN
R08Ah	PU_PLL	RSVD	PLL_SSC_RNG						MOS_DRIVER																V25_EN	V18_EN	RSVD	RSVD	SEMB	SYS_CLK_EN	SATA_DEV_1_CLK_EN	SATA_DEV_0_CLK_EN
R092h	RSVD																				SEMB_1P_MEM_WTC		SEMB_1P_MEM_RTC		PORT_2P_MEM_WTC		PORT_2P_MEM_RTC		PM_CTL_2P_MEM_WTC		PM_CTL_2P_MEM_RTC	
R093h	RSVD								RSVD		RSVD		RSVD		RSVD		RSVD				PORT1_PU		PORT1_SPEED_SEL		PORT0_PU		PORT0_SPEED_SEL		HOST_PORT_PU		HOST_PORT_SPEED_SEL	

Table 7-14 Vendor-Specific Port Multiplier Control Register Map Summary (continued)

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R095h	RSVD	RSVD			RSVD	CMODE		REF_CLK_30	TST_PT_SEL			VDD_DSEL			LP_GAIN		RSVD	RSVD	I2C_HS_SEL	RSVD		I2C_HS_SEL_LTCH	GPIO_SAR_9	GPIO_SAR_8	GPIO_SAR_7	GPIO_SAR_6	GPIO_SAR_5	GPIO_SAR_4	GPIO_SAR_3	GPIO_SAR_2	GPIO_SAR_1	GPIO_SAR_0
R096h	RSVD																					HOST_AUTO_PART_TO_SLUMB_STAT	DEV1_AUTO_PART_TO_SLUMB_STAT	DEV0_AUTO_PART_TO_SLUMB_STAT	RSVD					AUTO_PART_TO_SLUMB_EN	DEV1_AUTO_PART_TO_SLUMB_IGN	DEV0_AUTO_PART_TO_SLUMB_IGN
R0A0h	SPI_MEM_ACCESS	RSVD			UNIT_SEL				MEM_ADD																							
R0A1h	SIDE_BANK_ACCESS																															

Table 7-15 Host Port PHY Event Counter Register Map Summary

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R100h	PHY_EVENT_CNT_1																															

Table 7-16 SATA PHY—Low-Power SERDES PHY Register Map Summary

Address	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R8Dh																	G1_TX_SLEW_CTRL_EN	G1_TX_SLEW_RATE_SEL			G1_TX_EMPH_EN	G1_TX_EMPH_AMP			RSVD	G1_TX_AMP						RSVD
R8Fh																	G2_TX_SLEW_CTRL_EN	G2_TX_SLEW_RATE_SEL			G2_TX_EMPH_EN	G2_TX_EMPH_AMP			RSVD	G2_TX_AMP						RSVD
R91h																	G3_TX_SLEW_CTRL_EN	G3_TX_SLEW_RATE_SEL			G3_TX_EMPH_EN	G3_TX_EMPH_AMP			RSVD	G3_TX_AMP						RSVD

Table 7-17 Device Port PHY Event Counter Register Map Summary

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R100h	DEV_PORT_PHY_EVENT_CNTR_0																															
R101h	DEV_PORT_PHY_EVENT_CNTR_2																															

Table 7-18 SEMB Port Status and Control Register Map Summary

Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R0000h	RSVD																												SEMB_PORT_STATE			
R0001h	RSVD					PORT_DI_EX	RSVD																									
R0002h	RSVD																												SEMB_CTL			

7.3 Register Description

This section contains the following subsections:

- General Status and Control Registers
- Vendor-Specific Port Multiplier Control Registers
- Host Port PHY Event Counter Registers
- SATA PHY and Link Registers
- Device Port PHY Event Counter Registers
- SEMB Port Status and Control Registers

7.3.1 General Status and Control Registers

R000h (VVVV1B4Bh) • Product Identifier

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	DEV_ID																VENDOR_ID															
Default Value	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	0	0	0	1	1	0	1	1	0	1	0	0	1	0	1	1

Bits	Field Name	Read/ Write	Default Value	Description
31:16	DEV_ID	R	VVVVh	Product Identifier. 9602h:Two-Port port multiplier
15:0	VENDOR_ID	R	1B4Bh	Vendor Identifier.

R001h (0000A20Eh) • Revision Information

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD																PM_REV								RSVD				SPT_PM_12	SPT_PM_S1	SPPRT_PM_10	RSVD
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0	0	0	0	0	1	1	1	0

Bits	Field Name	Read/ Write	Default Value	Description
31:16	RSVD	R	0000h	Reserved. Do not change the default value.
15:8	PM_REV	R	A2h	Port Multiplier Revision.
7:4	RSVD	R	0h	Reserved.
3	SPT_PM_12	R	1h	Support for Port Multiplier Specification 1.2.
2	SPT_PM_S1	R	1h	Support for Port Multiplier Specification 1.1.
1	SPPRT_PM_10	R	1h	Support for Port Multiplier Specification 1.0.
0	RSVD	R	0h	Reserved. Do not change the default value.

R002h (0000000Vh) • Port Information

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD																												PORT_NUM			
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	V	V	V	V

Bits	Field Name	Read/ Write	Default Value	Description
31:4	RSVD	R	0000000h	Reserved.
3:0	PORT_NUM	R	Vh	Number of Exposed Device Fan Out Ports. The default value is 3h if SEMB enabled and 2h if not enabled.

R020h (00000000h) • Error Information

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD																											RSVD	RSVD	RSVD	P1_SEL_BIT_PSCR_OR	P0_SEL_BIT_PSCR_OR
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field Name	Read/ Write	Default Value	Description
31:5	RSVD	R	0000000h	Reserved.
4	RSVD	R	0h	Reserved.
3	RSVD	R	0h	Reserved.
2	RSVD	R	0h	Reserved.
1	P1_SEL_BIT_PSCR_OR	R	0h	OR of Selectable Bits in Port 1 PSCR[1] (SError).
0	P0_SEL_BIT_PSCR_OR	R	0h	OR of Selectable Bits in Port 0 PSCR[1] (SError).

R021h (0400FFFFh) • Error Information Bit Enable

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	ERR_INFO_BIT_EN																															
Default Value	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bits	Field Name	Read/ Write	Default Value	Description
31:0	ERR_INFO_BIT_EN	R/W	0400FFFFh	Error Information Bit Enable. When this bit is enabled use Error Information (R020h).

R022h (00000000h) • PHY Event Counter Control

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	H_PORTH_GLBL_CNT_RST	RSVD										RSVD	RSVD	RSVD	P1_CNT_RST	P0_CNT_RST	RSVD															PHY_EVENT_CNT_EN
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field Name	Read/ Write	Default Value	Description
31	H_PORTH_GLBL_CNT_RST	R/W	0h	Host Port Global Counter Reset. **0h:** No action is taken **1h:** Immediately resets all PHY event counters associated with the device port. After the reset is complete, this bit is cleared to 0h.
30:21	RSVD	R	000h	Reserved. Do not change the default value.
20	RSVD	R/W	0h	Reserved. Do not change the default value.
19	RSVD	R/W	0h	Reserved. Do not change the default value.
18	RSVD	R/W	0h	Reserved. Do not change the default value.
17	P1_CNT_RST	R/W	0h	Port 1 Global Counter Reset. **0h:** No action is taken **1h:** Immediately resets all PHY event counters associated with the device port. After the reset is complete, this bit is cleared to 0h.
16	P0_CNT_RST	R/W	0h	Port 0 Global Counter Reset. **0h:** No action is taken **1h:** Immediately resets all PHY event counters associated with the device port. After the reset is complete, this bit is cleared to 0h.
15:1	RSVD	R/W	0000h	Reserved. Do not change the default value.
0	PHY_EVENT_CNT_EN	R/W	0h	PHY Event Counter Enabled. **0h:** All event counters stop counting and retain their current value. **1h:** Enable all PHY event counters.

R040h (0000001Fh) • Port Multiplier Revision 1 X Features Support

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD																											SPT_PHY_CNT	SPT_NOTIFY	SPT_SSC	SPT_PMREQ	SPT_BIST
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1

Bits	Field Name	Read/ Write	Default Value	Description
31:5	RSVD	R	0000000h	Reserved. Do not change the default value.
4	SPT_PHY_CNT	R	1h	Support PHY Event Counter. **0h:** Does not support PHY event counters **1h:** Supports PHY event counters
3	SPT_NOTIFY	R	1h	Support Asynchronous Notification. This bit toggles asynchronous set bit device (SDB) notification. **0h:** Does not support SDB notification **1h:** Supports SDB notification
2	SPT_SSC	R	1h	Support Dynamic SSC Transmit Enable. This bit toggles support for dynamic spread spectrum clock (SSC) transmission. **0h:** Does not support SSC transmit **1h:** Supports SSC transmit
1	SPT_PMREQ	R	1h	Support PMREQp. **0h:** Does not support issuing a PMREQp to the host. **1h:** Supports issuing a PMREQp to the host.
0	SPT_BIST	R	1h	Support BIST. **0h:** Does not support BIST **1h:** Supports BIST

R060h (00000001h) • Port Multiplier 1 X Feature Enable

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD																												NOTIFY_EN	SSC_EN	PMREQP_EN	BIST_EN
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Field Name	Read/ Write	Default Value	Description
31:4	RSVD	R	0000000h	Reserved. Do not change the default value.

Bits	Field Name	Read/ Write	Default Value	Description
3	NOTIFY_EN	R/W	0h	Asynchronous Notification Enable. This bit enables asynchronous set bit device (SDB) notification. **0h:** Disable **1h:** Enable
2	SSC_EN	R/W	0h	SSC Enable. This bit enables dynamic SSC transmitting. **0h:** Disable **1h:** Enable
1	PMREQP_EN	R/W	0h	PMREQ Enable. This bit enables the issuing of PMREQp to the host. **0h:** Disable **1h:** Enable
0	BIST_EN	R/W	1h	BIST Support Enable. **0h:** Disable **1h:** Enable

7.3.2 Vendor-Specific Port Multiplier Control Registers

R080h (00000000h) • PM Control

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD		RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	SEMB_MEMBIST_TEST_FAIL	SEMB_MEMBIST_TEST_FIN	PORT_1_MEMBIST_TEST_FAIL	PORT_1_MEMBIST_TEST_FIN	PORT_0_MEMBIST_TEST_FAIL	PORT_0_MEMBIST_TEST_FIN	PM_CTL_MEMBIST_TEST_FAIL	PM_CTL_MEMBIST_TEST_FIN	RSVD													NOP_COM_EN	ALL_DEV_EN	HOST_DEV_INV	I2C_SPEED_SEL
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field Name	Read/ Write	Default Value	Description
31:30	RSVD	R	0h	Reserved.
29	RSVD	R	0h	Reserved.
28	RSVD	R	0h	Reserved.
27	RSVD	R	0h	Reserved.
26	RSVD	R	0h	Reserved.
25	RSVD	R	0h	Reserved.
24	RSVD	R	0h	Reserved.
23	SEMB_MEMBIST_TEST_FAIL	R	0h	SEMB Memory BIST Test Fail.
22	SEMB_MEMBIST_TEST_FIN	R	0h	SEMB Memory BIST Test Finish.
21	PORT_1_MEMBIST_TEST_FAIL	R	0h	Port 1 Memory BIST Test Fail.
20	PORT_1_MEMBIST_TEST_FIN	R	0h	Port 1 Memory BIST Test Finish.
19	PORT_0_MEMBIST_TEST_FAIL	R	0h	Port 0 Memory BIST Test Fail.
18	PORT_0_MEMBIST_TEST_FIN	R	0h	Port 0 Memory BIST Test Finish.
17	PM_CTL_MEMBIST_TEST_FAIL	R	0h	PM CTL Memory BIST Test Fail.
16	PM_CTL_MEMBIST_TEST_FIN	R	0h	PM CTL Memory BIST Test Finish.
15:4	RSVD	R	000h	Reserved.
3	NOP_COM_EN	R	0h	NOP Command Enable.
2	ALL_DEV_EN	R	0h	All Devices Enable.
1	HOST_DEV_INV	R	0h	Host Device Inversion.
0	I2C_SPEED_SEL	R	0h	I2C Speed Select.

R081h (00000000h) • Probe Control

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD																				PROBE_MON_SEL				PROBE_MOD_SEL				PROBE_SIG_SEL			
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field Name	Read/ Write	Default Value	Description
31:12	RSVD	R	00000h	Reserved.
11:8	PROBE_MON_SEL	R/W	0h	Probe Monitor Select.
7:4	PROBE_MOD_SEL	R/W	0h	Probe Module Select.
3:0	PROBE_SIG_SEL	R/W	0h	Probe Signal Select.

R082h (00000000h) • Probe Signal

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD																PROBE_SIG															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field Name	Read/ Write	Default Value	Description
31:16	RSVD	R	0000h	Reserved.
15:0	PROBE_SIG	R	0000h	Probe Signal.

R084h (00000000h) • PM Lock Status

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD																											PM_LOCK_VALID	PM_LOCK_PORT_ID			
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field Name	Read/ Write	Default Value	Description
31:5	RSVD	R	0000000h	Reserved.
4	PM_LOCK_VALID	R	0h	PM Lock Valid. When this bit is set to 1, a port is in a locked state.
3:0	PM_LOCK_PORT_ID	R	0h	PM Lock Port ID.

R086h (00002C2Bh) • SEMB I2C Control

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD			SEMB_INTR	SEMB_WR	SEMB_ADDR			SEMB_RD_WR_DATA								RSVD	SEP_TWOWIRE_SERIAL_ADD							RSVD	SEMB_TWOWIRE_SERIAL_ADD						
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0	0	0	1	0	1	0	1	1

Bits	Field Name	Read/ Write	Default Value	Description
31:29	RSVD	R	0h	Reserved.

Bits	Field Name	Read/ Write	Default Value	Description
28	SEMB_INTR	R	0h	SEMB Interrupt. Refer to the Two-Wire Serial IP specification for more detail.
27	SEMB_WR	R/W	0h	SEMB Register Write. SEMB_WR, SEMB_ADDR, and SEMB_RD_WR_DATA signals provide an interface for the software to program the Two-Wire Serial register so that the software can control the interface of Two-Wire Serial. Refer to the Two-Wire Serial IP Specification for more detail.
26:24	SEMB_ADDR	R/W	0h	SEMB Register Address. Refer to the Two-Wire Serial IP Specification for more detail.
23:16	SEMB_RD_WR_DATA	R/W	00h	SEMB Read Write Data. Refer to the Two-Wire Serial IP Specification for more detail.
15	RSVD	R	0h	Reserved.
14:8	SEP_TWOWIRE_SERIAL_ADD	R/W	2Ch	SEP Two-Wire Serial Address.
7	RSVD	R	0h	Reserved.
6:0	SEMB_TWOWIRE_SERIAL_ADD	R/W	2Bh	SEMB Two-Wire Serial Address.

R087h (00900000h) • SEMB Time-out Value

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD								SEMB_TO_VAL																							
Default Value	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field Name	Read/ Write	Default Value	Description
31:24	RSVD	R	00h	Reserved. Do not change the default value.
23:0	SEMB_TO_VAL	R/W	900000h	SEMB Time-Out Value. SEMB time-out occurs when wait time larger than time-out value times cycle time.

R088h (0269362Eh) • PLL Control 0 (200 MHz with 25 MHz REF_CLK)

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	PLL_LOCK	PLL_CAP_SEL			RSVD	PLL_VCOFBST	PLL_VDDM		PLL_VDDL		PLL_INTPI_SEL		PLL_VCO_VRNG		PLL_VCODIV_SEL		PLL_KVCO				PLL_ICP			PLL_FBDIV								
Default Value	0	0	0	0	0	0	1	0	0	1	1	0	1	0	0	1	0	0	1	1	0	1	1	0	0	0	1	0	1	1	1	0

Bits	Field Name	Read/ Write	Default Value	Description
31	PLL_LOCK	R	0h	PLL Locked.
30:28	PLL_CAP_SEL	R/W	0h	PLL Cap Select.
27	RSVD	R/W	0h	Reserved.

Bits	Field Name	Read/ Write	Default Value	Description
26	PLL_VCOFBST	R/W	0h	PLL VCOFBST.
25:24	PLL_VDDM	R/W	2h	PLL VDDM.
23:22	PLL_VDDL	R/W	1h	PLL VDDL.
21:20	PLL_INTPI_SEL	R/W	2h	PLL INTPI SEL.
19:18	PLL_VCO_VRNG	R/W	2h	PLL VCO VRNG.
17:16	PLL_VCODIV_SEL	R/W	1h	PLL VCODIV Select.
15:12	PLL_KVCO	R/W	3h	PLL KVCO.
11:9	PLL_ICP	R/W	3h	PLL ICP.
8:0	PLL_FBDIV	R/W	02Eh	PLL FBDIV.

R089h (0000683Ch) • PLL Control 1

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD	ANA_GROUP_TESTSEL			ANA_GROUP_GAINX2	ANA_GROUP_BYPASS	ANA_GROUP_BG_SEL		PLL_TEST_MON				PLL_SCC_RESET_EXT	PLL_SCC_FREQ_DIV															PLL_SSC_GAINX2	PLL_SSC_MODE	PLL_PU_SSC	PLL_SSC_EN
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0	1	1	1	1	0	0

Bits	Field Name	Read/ Write	Default Value	Description
31	RSVD	R/W	0h	Reserved.
30:28	ANA_GROUP_TESTSEL	R/W	0h	Analog Group Test Select.
27	ANA_GROUP_GAINX2	R/W	0h	Analog Group Gain x2.
26	ANA_GROUP_BYPASS	R/W	0h	Analog Group Bypass.
25:24	ANA_GROUP_BG_SEL	R/W	0h	Analog Group BG_SEL.
23:20	PLL_TEST_MON	R/W	0h	PLL Test Monitor.
19	PLL_SCC_RESET_EXT	R/W	0h	PLL SCC Reset Extend.
18:4	PLL_SCC_FREQ_DIV	R/W	0683h	PLL SCC Frequency Divider.
3	PLL_SSC_GAINX2	R/W	1h	PLL SSC Gain x2.
2	PLL_SSC_MODE	R/W	1h	PLL SSC Mode.
1	PLL_PU_SSC	R/W	0h	PLL Power Up SSC.
0	PLL_SSC_EN	R/W	0h	PLL SSC Enable.

R08Ah (96048807h) • PLL Control 2

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	PU_PLL	RSVD	PLL_SSC_RNG														MOS_DRIVER								V25_EN	V18_EN	RSVD	RSVD	SEMB	SYS_CLK_EN	SATA_DEV_1_CLK_EN	SATA_DEV_0_CLK_EN
Default Value	1	0	0	1	0	1	1	0	0	0	0	0	0	1	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	1	1	1

Bits	Field Name	Read/ Write	Default Value	Description
31	PU_PLL	R/W	1h	Power-Up PLL (Asynchronous Reset).
30	RSVD	R/W	0h	Reserved.
29:16	PLL_SSC_RNG	R/W	1604h	PLL SSC Range.
15:8	MOS_DRIVER	R/W	88h	MOS Driver.
7	V25_EN	R/W	0h	2.5V Enable.
6	V18_EN	R/W	0h	1.8V Enable.
5	RSVD	R	0h	Reserved.
4	RSVD	R/W	0h	Reserved. Do not change the default value.
3	SEMB	R/W	0h	SEMB Clock Enable.
2	SYS_CLK_EN	R/W	1h	System Clock Enable.
1	SATA_DEV_1_CLK_EN	R/W	1h	SATA Device 1 Clock Enable.
0	SATA_DEV_0_CLK_EN	R/W	1h	SATA Device 0 Clock Enable.

R092h (00000666h) • Memory Control

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD																				SEMB_1P_MEM_WTC		SEMB_1P_MEM_RTC		PORT_2P_MEM_WTC		PORT_2P_MEM_RTC		PM_CTL_2P_MEM_WTC		PM_CTL_2P_MEM_RTC	
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	0	0	1	1	0

Bits	Field Name	Read/ Write	Default Value	Description
31:12	RSVD	R	00000h	Reserved.
11:10	SEMB_1P_MEM_WTC	R/W	1h	SEMB 1P Memory WTC.
9:8	SEMB_1P_MEM_RTC	R/W	2h	SEMB 1P Memory RTC.
7:6	PORT_2P_MEM_WTC	R/W	1h	Port 2P Memory WTC.
5:4	PORT_2P_MEM_RTC	R/W	2h	Port 2P Memory RTC.
3:2	PM_CTL_2P_MEM_WTC	R/W	1h	PM Control Port 2P Memory WTC.
1:0	PM_CTL_2P_MEM_RTC	R/W	2h	PM Control Port 2P Memory RTC.

R093h (00000888h) • SATA Port PHY Control

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD								RSVD	RSVD			RSVD	RSVD			RSVD	RSVD			PORT1_PU	PORT1_SPEED_SEL			PORT0_PU	PORT0_SPEED_SEL			HOST_PORT_PU	HOST_PORT_SPEED_SEL		
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0

Bits	Field Name	Read/ Write	Default Value	Description
31:24	RSVD	R	00h	Reserved.
23	RSVD	R	0h	Reserved.
22:20	RSVD	R	0h	Reserved.
19	RSVD	R	0h	Reserved.
18:16	RSVD	R	0h	Reserved.
15	RSVD	R	0h	Reserved.
14:12	RSVD	R	0h	Reserved.
11	PORT1_PU	R/W	1h	Port 1 Power Up.
10:8	PORT1_SPEED_SEL	R/W	0h	Port 1 Speed Select.
7	PORT0_PU	R/W	1h	Port 0 Power Up.
6:4	PORT0_SPEED_SEL	R/W	0h	Port 0 Speed Select.
3	HOST_PORT_PU	R/W	1h	Host Port Power Up.
2:0	HOST_PORT_SPEED_SEL	R/W	0h	Host Port Speed Select.

R095h (090D01FFh) • GPIO Sample-at-Reset Switch

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD	RSVD			RSVD	CMODE		REF_CLK_30	TST_PT_SEL			VDD_DSEL			LP_GAIN		RSVD	RSVD	I2C_HS_SEL	RSVD		I2C_HS_SEL_LTCH	GPIO_SAR_9	GPIO_SAR_8	GPIO_SAR_7	GPIO_SAR_6	GPIO_SAR_5	GPIO_SAR_4	GPIO_SAR_3	GPIO_SAR_2	GPIO_SAR_1	GPIO_SAR_0
Default Value	0	0	0	0	1	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1

Bits	Field Name	Read/ Write	Default Value	Description
31	RSVD	R	0h	Reserved.
30:28	RSVD	R	0h	Reserved.
27	RSVD	R	1h	Reserved.
26:25	CMODE	R	0h	CMODE[2:1] Bonding. **0h:** PM mode. **Others:**Reserved.
24	REF_CLK_30	R	0h	REFCLK 30 MHz. **0h:** 25 MHz REF Clock. **1h:** 30 MHz REF Clock.
23:21	TST_PT_SEL	R/W	0h	Test Point Select. Default no select.
20:18	VDD_DSEL	R/W	3h	VDD Select. Default is 1V.
17:16	LP_GAIN	R/W	1h	LP Gain.
15	RSVD	R/W	0h	Reserved. Do not change the default value.
14	RSVD	R/W	0h	Reserved. Do not change the default value.
13	I2C_HS_SEL	R/W	0h	I2C High-Speed Select.
12:11	RSVD	R	0h	Reserved.
10	I2C_HS_SEL_LTCH	W	0h	I2C High-Speed Select Latch.
9	GPIO_SAR_9	R/W	0h	GPIO Sample at Reset 9.
8	GPIO_SAR_8	R/W	1h	GPIO Sample at Reset 8.
7	GPIO_SAR_7	R/W	1h	GPIO Sample at Reset 7.
6	GPIO_SAR_6	R/W	1h	GPIO Sample at Reset 6.
5	GPIO_SAR_5	R/W	1h	GPIO Sample at Reset 5.
4	GPIO_SAR_4	R/W	1h	GPIO Sample at Reset 4.
3	GPIO_SAR_3	R/W	1h	GPIO Sample at Reset 3.
2	GPIO_SAR_2	R/W	1h	GPIO Sample at Reset 2.
1	GPIO_SAR_1	R/W	1h	GPIO Sample at Reset 1.
0	GPIO_SAR_0	R/W	1h	GPIO Sample at Reset 0.

R096h (00000007h) • Auto Partial-to-Slumber Global Control

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD																					HOST_AUTO_PART_TO_SLUMB_STAT	DEV1_AUTO_PART_TO_SLUMB_STAT	DEV0_AUTO_PART_TO_SLUMB_STAT	RSVD					AUTO_PART_TO_SLUMB_EN	DEV1_AUTO_PART_TO_SLUB_IGN	DEV0_AUTO_PART_TO_SLUB_IGN
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bits	Field Name	Read/ Write	Default Value	Description
31:11	RSVD	R	000000h	Reserved.
10	HOST_AUTO_PART_TO_SLUMB_STAT	R	0h	Host Port Auto Partial-to-Slumber Status.
9	DEV1_AUTO_PART_TO_SLUMB_STAT	R	0h	Device 1 Port Auto Partial-to-Slumber Status.
8	DEV0_AUTO_PART_TO_SLUMB_STAT	R	0h	Device 0 Port Auto Partial-to-Slumber Status.
7:3	RSVD	R	00h	Reserved. Do not change the default value.
2	AUTO_PART_TO_SLUMB_EN	R/W	1h	Auto Partial-to-Slumber Enable. **0h:** Disables auto Partial-to-Slumber for host port. **1h:** Host port enters slumber mode when the following conditions are met: • Auto Partial-to-Slumber for both device ports are enabled • The host port has entered partial mode • 10 ms has passed
1	DEV1_AUTO_PART_TO_SLUB_IGN	R/W	1h	Device 1 Auto Partial-to-Slumber Ignore. **0h:** Port 1 auto partial-to-slumber must be enabled by setting AUTO_PART_TO_SLUMB_EN. **1h:** Always enable Port 1 auto partial-to-slumber.
0	DEV0_AUTO_PART_TO_SLUB_IGN	R/W	1h	Device 0 Auto Partial-to-Slumber Ignore. **0h:** Port 0 auto partial-to-slumber must be enabled by setting AUTO_PART_TO_SLUMB_EN. **1h:** Always enable Port 0 auto partial-to-slumber.

R0A0h (00000000h) • Side Bank Address

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	SPI_MEM_ACCESS	RSVD			UNIT_SEL				MEM_ADD																							
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field Name	Read/ Write	Default Value	Description
31	SPI_MEM_ACCESS	R/W	0h	Memory Access for SPI. **0h:** Other register access **1h:** Read SPI memory.
30:28	RSVD	R/W	0h	Reserved.
27:24	UNIT_SEL	R/W	0h	Unit Select. **0h:** SPI controller register. **1h:** UART controller register.
23:0	MEM_ADD	R/W	000000h	Address for the Memory or Register.

R0A1h (00000000h) • Side Bank Data

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	SIDE_BANK_ACCESS																															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field Name	Read/ Write	Default Value	Description
31:0	SIDE_BANK_ACCESS	R/W	00000000h	Data Register of Side Bank Access.

7.3.3 Host Port PHY Event Counter Registers

R100h (00000000h) • Host Port PHY Event Counter 1

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	PHY_EVENT_CNT_1																															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field Name	Read/ Write	Default Value	Description
31:0	PHY_EVENT_CNT_1	R/W	00000000h	PHY Event Counter 1. This register contains both the counter identifier and the counter value: • Counter identifier: Read-only value 00002C01h. • Counter: 32-bit counter, contains number of signature D2H register FISes that were transmitted to the host from the control port.

7.3.4 SATA PHY and Link Registers

This section contains the following subsections:

- Link Registers
- SATA PHY—Low-Power SERDES PHY Registers

7.3.4.1 Link Registers

R00Eh (00002001h) • PHY Reserved Input Control

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD																						SSC_EN	TX_AMP_ADJ	RSVD							
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1

Bits	Name	Read/ Write	Default Value	Description
31:10	RSVD	R/W	000008h	Reserved. Do not change the default value.
9	SSC_EN	R/W	0h	Tx Spread Spectrum Enable. **0:** Disable. **1:** Enable.
8	TX_AMP_ADJ	R/W	0h	Transmitter Amplitude Adjust. For each reduction in range, additional power savings can be realized.
7:0	RSVD	R/W	01h	Reserved. Do not change the default value.

7.3.4.2 SATA PHY—Low-Power SERDES PHY Registers

R8Dh (C958h) • Generation 1 Setting 0

Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	G1_TX_SLEW_CTRL_EN	G1_TX_SLEW_RATE_SEL			G1_TX_EMPH_EN	G1_TX_EMPH_AMP				RSVD	G1_TX_AMP					RSVD
Default Value	1	1	0	0	1	0	0	1	0	1	0	1	1	0	0	0

Bits	Field Name	Read/ Write	Default Value	Description
15	G1_TX_SLEW_CTRL_EN	R/W	1h	Transmitter Slew Control Enable. This setting is used for 1.5 Gbps in SATA.
14:12	G1_TX_SLEW_RATE_SEL	R/W	4h	Transmitter Slew Rate Select. **000:** Fastest edge **111:** Slowest edge The difference between the slowest and the fastest setting is about 100 ps. This setting is used for 1.5 Gbps in SATA.
11	G1_TX_EMPH_EN	R/W	1h	Transmitter Emphasis Enable. This setting is used for 1.5 Gbps in SATA.
10:7	G1_TX_EMPH_AMP	R/W	2h	Transmitter Emphasis Amplitude. Approximately 4% per step at the package pin. **0h:** 4% **1h:** 8% ⋮ ⋮ **Ch:** 48% Settings Dh - Fh are not supported.
6	RSVD	R/W	1h	Reserved. Do not change the default value.
5:1	G1_TX_AMP	R/W	0Ch	Transmitter Amplitude. This setting is used for 1.5 Gbps in SATA.
0	RSVD	R/W	0h	Reserved. Do not change the default value.

R8Fh (AA62h) • Generation 2 Setting 0

Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	G2_TX_SLEW_CTRL_EN	G2_TX_SLEW_RATE_SEL			G2_TX_EMPH_EN	G2_TX_EMPH_AMP				RSVD	G2_TX_AMP					RSVD
Default Value	1	0	1	0	1	0	1	0	0	1	1	0	0	0	1	0

Bits	Field Name	Read/ Write	Default Value	Description
15	G2_TX_SLEW_CTRL_EN	R/W	1h	Transmitter Slew Control Enable. This setting is used for 3 Gbps in SATA.

Bits	Field Name	Read/ Write	Default Value	Description
14:12	G2_TX_SLEW_RATE_ SEL	R/W	2h	Transmitter Slew Rate Select. **000:** Fastest edge **111:** Slowest edge The difference between the slowest and the fastest setting is about 100 ps. This setting is used for 3 Gbps in SATA.
11	G2_TX_EMPH_EN	R/W	1h	Transmitter Emphasis Enable. This setting is used for 3 Gbps in SATA.
10:7	G2_TX_EMPH_AMP	R/W	4h	Transmitter Emphasis Amplitude. Approximately 4% per step at the package pin. **0h:** 4% **1h:** 8% ⋮ ⋮ **Ch:** 48% Settings Dh - Fh are not supported.
6	RSVD	R/W	1h	Reserved. Do not change the default value.
5:1	G2_TX_AMP	R/W	11h	Transmitter Amplitude. This setting is used for 3 Gbps in SATA.
0	RSVD	R/W	0h	Reserved. Do not change the default value.

R91h (0BEBh) • Generation 3 Setting 0

Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	G3_TX_SLEW_CTRL_EN	G3_TX_SLEW_RATE_SEL			G3_TX_EMPH_EN	G3_TX_EMPH_AMP				RSVD	G3_TX_AMP					RSVD
Default Value	0	0	0	0	1	0	1	1	1	1	1	0	1	0	1	1

Bits	Field Name	Read/ Write	Default Value	Description
15	G3_TX_SLEW_CTRL_ EN	R/W	0h	Transmitter Slew Control Enable. This setting is used for 6 Gbps in SATA.
14:12	G3_TX_SLEW_RATE_ SEL	R/W	0h	Transmitter Slew Rate Select. **000:** Fastest edge **111:** Slowest edge The difference between the slowest and the fastest setting is about 100 ps This setting is used for 6 Gbps in SATA.
11	G3_TX_EMPH_EN	R/W	1h	Transmitter Emphasis Enable. This setting is used for 6 Gbps in SATA.

Bits	Field Name	Read/ Write	Default Value	Description
10:7	G3_TX_EMPH_AMP	R/W	7h	Transmitter Emphasis Amplitude. Approximately 4% per step at the package pin. **0h:** 4% **1h:** 8% ⋮ ⋮ **Ch:** 48% Settings Dh - Fh are not supported.
6	RSVD	R/W	1h	Reserved. Do not change the default value.
5:1	G3_TX_AMP	R/W	15h	Transmitter Amplitude. This setting is used for 6 Gbps in SATA.
0	RSVD	R/W	1h	Reserved. Do not change the default value.

7.3.5 Device Port PHY Event Counter Registers

R100h (00000000h) • Device Port PHY Event Counter 0

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	DEV_PORT_PHY_EVENT_CNTR_0																															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field Name	Read/ Write	Default Value	Description
31:0	DEV_PORT_PHY_EVENT_CNTR_0	R/W	00000000h	Device Port PHY Event Counter 0. This register contains both the identifier and the counter value. Counter identifier: 00002C00h. Counter: 32-bit counter, contains number of transmitted H2D non-data FISes to which the port multiplier responded with R_ERR due to collision.

R101h (00000000h) • Device Port PHY Event Counter 2

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	DEV_PORT_PHY_EVENT_CNTR_2																															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field Name	Read/ Write	Default Value	Description
31:0	DEV_PORT_PHY_EVENT_CNTR_2	R/W	00000000h	Device Port PHY Event Counter 2. This register contains both the identifier and the counter value. Counter identifier: 00002C02h. Counter: 32-bit counter, contains number of corrupted CRC values that were transmitted to the host.

7.3.6 SEMB Port Status and Control Registers

R0000h (00000000h) • S-Status

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD																												SEMB_PORT_STATE			
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field Name	Read/ Write	Default Value	Description
31:4	RSVD	R	0000000h	Reserved.
3:0	SEMB_PORT_STATE	R	0h	SEMB Port State. **0h:** SEMB Port is disabled. **1h:** Reserved. **2h:** Reserved. **3h:** SEMB Port is enabled.

R0001h (00000000h) • S-Error

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD					PORT_DI_EX	RSVD																									
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field Name	Read/ Write	Default Value	Description
31:27	RSVD	R	00h	Reserved.
26	PORT_DI_EX	R	0h	Port Diagnostic Exchange. When this bit is set to 1, SEMB has been initialized since last time this bit was cleared.
25:0	RSVD	R	0000000h	Reserved.

R0002h (00000000h) • S-Control

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bits	RSVD																												SEMB_CTL			
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Field Name	Read/ Write	Default Value	Description
31:4	RSVD	R	0000000h	Reserved.
3:0	SEMB_CTL	R	0h	SEMB Control. **0h:** No device initialization action requested. **1h:** Perform SEMB initialization sequence. **2h:** Reserved. **3h:** Reserved. **4h:** SEMB port in offline mode.

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8 ELECTRICAL SPECIFICATIONS

This chapter contains the following sections:

Note: The absolute voltage, power, and temperature data provided in this chapter are estimated values.

8.1 Absolute Maximum Ratings

Table 8-1 describes the 88SM9602 absolute maximum ratings.

Table 8-1 Absolute Maximum Ratings

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Absolute Digital Power Supply Voltage	VDD_{ABS}		-0.5	1.0	1.1	V
Absolute Digital I/O pad Supply Voltage	$VDDIO_{ABS}$		-0.5	3.3	3.63	V
Absolute Analog Power Supply Voltage for TBG	$VAA1_{ABS}$		-0.5	1.8	1.98	V
Absolute Analog Power Supply Voltage for PHY	$VAA2_{ABS}$		-0.5	1.8	1.98	V
Absolute Input Voltage	Vin_{ABS}		-0.4		vddio + 0.4	V
Absolute Storage Temperature	$Tstor_{ABS}$		-55		+85	°C
Absolute Junction Temperature	$Tjunc_{ABS}$				125	°C

8.2 Power Requirements

Table 8-2 describes the 88SM9602 power requirements.

Table 8-2 Total Power Dissipation

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Absolute digital I/O pad power supply	I_{VDDIO}			5		mA
Absolute digital power supply	I_{VDD}			178		mA
Absolute analog power supply for TBG	I_{VAA1}			10		mA
Absolute analog power supply for PHY	I_{VAA2}			210		mA

8.3 Recommended/Typical Operating Conditions

Table 8-3 describes the 88SM9602 recommended/typical operating conditions.

Table 8-3 Recommended/Typical Operating Conditions

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Industrial Grade Operating Temperature			-40		85	°C
Ambient Operating Temperature			-10		70	°C
Junction Operating Temperature			0		125	°C
Operating Digital Power Supply Voltage	VDD_{OP}		1.0 - 5%	1.0	1.0 + 5%	V
Operating Digital I/O Pad Supply Voltage	$VDDIO_{OP}$		3.3 - 5%	3.3	3.3 + 5%	V
Operating Analog Power Supply Voltage for TBG	$VAA1_{OP}$		1.8 - 5%	1.8	1.8 + 5%	V
Operating Analog Power Supply Voltage for PHY	$VAA2_{OP}$		1.8 - 5%	1.8	1.8 + 5%	V

8.4 DC Characteristics

Table 8-4 describes the 88SM9602 DC Characteristics.

Table 8-4 DC Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Low Voltage	V_{IL}		-0.4		0.8	V
Input High Voltage	V_{IH}		2.0		VDDIO + 0.4	V
Output Low Voltage	V_{OL}	I_{OL}=4 mA, VDDP=3.3V	-0.4	0.13	0.4	V
Output High Voltage	V_{OH}	I_{OL}=-2 mA, VDDP=3.3V	2.4	3.3		V

8.5 Thermal Data

It is recommended to read application note AN-63 Thermal Management for Selected Marvell® Products and the ThetaJC, ThetaJA, and Temperature Calculations White Paper, available from Marvell, before designing a system. These documents describe the basic understanding of thermal management of integrated circuits (ICs) and guidelines to ensure optimal operating conditions for Marvell products.

Table 8-5 provides the thermal data for the 88SM9602. It shows the values for the package thermal parameters for the 48-lead Micro Quad Flat Non-Lead package (MQFN 48) mounted on a 4-layer PCB.The simulation was performed according to JEDEC standards.‘

Table 8-5 Package Thermal Data, 4-Layer PCB*

Parameter	Definition	Airflow Value			
		0 m/s	1 m/s	2 m/s	3 m/s
θ_{JA}	Thermal resistance: junction to ambient	42.9 C/W	37.9 C/W	35.9 C/W	–
θ_{JB}	Thermal resistance: junction to board	–	–	–	–
θ_{JC}	Thermal resistance: junction to case	21.3 C/W	–	–	–

* All data is based on parts mounted on a 4” x 4.5” JEDEC 4L PCB.

8.6 Thermal Data

It is recommended to read application note AN-63 Thermal Management for Selected Marvell® Products and the ThetaJC, ThetaJA, and Temperature Calculations White Paper, available from Marvell, before designing a system. These documents describe the basic understanding of thermal management of integrated circuits (ICs) and guidelines to ensure optimal operating conditions for Marvell products.

Table 8-6 provides the thermal data for the 88SM9602. It shows the values for the package thermal parameters for the 48-lead Micro Quad Flat Non-Lead package (MQFN 48) mounted on a 4-layer PCB.The simulation was performed according to JEDEC standards.‘

Table 8-6 Package Thermal Data, 4-Layer PCB*

Parameter	Definition	Airflow Value			
		0 m/s	1 m/s	2 m/s	3 m/s
θ_{JA}	Thermal resistance: junction to ambient	42.9 C/W	37.9 C/W	35.9 C/W	–
θ_{JB}	Thermal resistance: junction to board	–	–	–	–
θ_{JC}	Thermal resistance: junction to case	21.3 C/W	–	–	–

* All data is based on parts mounted on a 4” x 4.5” JEDEC 4L PCB.

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