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Product Brief

Structera™ S 20256 CXL Switch

256-lane CXL 2.0 switch

P/N: XC50256_3

Overview

The Marvell® Structera™ S 20256 (P/N XC50256_3) CXL switch is a CXL 2.0 switch device designed to enable memory pooling and composable infrastructure. The switch delivers ultra-low latency, high radix connectivity, and advanced fabric capabilities required for next-generation AI and HPC infrastructures.

Data centers are undergoing a fundamental architectural shift driven by AI/ML workloads, large language models, and memory-intensive computing. Traditional server architectures are constrained by fixed memory capacity and inefficient resource utilization, leading to the well-known memory wall bottleneck.

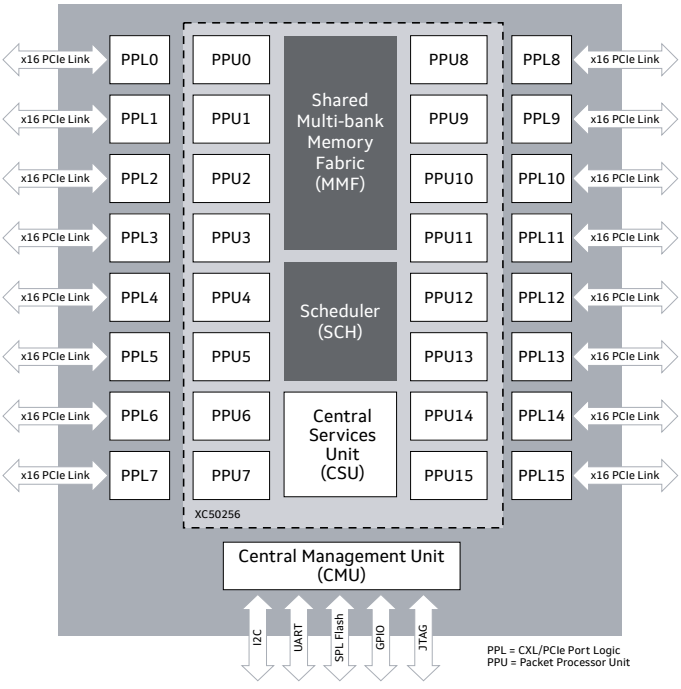
Compute Express Link (CXL) introduces a new paradigm—memory pooling and composable infrastructure—enabling dynamic scaling of memory resources across servers. This shift demands a new class of switching silicon optimized for low latency, high bandwidth, and memory-semantic traffic.

The Structera S 20256 device is industry's first CXL 2.0 switch, engineered from the ground up to address these challenges and integrating several key architectural building blocks:

- **CXL-native switching fabric:** optimized for CXL.mem and CXL.io traffic with ultra-low latency data paths.
- **High-radix, flexible port architecture:** configurable ports supporting x16 or x8 modes with dynamic upstream/downstream assignment.
- **Multi-level fabric scalability:** supports cascading to build large-scale memory fabrics.
- **Virtualized switching architecture:** enables multi-tenant and composable infrastructure.
- **Advanced traffic management:** virtual output queues (VOQ) eliminate head-of-line blocking and ensure deterministic performance.

The Structera S 20256 switch enables scalable CXL fabrics that significantly improve system performance, power efficiency, and total cost of ownership (TCO) by decoupling memory from compute.

Block Diagram



Key Features

Features	Details
Up to 2 TB/s switching capacity	• Enables high-bandwidth memory fabrics for AI/ML and HPC workloads
16 ports (x16) or 32 ports (x8)	• High radix enables scalable system topologies and reduced switch tiers
Full CXL 2.0 compliance (CXL.io, CXL.mem, CXL.cache)	• Ensures interoperability with CPUs, accelerators, and memory expanders
Support for CXL Type 2 and Type 3 devices	• Enables both accelerator coherency and memory expansion use cases
CXL fabric manager support	• Facilitates orchestration of composable memory infrastructure
CXL memory pooling and sharing, dynamic capacity allocation	• Enables fine-grained resource sharing and partitioning
Hot-plug and dynamic reconfiguration	• Improves system flexibility and serviceability
Memory and reliability	• ECC protection for memory paths • Data path parity protection • PCIe advanced error reporting (AER) • Downstream port containment (DPC)
Diagnostics and debug	• Built-in TLP packet generator • SerDes eye diagram capture • Traffic statistics and performance counters • External loopback capability
Power management	• Active state power management (ASPM) • Software-controlled power optimization
Interfaces	• PCIe and I2C management interfaces • SPI, UART, JTAG, GPIO support
Package and physical characteristics	• FCBGA package (65mm x 65mm) • High-density SerDes integration

Deployment Scenarios

- **AI/ML infrastructure:** Memory pooling for large model inference
- **Hyperscale data centers:** Composable infrastructure, resource disaggregation
- **High performance computing (HPC):** Large dataset processing, low-latency memory sharing
- **Enterprise systems:** Database acceleration, in-memory analytics

Software Support

- CXL 2.0 Fabric Manager compatibility
- Standard PCIe enumeration and configuration

Ordering Information

Part number: XC50256_3

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To deliver the data infrastructure technology that connects the world, we're building solutions on the most powerful foundation: our partnerships with our customers. Trusted by the world's leading technology companies for over 30 years, we move, store, process and secure the world's data with semiconductor solutions designed for our customers' current needs and future ambitions. Through a process of deep collaboration and transparency, we're ultimately changing the way tomorrow's enterprise, cloud and carrier architectures transform—for the better.

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