MARVELL

Product Brief

Structera™ S 50256 PCIe Switch

256-lane PCIe 5.0 switch

P/N: XC51256_3

Overview

The Marvell® Structera™ S 50256 (P/N XC51256_3) is a PCIe 5.0 switch device designed to enable AI infrastructure and fanout connectivity. The switch delivers ultra-low latency, high radix connectivity, and advanced fabric capabilities required for next-generation AI and HPC infrastructures.

Data centers are undergoing a fundamental architectural shift driven by AI/ML workloads, large language models, and memory-intensive computing. Traditional PCIe switches are constrained by the small lane counts available leading to the use of multiple switches causing higher latency and impacting performance of the AI systems.

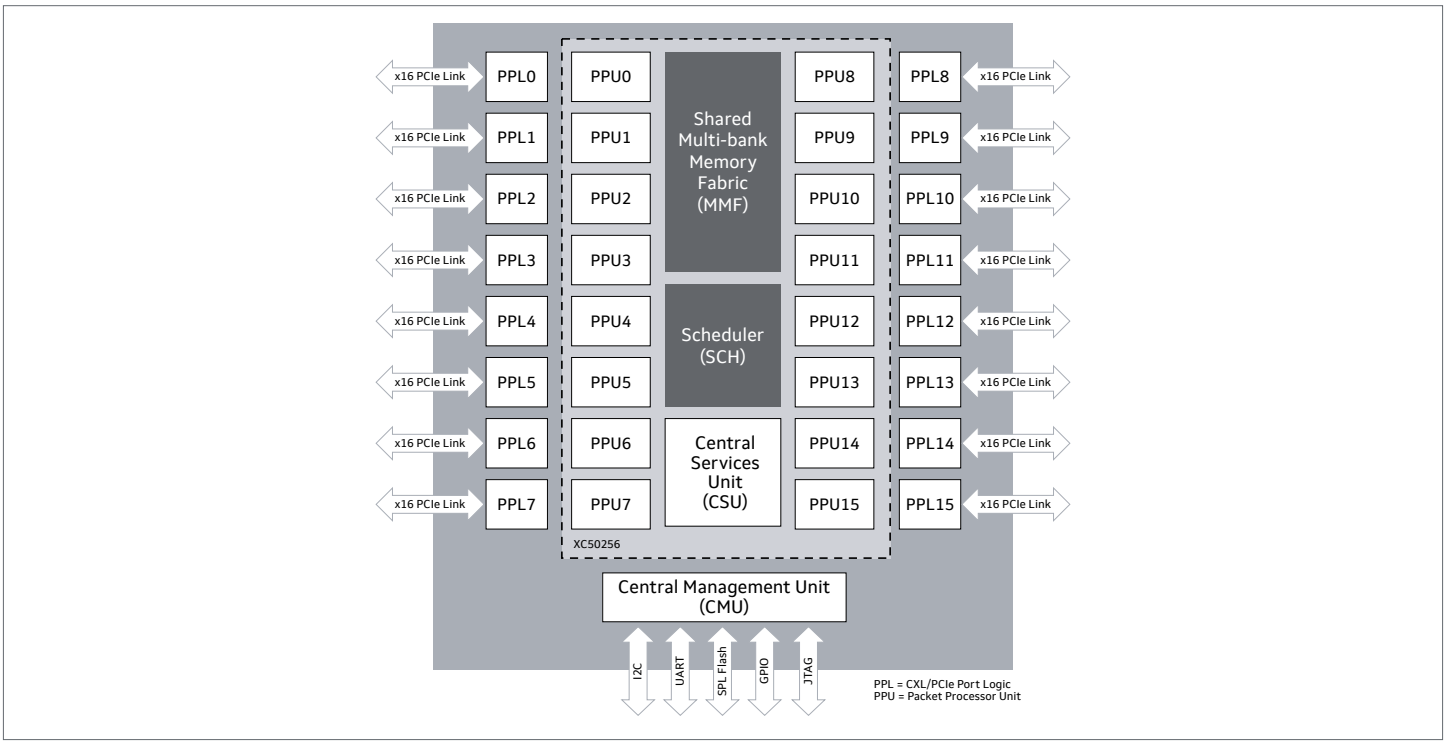
The Structera S 50256 device is industry's first PCIe 5.0 switch with 256 lanes, engineered from the ground up to address the latest data center connectivity challenges.

The Structera S 50256 switch features the following key building blocks:

- **High-radix, flexible port architecture:** configurable ports supporting x16 or x8 bifurcation with dynamic upstream/downstream assignment.
- **Multi-level fabric scalability:** supports cascading to build large-scale fabrics.
- **Virtualized switching architecture:** enables multi-tenant and composable infrastructure.
- **Advanced traffic management:** virtual output queues (VOQ) eliminate head-of-line blocking and ensure deterministic performance.

The Structera S 50256 switch enables low-latency, high-performance AI systems by enabling connections to several CPUs, GPUs, NICs and SSDs, which significantly improves system performance, power efficiency, and total cost of ownership (TCO).

Block Diagram



Key Features

Features	Details
Up to 2 TB/s switching capacity	• Enables high-bandwidth interconnection with low-latency for AI/ML and HPC workloads
16 ports (x16) or 32 ports (x8)	• High radix enables scalable system topologies and reduced switch tiers
PCIe 5.0 compliance (listed on PCISIG compliance website)	• Ensures interoperability with a large number of PCIe devices including CPUs, GPUs, NICs, SSDs and many more devices
Hot-plug and dynamic reconfiguration	• Improves system flexibility and serviceability
Memory and reliability	• ECC protection for memory paths • Data path parity protection • PCIe advanced error reporting (AER)
Diagnostics and debug	• Built-in TLP packet generator • SerDes eye diagram capture • Traffic statistics and performance counters • External loopback capability
Power management	• Active state power management (ASPM) Software-controlled power optimization
Interfaces	• PCIe and I2C management interfaces • SPI, UART, JTAG, GPIO support
Package and physical characteristics	• FCBGA package (65mm x 65mm) • High-density SerDes integration

Deployment Scenarios

- **AI/ML infrastructure:** low latency interconnection for connecting multiple CPUs, GPUs, NICs and SSDs
- **Hyperscale data centers:** composable infrastructure, resource disaggregation
- **High performance computing (HPC):** large dataset processing, low-latency performance

Software Support

- Standard PCIe enumeration and configuration

Ordering Information

Part number: XC51256_3

MARVELL

To deliver the data infrastructure technology that connects the world, we're building solutions on the most powerful foundation: our partnerships with our customers. Trusted by the world's leading technology companies for over 30 years, we move, store, process and secure the world's data with semiconductor solutions designed for our customers' current needs and future ambitions. Through a process of deep collaboration and transparency, we're ultimately changing the way tomorrow's enterprise, cloud and carrier architectures transform—for the better.

Marvell_Structera_S 50256 _PB Revised: 06/26