Marvell® Alaska® X 88X2222M and 88X2242M

Integrated Dual-port and Quad-port Multi-speed Ethernet Transceiver with MACSec and Electronic Dispersion Compensation Technology

Product Overview

The Marvell® Alaska® X 88X2222M and 88X2242M transceiver family is a fully integrated single-chip solution providing end-to-end data transmission over fiber-optic networks as well as Twinax copper links. It offers 2- or 4-port devices that perform all physical layer functions associated with 10GBASE-R, 2000BASE-X, 1000BASE-X and 10GBASE-W. In addition, the device supports one port of 10GBASE-X4, 40GBASE-R4 and 10GBASE-X2.

The electronic dispersion compensation (EDC) engine delivers high-speed bidirectional point-to-point full duplex data transmission at 10.3 Gbps per port over a variety of media. The performance of the engine can be reduced to save power in fiber-optic applications that do not require EDC.

The host-side interface supports two or four ports of 10GBASE-R, 10GBASE-X2, 2000BASE-X or 1000BASE-X with two ports of 40GBASE-R4 or 10GBASE-X4, and one port of 40GBASE-R8.

Any port from the host side can be attached to any port on the line side as long as the speeds match. The device outputs a recovered clock for use in synchronous Ethernet applications.

The 88X2242M supports the Marvell LinkCrypt® feature, which is based on the IEEE802.1ae MACSec protocol. The 88X2242M device also supports the features above those required by the IEEE802.1ae MACSec protocol. These include the ability to select and filter uncontrolled port traffic; support of packet redirection by addition of a new MAC DA, SA and Ethertype; support of latency minimization for flow control packets; and support for diagnostics, MACSec header retention and additional statistics counters. The device also supports the ability to select a secure channel by means other than the SCI, FIPS compliance testing, adaptive rate control to compensate for packet expansion and Ethertype matching for the uncontrolled path.

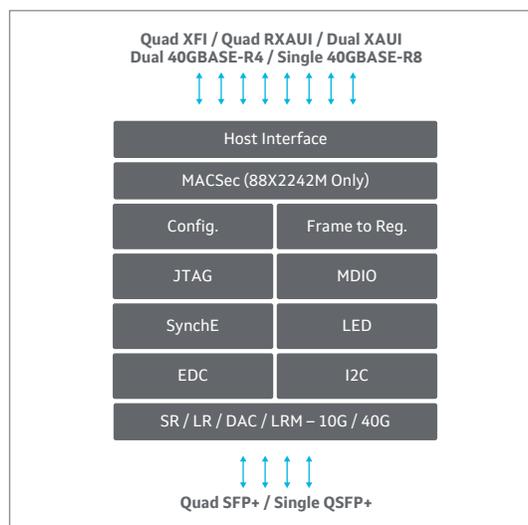| PART NUMBER	DESCRIPTION
88X2222	• 2-port
88X2222M	• 2-port with MACSec
88X2242	• 4-port
88X2242M	• 4-port with MACSec

Fig 1. 88X2242M System Block Diagram

Key Features

- 40GBASE-R4, 10GBASE-W, 10GBASE-R, 10GBASE-X2, 10GBASE-X4, 2000BASE-X, 1000BASE-X support on the line interface
- EDC meets SFF-8431 requirements (SFP+MSA)
- MMF compensation exceeding 220 m of OM1, OM2, OM3 fibers
- Twinax compensation up to 15 m
- SMF CD/PMD compensation exceeding 80 km
- 40GBASE-R4, 40GBASE-R8, 10GBASE-R, 10GBASE-X2, 10GBASE-X4, 2000BASE-X, 1000BASE-X supports on the host interface
- Transmitter adjustable signal level and pre-emphasis
- Re-timer mode supported for transparent data passing
- Synchronous Ethernet support
- MACSec function – Full 802.1ae compliance supporting default cipher suite GCM-AES-128
- MACSec features include encryption, decryption authentication, MACSec tag insertion and removal and bypass capability
- Integral FIFOs to absorb MACSec processing overhead which can operate in both cut-through and store-forward modes
- Integral MACs ensure IEEE-compliant statistics collection and timely response to pause frames
- Complete IEEE MAC and MACSec statistics collected for all ports
- IEEE 802.3 local/remote fault monitoring at SFP/SFP+ interface
- Built-in generators and checkers
- ECC memory protection
- Programmable inversion on all differential signals
- Power-saving modes
- Global multi-status interrupt pin
- MDIO/MDC and frame to register access
- Per-port in-band frame to register access
- Near- and far-end loopbacks
- Ingress and egress eye monitors
- Supports IEEE-1149.1 and 1149.6 JTAG
- Typical power – 1.5 W per port
- 19mm x 19mm FCBGA package

Target Applications

- High-density line card SFP+ interfacing
- SFP+ modules, 10GSFP+Cu direct attach cables
- 1G SFP modules
- Re-timer
- Switch to switch bridging