

Marvell Alaska X 88X2222P and 88X2242P

Integrated Dual-port and Quad-port Multi-speed Ethernet Transceiver with MACSec, IEEE 1588 PTP, Electronic Dispersion Compensation Technology and TurboBoost Backplane Technology

PRODUCT OVERVIEW

The Marvell® 88X2242P transceiver is a fully integrated, single chip solution providing end-to-end data transmission over fiber-optic networks as well as Twinax copper links which support SFF-8431 requirements. It is a 4-port device that performs all physical layer functions associated with 10GBASE-R, 2500BASE-X, 1000BASE-X and 10GBASE-W.

The Electronic Dispersion Compensation (EDC) engine exceeds the requirements of IEEE 10GBase-LRM to deliver high-speed bi-directional point-to-point full duplex data transmission at 10Gbps per port over a legacy multimode fiber. The host side interface supports 8 ports of 10GBASE-KR, 2500BASE-KX, 1000BASE-KX, 4 ports of RXAUI, or 2 ports of XAUI. The redundant host interfaces can be multiplexed onto the line interface for applications requiring redundancy.

All host interfaces have TurboBoost KR DSP engine performance that exceeds conventional DFE architectures, enabling 10Gbps transmission over legacy backplanes.

The device outputs two recovered clocks for use in Synchronous Ethernet applications and supports Precise Timing Protocol (PTP) Time Stamping based on IEEE1588 v2 and IEEE802.1AS.

The 88X2242P supports the Marvell LinkCrypt® feature, which is based on the IEEE802.1ae MACsec protocol. The 88X2242P device also supports features required by the IEEE802.1ae MACsec protocol. These include the ability to select and filter Uncontrolled Port traffic, support of Packet redirection by addition of a new MAC DA, SA and Ethertype, support of latency minimization for flow control packets, and support for diagnostics, MACsec header retention, and additional statistics counters. The device also supports the ability to select a Secure Channel by means other than the SCI, FIPS compliance testing, adaptive rate control to compensate for packet expansion, and Ethertype matching for the uncontrolled path.

PART NUMBER

DESCRIPTION

| | |
|----------|---|
| 88X2222P | • 2-PORT WITH MACSec, PTP, EDC and TurboBoost |
| 88X2242P | • 4-PORT WITH MACSec, PTP, EDC and TurboBoost |

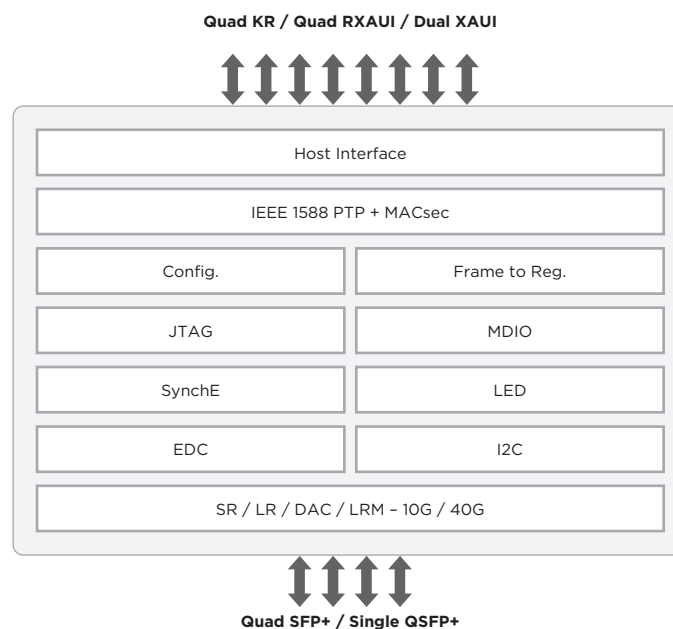


Fig 1. 88X2242P System Block Diagram

KEY FEATURES

- 10GBASE-W, 10GBASE-R, 10GBASE-X2, 2500BASE-X, 1000BASE-X support on the line interface
- EDC meets SFF-8431 requirements (SFP+MSA)
- MMF compensation exceeding 220 m of OM1, OM2, OM3 fibers
- Twinax compensation exceeding requirements of SFF-8431 Annex E
- SMF CD/PMD compensation exceeding 80 km
- 10GBASE-KR, RXAUI, XAUI, 2500BASE-X and 1000BASE-X support on the host interface
- Fully redundant host interface
- TurboBoost DSP engine on all host receivers
- Transmitter adjustable signal level and pre-emphasis
- Synchronous Ethernet support
- IEEE 1588 v2 1-step and 2-step PTP time stamping
- Fully 802.1ae compliant MACsec with GCM-AES-128 cipher suite
- MACSec features include encryption, decryption authentication, MACSec tag insertion and removal and bypass capability
- Integral FIFOs to absorb MACSec processing overhead which can operate in both cut-through and store-forward modes
- Integral MACs ensure IEEE-compliant statistics collection and timely response to pause frames
- Complete IEEE MAC and MACSec statistics collected for all ports
- IEEE 802.3 local/remote fault monitoring at SFP/SFP+ interface
- Built-in generators and checkers
- ECC memory protection
- Programmable inversion on all differential signals
- Power-saving modes
- Global multi-status interrupt pin
- MDIO/MDC and frame to register access
- Per-port in-band frame to register access
- Near- and far-end loopbacks
- Supports IEEE-1149.1 and 1149.6 JTAG
- Typical power - 2.0 W per port
- 19mm x 19mm FCBGA package

APPLICATIONS

- High-density line card SFP+ interfacing
- SFP+ modules, 10GSFP+Cu direct attach cables
- 1G SFP modules
- 10GBase-KR backplane applications
- Switch to switch bridging

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