88SE1475

PCIe 3.0 x8 to 16-Port 6 Gbps SATA I/O Controller

Datasheet

Doc No. MV-S110697-U0 Rev. A

June 20, 2018

Document Classification: Public

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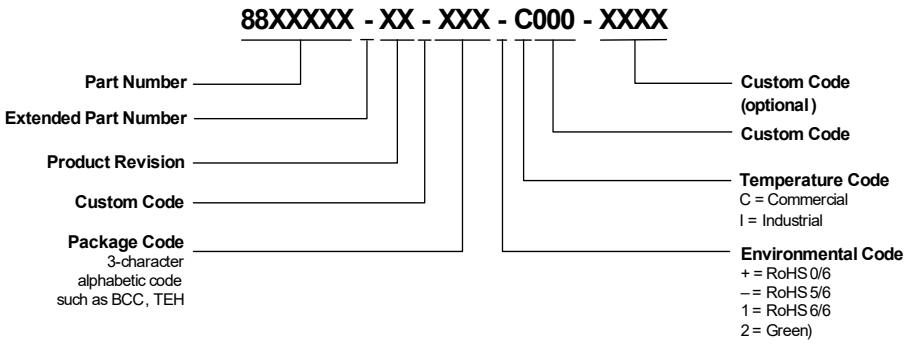
ORDERING INFORMATION

Ordering Part Numbers and Package Markings

The following figure shows the ordering part numbering scheme for the 88SE1475 part. For complete ordering information, contact your Marvell FAE or sales representative.

Sample Ordering Part Number



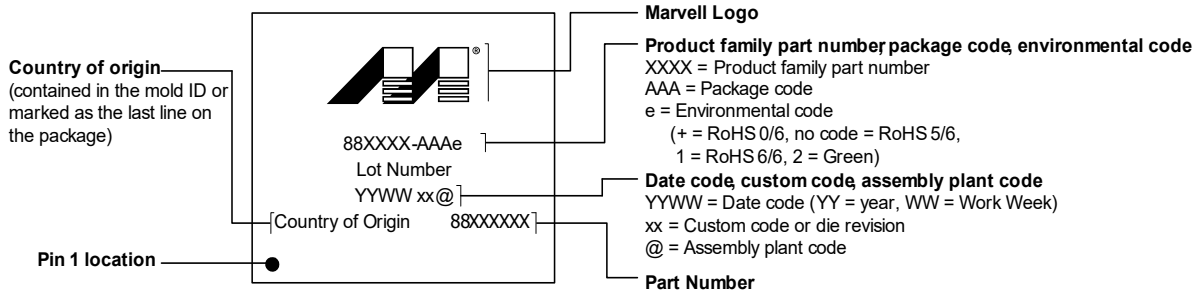
The standard ordering part numbers for the respective solutions are indicated in the following table.

Ordering Part Numbers

Part Number	Description
88SE1475A1-BSS2C000-A189	625-Ball HFCBGA 21 × 21 mm.

The next figure shows a typical Marvell package marking.

88SE1475 Package Marking and Pin 1 Location



Note: The above drawing is not drawn to scale. The location of markings is approximate. Add-on marks are not represented. Flip chips vary widely in their markings and flip chip examples are not shown here. For flip chips, the markings may be omitted per customer requirement.

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CHANGE HISTORY

The following table identifies the document change history for Rev. A.

Document Changes *

Location	Type	Description	Date
Global	Update	Removed “preliminary” designation from titles and page headers.	May 21, 2018
Page 4-6	Update	Updated Figure 4-3, PCB Layer Stack-Up.	May 23, 2018
page 4-1	Update	Updated 4.5, SATA Routing	June 20, 2018

* The type of change is categorized as: Parameter, Revision, or Update. A Parameter change is a change to a spec value, a Revision change is one that originates from the chip Revision Notice, and an Update change includes all other document updates.

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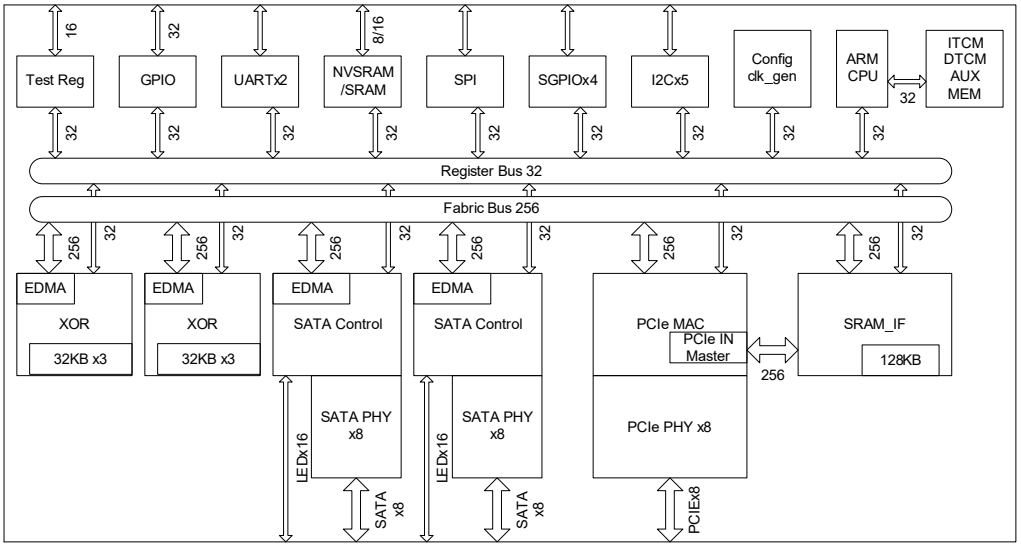
CONTENTS

1 OVERVIEW

The 88SE1475 is a 16-port, 6 Gbps SATA controller that contains an eight-lane PCIe 3.0 interface.

The 88SE1475 integrates 16 high-performance SATA PHYs capable of 1.5 Gbps, 3.0 Gbps, 6.0 Gbps SATA link rates. The controller supports the SATA protocol defined in the Serial ATA Revision 3.0 Specification. Figure 1-1 shows the 88SE1475system architecture.

Figure 1-1 88SE1475 System Architecture



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2 FEATURES

This chapter contains the following sections:

2.1 General

The 88SE1475 supports the following features:

- 16 SATA ports.
- Eight-lane PCIe 3.0 host interface.
- Supports five Serial Device Bus (I2C) controllers for communicating with hardware monitoring ICs.
- Supports two industry standard 57600 UART.
- Supports four SFF-8485-compliant SGPIO ports.
- Supports auto-detection of native SATA device.
- Up to 8192 concurrent I/O operations (2048 I/O Context on-chip).
- Up to 128 concurrent SATA devices.
- Advanced CMOS process.
- 9 W estimated power
- Unique pin outs of 34 LEDs and 32 GPIO.
- All data paths and internal memories are parity-protected.
- The 88SE1475 supports up to 16 MB of external NVSRAM memory (x8/ x16).

2.2 PCIe

The 88SE1475 supports the following PCIe features:

- Primary PCIe interface supports x1, x4, and x8 lane PCIe 3.0 at 8 Gbps.
- Supports independent communication, message, and interrupt mechanisms.
- Supports MSI/MSI-X interrupts.
- Supports PCIe power management for D0, D1, D3COLD, and D3HOT.
- Supports legacy interrupts.
- All registers are memory-mapped.

2.3 SATA

The 88SE1475 supports the following SATA features:

- SATA 3.0 (6 Gbps) compliant, with speed negotiation to 6.0 Gbps, 3.0 Gbps, and 1.5 Gbps.
- Supports programmable SATA signaling levels, including Gen1x, Gen2i, Gen2x, Gen3, and Gen3i.
- Supports ATA and ATAPI commands.
- Supports Native Command Queuing (NCQ).
  - Non-0 offset and non-sequential data delivery.
  - 32 outstanding commands per device.
- Supports Port Multiplier—FIS-based Switching on NCQ and legacy commands.
- Supports Host mode and Device mode of operation.

2.4 XOR Engine

The 88SE1475 supports the following XOR features:

- Generates up to three checksums concurrently, including any combination of P and Q.
- Independent GF Multiply coefficient for each of three concurrent Q checksum calculations.
- Supports rebuilding up to three failed drives simultaneously with a single read of remaining good drives.
- Supports chained XOR Descriptor Tables, with up to 32 operations in each Table.
- Supports Scatter-Gather transfers using a common PRD format.
- Supports T10 Protection Information Model. DIF fields can be inserted, checked, replaced, and/or removed before or after XOR operation.
- Supports CRC32 checksum generation and checking.

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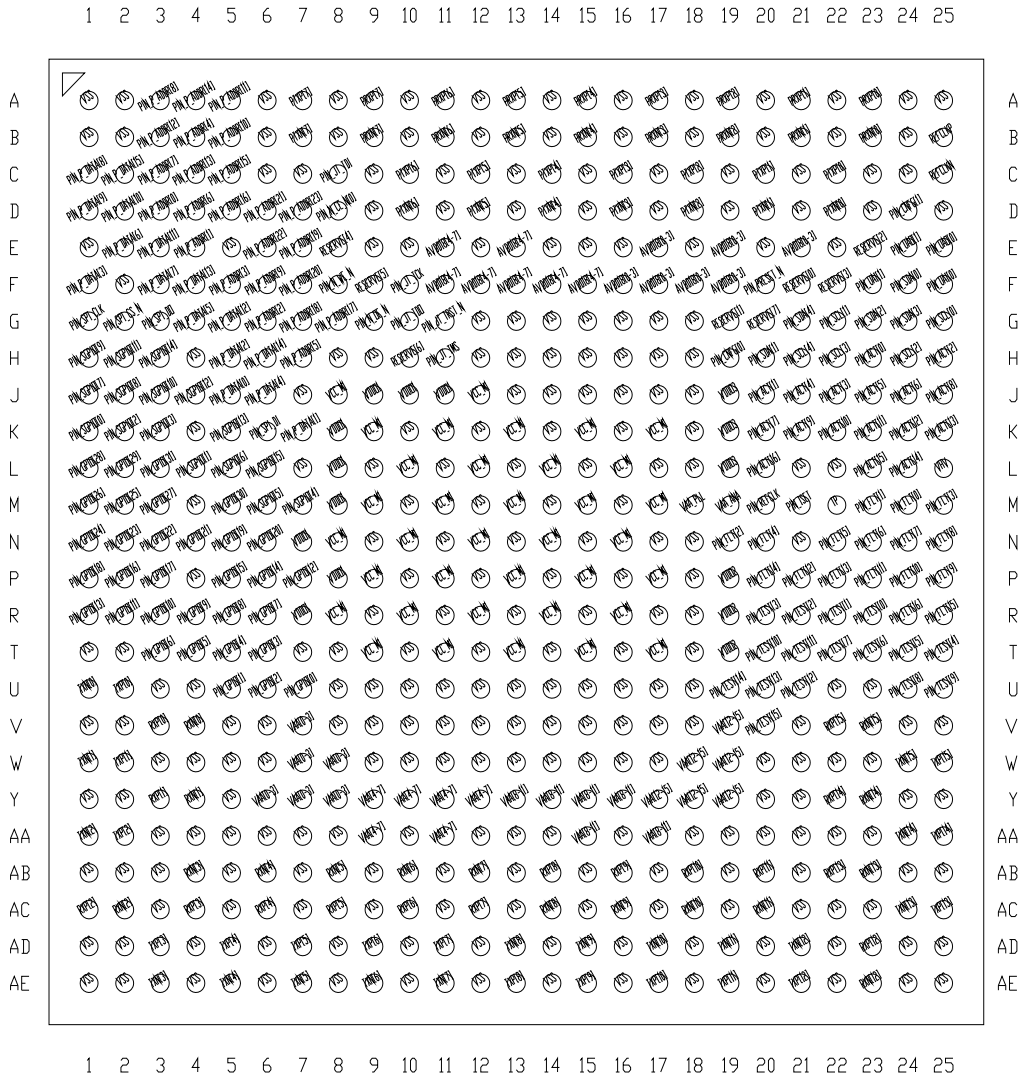
3 PACKAGE

This chapter contains the following sections:

3.1 Ball Diagram

Figure 3-1 illustrates the 625-Ball HFCBGA 21 × 21 mm ball diagram for the 88SE1475.

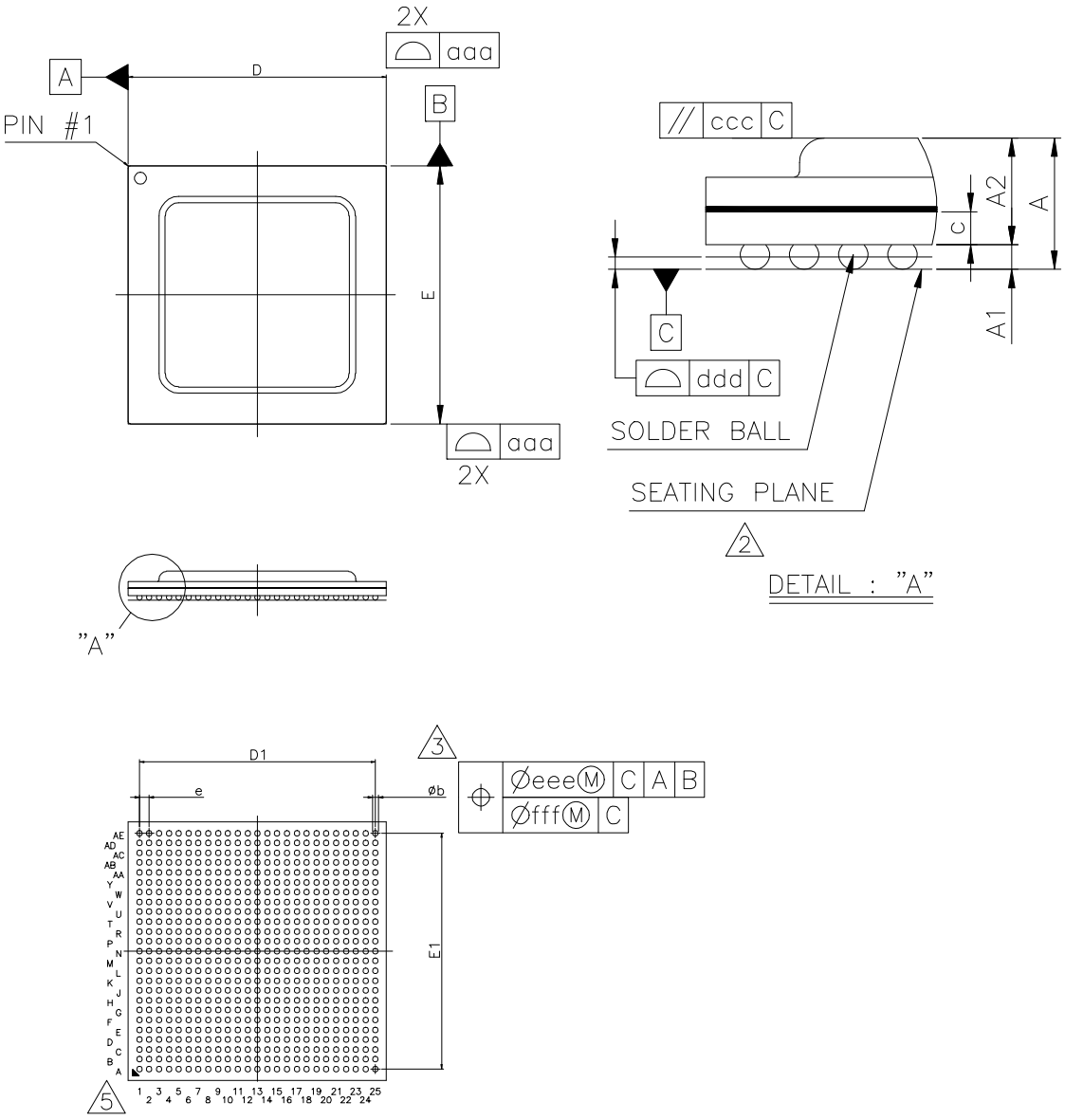
Figure 3-1 Ball Diagram



3.2 Mechanical Drawing

Figure 3-2 shows the mechanical drawing for the 88SE1475.

Figure 3-2 Package Mechanical Drawing



3.3 Mechanical Dimensions

Figure 3.3 lists the Mechanical Dimensions for the 88SE1475.

Figure 3-3 Package Mechanical Dimensions

Symbol	Unit: mm		
	MIN	NOM	MAX
A	2.23	2.38	2.53
A1	0.36	0.41	0.46
A2	---	1.97	---
c	---	0.57	---
D/E	20.80	21.00	21.20
D1/E1	---	19.20	---
e	---	0.80	---
b	0.44	0.54	0.64
aaa	0.20		
ccc	0.25		
ddd	0.20		
eee	0.25		
fff	0.10		

3.4 Signal Descriptions

This section contains the following subsections:

3.4.1 Signal Descriptions Overview

This section includes signal definitions and signal descriptions.

3.4.2 Signal Definitions

Table 3-1 shows signal types and definitions.

Table 3-1 Signal Type Definitions

Signal Type	Definition
I/O	Input and Output
I	Input Only
O	Output Only
OC	Open Collector
OD	Open-Drain Pad
Ground	Ground
Power	Power
NC	No Connect*
DNC	Do Not Connect†

* Pin is floating and is not connected internally to any active circuitry nor has any electrical continuity to any other pin

† Device pin to which there may or may not be an internal connection, but to which no external connections are allowed.

3.4.3 Signal Descriptions

This section outlines the 88SE1475 signal descriptions. Table 3-2 lists the General Purpose I/O Signals. Signals ending with the letter _N are active-low signals.

Table 3-2 General Purpose I/O Signals

Signal Name	Signal Number	Type	Description
PIN_ACT[16]	L20	I/O	Activity LED. Internal Pull-Up. The following pins can be used as GPIO: • PIN_ACT[7:0]–SATA PHY[7:0] activity. • PIN_ACT[15:8]–SATA PHY[15:8] activity. • PIN_ACT[16]–Global Activity. Enabled when any SATA PHY is active.
PIN_ACT[15]	L23		
PIN_ACT[14]	L24		
PIN_ACT[13]	K25		
PIN_ACT[12]	K24		
PIN_ACT[11]	K23		
PIN_ACT[10]	K22		
PIN_ACT[9]	K21		
PIN_ACT[8]	J25		
PIN_ACT[7]	K20		
PIN_ACT[6]	J24		
PIN_ACT[5]	J23		
PIN_ACT[4]	J21		
PIN_ACT[3]	J22		
PIN_ACT[2]	H25		
PIN_ACT[1]	J20		
PIN_ACT[0]	H23		

Table 3-2 General Purpose I/O Signals (continued)

Signal Name	Signal Number	Type	Description
PIN_FLT[16]	R24	I/O	• Fault LED, Active Low Signals. • PIN_FLT is active when PHY is not ready or when PHY is ready and there is any PHY related error or connection error. • PIN_FLT[15:0]--Corresponds to SATA PHY15 through PHY0. When PHY is not ready, PIN_FLT[15:0] is always on. After the PHY is ready, a fault occurs. • PIN_FLT[16]–Global Fault indication. The indicator is on when any SATA_PHY has a fault. • PIN_FLT[7:0]–Corresponds to SATA_PHY7 through PHY0. • PIN_FLT[15:8]–Corresponds to SATA_PHY15 through PHY8.
PIN_FLT[15]	R25		
PIN_FLT[14]	P20		
PIN_FLT[13]	P22		
PIN_FLT[12]	P21		
PIN_FLT[11]	P23		
PIN_FLT[10]	P24		
PIN_FLT[9]	P25		
PIN_FLT[8]	N25		
PIN_FLT[7]	N24		
PIN_FLT[6]	N23		
PIN_FLT[5]	N22		
PIN_FLT[4]	N20		
PIN_FLT[3]	M25		
PIN_FLT[2]	N19		
PIN_FLT[1]	M23		
PIN_FLT[0]	M24		
PIN_TEST[15]	V20	I/O	Test Pin. See Table 7-8, Boot Modes for more detailed description.
PIN_TEST[14]	U19		
PIN_TEST[13]	U20		
PIN_TEST[12]	U21		
PIN_TEST[11]	T21		
PIN_TEST[10]	T20		
PIN_TEST[9]	U25		
PIN_TEST[8]	U24		
PIN_TEST[7]	T22		
PIN_TEST[6]	T23		
PIN_TEST[5]	T24		
PIN_TEST[4]	T25		
PIN_TEST[3]	R20		
PIN_TEST[2]	R21		
PIN_TEST[1]	R22		
PIN_TEST[0]	R23		

Table 3-2 General Purpose I/O Signals (continued)

Signal Name	Signal Number	Type	Description
PIN_SGPIO[15]	L6	I/O	Serial GPIO 15. This pin has different definitions when I2C_SGPIO_FLT_PAD_SLCT (RE402C104h [9]) is set as follows: **0h:** This pin replaces PIN_SCL[4]. **1h:** This pin is SGPIO3 SCLK.
PIN_SGPIO[14]	H3	I/O	Serial GPIO 14. This pin has different definitions when I2C_SGPIO_FLT_PAD_SLCT (RE402C104h [9]) is set as follows: **0h:** This pin replaces PIN_SDA[4]. **1h:** This pin is SGPIO3 SLOAD.
PIN_SGPIO[13]	K5	I/O	Serial GPIO 13. This pin has different definitions when I2C_SGPIO_FLT_PAD_SLCT (RE402C104h [9]) is set as follows: **0h:** Input signal. Not used. **1h:** This pin is SGPIO3 SDOUT.
PIN_SGPIO[12]	J4	I/O	Serial GPIO 12. This pin has different definitions when I2C_SGPIO_FLT_PAD_SLCT (RE402C104h [9]) is set as follows: **0h:** Input signal. Not used. **1h:** This pin is SGPIO3 SDIN.
PIN_SGPIO[11]	H2	I/O	Serial GPIO 11. This pin has different definitions when I2C_SGPIO_FLT_PAD_SLCT (RE402C104h [9]) is set as follows: **0h:** This pin replaces PIN_SCL[3]. **1h:** This pin is SGPIO2 SCLK.
PIN_SGPIO[10]	J3	I/O	Serial GPIO 10. This pin has different definitions when I2C_SGPIO_FLT_PAD_SLCT (RE402C104h [9]) is set as follows: **0h:** This pin replaces PIN_SDA[3]. **1h:** This pin is SGPIO2 SLOAD.
PIN_SGPIO[9]	H1	I/O	Serial GPIO 9. This pin has different definitions when I2C_SGPIO_FLT_PAD_SLCT (RE402C104h [9]) is set as follows: **0h:** Input signal. Not used. **1h:** This pin is SGPIO2 SDOUT.

Table 3-2 General Purpose I/O Signals (continued)

Signal Name	Signal Number	Type	Description
PIN_SGPIO[8]	J2	I/O	Serial GPIO 8. This pin has different definitions when I2C_SGPIO_FLT_PAD_SLCT (RE402C104h [9]) is set as follows: **0h:** Input signal. Not used. **1h:** This pin is SGPIO2 SDIN.
PIN_SGPIO[7]	J1	I/O	Serial GPIO 7. This pin has different definitions when I2C_SGPIO_FLT_PAD_SLCT (RE402C104h [9]) is set as follows: **0h:** This pin replaces PIN_SCL[2]. **1h:** This pin is SGPIO1 SCLK.
PIN_SGPIO[6]	L5	I/O	Serial GPIO 6. This pin has different definitions when I2C_SGPIO_FLT_PAD_SLCT (RE402C104h [9]) is set as follows: **0h:** This pin replaces PIN_SDA[2]. **1h:** This pin is SGPIO1 SLOAD.
PIN_SGPIO[5]	M6	I/O	Serial GPIO 5. This pin has different definitions when I2C_SGPIO_FLT_PAD_SLCT (RE402C104h [9]) is set as follows: **0h:** Input signal. Not used. **1h:** This pin is SGPIO1 SDOUT.
PIN_SGPIO[4]	M7	I/O	Serial GPIO 4. This pin has different definitions when I2C_SGPIO_FLT_PAD_SLCT (RE402C104h [9]) is set as follows: **0h:** Input signal. Not used. **1h:** This pin is SGPIO1 SDIN.
PIN_SGPIO[3]	K3	I/O	Serial GPIO 3. This pin has different definitions when I2C_SGPIO_FLT_PAD_SLCT (RE402C104h [9]) is set as follows: **0h:** This pin replaces PIN_SCL[1]. **1h:** This pin is SGPIO0 SCLK.
PIN_SGPIO[2]	K2	I/O	Serial GPIO 2. This pin has different definitions when I2C_SGPIO_FLT_PAD_SLCT (RE402C104h [9]) is set as follows: **0h:** This pin replaces PIN_SDA[1]. **1h:** This pin is SGPIO0 SLOAD.

Table 3-2 General Purpose I/O Signals (continued)

Signal Name	Signal Number	Type	Description
PIN_SGPIO[1]	L4	I/O	Serial GPIO 1. This pin has different definitions when I2C_SGPIO_FLT_PAD_SLCT (RE402C104h [9]) is set as follows: **0h:** Input signal. Not used. **1h:** This pin is SGPIO0 SDOUT.
PIN_SGPIO[0]	K1	I/O	Serial GPIO 0. This pin has different definitions when I2C_SGPIO_FLT_PAD_SLCT (RE402C104h [9]) is set as follows: **0h:** Input signal. Not used. **1h:** This pin is SGPIO0 SDIN.

Table 3-2 General Purpose I/O Signals (continued)

Signal Name	Signal Number	Type	Description
PIN_GPIO[31]	L3	I/O	General Purpose I/O Pin.
PIN_GPIO[30]	M5		
PIN_GPIO[29]	L2		
PIN_GPIO[28]	L1		
PIN_GPIO[27]	M3		
PIN_GPIO[26]	M1		
PIN_GPIO[25]	M2		
PIN_GPIO[24]	N1		
PIN_GPIO[23]	N2		
PIN_GPIO[22]	N3		
PIN_GPIO[21]	N4		
PIN_GPIO[20]	N6		
PIN_GPIO[19]	N5		
PIN_GPIO[18]	P1		
PIN_GPIO[17]	P3		
PIN_GPIO[16]	P2		
PIN_GPIO[15]	P5		
PIN_GPIO[14]	P6		
PIN_GPIO[13]	R1		
PIN_GPIO[12]	P7		
PIN_GPIO[11]	R2		
PIN_GPIO[10]	R3		
PIN_GPIO[9]	R4		
PIN_GPIO[8]	R5		
PIN_GPIO[7]	R6		
PIN_GPIO[6]	T3		
PIN_GPIO[5]	T4		
PIN_GPIO[4]	T5		
PIN_GPIO[3]	T6		
PIN_GPIO[2]	U6		
PIN_GPIO[1]	U5		
PIN_GPIO[0]	U7		

Table 3-3 Clock and Reset Signals

Signal Name	Signal Number	Type	Description
PIN_REFCLK	M20	I	Reference Clock. • 50 MHz • 1.8V • ± 50 ppm
PIN_PRESET_N	F20	I	PCIe RESET_N Signal. Chip RESET_N Signal.
TP	M22	I/O	Analog Test Port.

Table 3-4 I2C Signals

Signal Name	Signal Number	Type	Description
PIN_SDA[4]	G21	I/O	I2C Interface Data Signal. Internal Pull-Up.
PIN_SDA[3]	G24		
PIN_SDA[2]	G23		
PIN_SDA[1]	H20		
PIN_SDA[0]	F24		
PIN_SCL[4]	H21	I/O	I2C Interface Clock Signal. Internal Pull-Up.
PIN_SCL[3]	H22		
PIN_SCL[2]	H24		
PIN_SCL[1]	G22		
PIN_SCL[0]	G25		

Table 3-5 UART Signals

Signal Name	Signal Number	Type	Description
PIN_UAO[1]	E24	O	UART Interface Output.
PIN_UAO[0]	E25		
PIN_UAI[1]	F23	I	UART Interface Input.
PIN_UAI[0]	F25		

Table 3-6 NVSRAM Signals

Signal Name	Signal Number	Type	Description
PIN_N_WE_N	F8	O	Flash Interface Write Enable Signals.
PIN_N_OE_N	G9	O	Flash Interface Output Enable Signals.
RESERVE[6]	H10	NC	Reserved. Not Connected.
RESERVE[5]	F9		
RESERVE[4]	E8		
PIN_N_CE_N[0]	D8	O	Flash Interface Chip Enable Signal.
PIN_P_ADDR[23]	D7	O	Flash Interface Address Signals.
PIN_P_ADDR[22]	E6		
PIN_P_ADDR[21]	D6		
PIN_P_ADDR[20]	F7		
PIN_P_ADDR[19]	E7		
PIN_P_ADDR[18]	G7		
PIN_P_ADDR[17]	G8		
PIN_P_ADDR[16]	D5		
PIN_P_ADDR[15]	C5		
PIN_P_ADDR[14]	A4		
PIN_P_ADDR[13]	C4		
PIN_P_ADDR[12]	B3		
PIN_P_ADDR[11]	A5		
PIN_P_ADDR[10]	B5		
PIN_P_ADDR[9]	F6		
PIN_P_ADDR[8]	A3		
PIN_P_ADDR[7]	C3		
PIN_P_ADDR[6]	D4		
PIN_P_ADDR[5]	H7		
PIN_P_ADDR[4]	B4		
PIN_P_ADDR[3]	F5		
PIN_P_ADDR[2]	G6		
PIN_P_ADDR[1]	E4		
PIN_P_ADDR[0]	D3		

Table 3-6 NVSRAM Signals (continued)

Signal Name	Signal Number	Type	Description
PIN_P_DATA[15]	C2	I/O	Flash Interface Data Signals.
PIN_P_DATA[14]	H6		
PIN_P_DATA[13]	F4		
PIN_P_DATA[12]	G5		
PIN_P_DATA[11]	E3		
PIN_P_DATA[10]	D2		
PIN_P_DATA[9]	D1		
PIN_P_DATA[8]	C1		
PIN_P_DATA[7]	F3		
PIN_P_DATA[6]	E2		
PIN_P_DATA[5]	G4		
PIN_P_DATA[4]	J6		
PIN_P_DATA[3]	F1		
PIN_P_DATA[2]	H5		
PIN_P_DATA[1]	K7		
PIN_P_DATA[0]	J5		

Table 3-7 System Interface Signals

Signal Name	Signal Number	Type	Description
PIN_CNFG[1]	D24	I	Chip Operation Mode.
PIN_CNFG[0]	H19	I	Chip Operation Mode.
REFCLKP	B25	I	PCIe Reference Clock. 100 MHz.
REFCLKN	C25	I	PCIe Reference Clock. 100 MHz.

Table 3-8 SPI Interface Signals

Signal Name	Signal Number	Type	Description
PIN_SPI_DI	K6	I	SPI Interface Data in Signals.
PIN_SPI_DO	G3	O	SPI Interface Data out Signals.

Table 3-8 SPI Interface Signals (continued)

Signal Name	Signal Number	Type	Description
PIN_SPI_CS_N	G2	O	SPI Interface Chip Select Signals.
PIN_SPI_CLK	G1	O	SPI Interface Clock Signals.

Table 3-9 PCIe Interface Signals

Signal Name	Signal Number	Type	Description
PIN_ISET	M21	I	Current Source. 6.04 Ohm resistor with 1% accuracy bias current resistor.

Table 3-10 SATA Transmitter and Receiver Interface Signals

Signal Name	Signal Number	Type	Description
RXP[15]	V22	I	RXP[7:0]–SATA PHY 7–0 Receiver Differential Signal. RXP[15:8]–SATA PHY 15–8 Receiver Differential Signal. 6 GHz.
RXP[14]	Y22		
RXP[13]	AB22		
RXP[12]	AD23		
RXP[11]	AB20		
RXP[10]	AB18		
RXP[9]	AB16		
RXP[8]	AB14		
RXP[7]	AC12		
RXP[6]	AC10		
RXP[5]	AC8		
RXP[4]	AC6		
RXP[3]	AC4		
RXP[2]	AC1		
RXP[1]	Y3		
RXP[0]	V3		

Table 3-10 SATA Transmitter and Receiver Interface Signals (continued)

Signal Name	Signal Number	Type	Description
RXN[15]	V23	I	RXN[7:0]–SATA PHY 7–0 Receiver Differential Signals. RXN[15:8]–SATA PHY 15–8 Receiver Differential Signals. 6 GHz.
RXN[14]	Y23		
RXN[13]	AB23		
RXN[12]	AE23		
RXN[11]	AC20		
RXN[10]	AC18		
RXN[9]	AC16		
RXN[8]	AC14		
RXN[7]	AB12		
RXN[6]	AB10		
RXN[5]	AB8		
RXN[4]	AB6		
RXN[3]	AB4		
RXN[2]	AC2		
RXN[1]	Y4		
RXN[0]	V4		
TXP[15]	W25	O	TXP[7:0]–SATA 7–0 Transmitter Differential Signals. TXP[15:8]–SATA 15–8 Transmitter Differential Signals. 6 GHz.
TXP[14]	AA25		
TXP[13]	AC25		
TXP[12]	AE21		
TXP[11]	AE19		
TXP[10]	AE17		
TXP[9]	AE15		
TXP[8]	AE13		
TXP[7]	AD11		
TXP[6]	AD9		
TXP[5]	AD7		
TXP[4]	AD5		
TXP[3]	AD3		
TXP[2]	AA2		
TXP[1]	W2		
TXP[0]	U2		

Table 3-10 SATA Transmitter and Receiver Interface Signals (continued)

Signal Name	Signal Number	Type	Description
TXN[15]	W24	O	TXN[7:0]–SATA PHY 7–0 Transmitter Differential Signals. TXN[15:8]–SATA PHY 15–8 Transmitter Differential Signals. 6 GHz.
TXN[14]	AA24		
TXN[13]	AC24		
TXN[12]	AD21		
TXN[11]	AD19		
TXN[10]	AD17		
TXN[9]	AD15		
TXN[8]	AD13		
TXN[7]	AE11		
TXN[6]	AE9		
TXN[5]	AE7		
TXN[4]	AE5		
TXN[3]	AE3		
TXN[2]	AA1		
TXN[1]	W1		
TXN[0]	U1		

Table 3-11 PCIe Transmitter and Receiver Interface Signals

Signal Name	Signal Number	Type	Description
PRXP[7]	A9	I	PRXP[7:0]–PCIe Lane 7–0 Receiver Differential Signal (PCIe Rx ±). 8 GTps.
PRXP[6]	A11		
PRXP[5]	A13		
PRXP[4]	A15		
PRXP[3]	A17		
PRXP[2]	A19		
PRXP[1]	A21		
PRXP[0]	A23		
PRXN[7]	B9	I	PRXN[7:0]–PCIe Lane 7–0 Receiver Differential Signals (PCIe Rx ±). 8 GTps.
PRXN[6]	B11		
PRXN[5]	B13		
PRXN[4]	B15		
PRXN[3]	B17		
PRXN[2]	B19		
PRXN[1]	B21		
PRXN[0]	B23		

Table 3-11 PCIe Transmitter and Receiver Interface Signals (continued)

Signal Name	Signal Number	Type	Description
PTXP[7]	A7	O	PTXP[7:0]–PCIe Lane 7–0 Transmitter Differential Signals (PCIe Tx -/+). 8 GTps.
PTXP[6]	C10		
PTXP[5]	C12		
PTXP[4]	C14		
PTXP[3]	C16		
PTXP[2]	C18		
PTXP[1]	C20		
PTXP[0]	C22		
PTXN[7]	B7	O	PTXN[7:0]–PCIe Lane 7–0 Transmitter Differential Signals (PCIe Tx -/+). 8 GTps.
PTXN[6]	D10		
PTXN[5]	D12		
PTXN[4]	D14		
PTXN[3]	D16		
PTXN[2]	D18		
PTXN[1]	D20		
PTXN[0]	D22		

Table 3-12 Power Interface Signals

Signal Name	Signal Number	Type	Description
VAA_PLL	M18	I	Analog Power. Typ 1.8V.
VAA_ANA	M19	I	Analog Power. Typ 1.8V.
AVDD18[4–7]	F15, F14, F13, F12, F11, E13, E11	I	PCIe Analog Power for PHY4 to PHY7 Shared. Typ 1.8V.
AVDD18[0–3]	F19, F18, F17, F16, E21, E19, E17	I	PCIe Analog Power for PHY0 to PHY3 Shared. Typ 1.8V.
VAA[12–15]	Y19, Y18, Y17, W19, W18, V19	I	SATA1 Analog Power for PHY12 to PHY15 Shared. Typ 1.8V.
VAA[8–11]	AA17, AA15, Y16, Y15, Y14, Y13	I	SATA1 Analog Power for PHY8 and PHY11 Shared. Typ 1.8V.
VAA[4–7]	AA11, AA9, Y12, Y11, Y10, Y9	I	SATA0 Analog Power for PHY4 and PHY7 Shared. Typ 1.8V.
VAA[0–3]	Y8, Y7, Y6, W8, W7, V7	I	SATA0 Analog Power for PHY0 and PHY3 Shared. Typ 1.8V

Table 3-12 Power Interface Signals (continued)

Signal Name	Signal Number	Type	Description
VDDO1	J9, J10, J11, K8, L8, M8, P8, N7, R7	I	PAD Power. Typ 2.5V.
VDDO2	P19, R19, T19	I	PAD Power. Typ 2.5V.
VDDO3	J19, K19, L19	I	PAD Power. Typ 2.5V.
VCC_M1	K9, K11, K13, K15, K17, L10, L12, L14, L16, M9, M11, M13, M15, N10, N12, N14, N16, P9, P11, P13, P15, P17, R10, R12, R14, R16, T11, T13, T15, N8, R8, J8, J12, M17, T9, T17	I	Core Digital Power. Typ 0.95V.

Table 3-12 Power Interface Signals (continued)

Signal Name	Signal Number	Type	Description
VSS	A1, A2, A6, A8, A10, A12, A14, A16, A18, A20, A22, A24, A25, B1, B2, B6, B8, B10, B12, B14, B16, B18, B20, B22, B24, C6, C7, C9, C11, C13, C15, C17, C19, C21, C23, C24, D9, D11, D13, D15, D17, D19, D21, D23, D25, E1, E5, E9, E10, E12, E14, E15, E16, E18, E20, E22, F2, G12, G13, G14, G15, G16, G17, G18, H4, H8, H9, H12, H13, H14, H15, H16, H17, H18, J7, J13, J14, J15, J16, J17, J18, K4, K10, K12, K14, K16, K18, L7, L9, L11, L13, L15, L17, L18, L21, L22, M4, M10, M12, M14, M16, N9, N11, N13, N15, N17, N18, N21, P4, P10, P12, P14, P16, P18, R9, R11, R13, R15, R17, R18, T1, T2, T7, T8, T10, T12, T14, T16, T18, U3, U4, U8, U9, U10, U11, U12, U13, U14, U15, U16, U17, U18, U22, U23, V1, V2, V5, V6, V8, V9, V10, V11, V12, V13, V14, V15, V16, V17, V18, V21, V24, V25, W3, W4, W5, W6, W9, W10, W11, W12, W13, W14, W15, W16, W17, W20, W21, W22, W23, Y1, Y2, Y5, Y20, Y21, Y24, Y25, AA3, AA4, AA5, AA6, AA7, AA8, AA10, AA12, AA13, AA14, AA16, AA18, AA19, AA20, AA21, AA22, AA23, AB1,	Ground	Ground.

Table 3-12 Power Interface Signals (continued)

Signal Name	Signal Number	Type	Description
(continued)	(continued) AB2, AB3, AB5, AB7, AB9, AB11, AB13, AB15, AB17, AB19, AB21, AB24, AB25, AC3, AC5, AC7, AC9, AC11, AC13, AC15, AC17, AC19, AC21, AC22, AC23, AD1, AD2, AD4, AD6, AD8, AD10, AD12, AD14, AD16, AD18, AD20, AD22, AD24, AD25, AE1, AE2, AE4, AE6, AE8, AE10, AE12, AE14, AE16, AE18, AE20, AE22, AE24, AE25,	Ground	(continued)

Table 3-13 Debug Signals

Signal Name	Signal Number	Type	Description
VHV	L25	I	For eFUSE Input Pin. eFUSE can be programmed when the signal is 1.8V. When the signal is 0.0V, eFUSE is protected.
RESERVE[7]	G20	I	Reserved Input Pin. Connect to the Ground.
RESERVE[3]	F22	I	External Pull Down to Ground.
RESERVE[2]	E23	I	External Pull Down to Ground.
RESERVE[1]	G19	I	External Pull Down to Ground.
RESERVE[0]	F21	I	External Pull Down to Ground.

Table 3-14 JTAG Signals

Signal Name	Signal Number	Type	Description
PIN_JT_TCK	F10	I	JTAG Test Clock.
PIN_JT_TDI	C8	I	JTAG Test Data Input.
PIN_JT_TDO	G10	O	JTAG Test Data Output.
PIN_JT_TMS	H11	I	JTAG Test Mode Select.
PIN_JT_TRST_N	G11	I	JTAG Test Reset.

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4 LAYOUT GUIDELINES

This chapter contains the following sections:

Note: The layout guidelines are provided simply as guidelines, and are not meant to restrict the customer from exercising discretion in implementing their board designs. In cases where it is deemed necessary to deviate from the guidelines, Marvell recommends that the customer consult with the Marvell Field Applications Engineers (FAE) to ensure that the performance of the Marvell product is not compromised. These guidelines are applicable to both SAS and SATA bus designs.

4.1 Overview

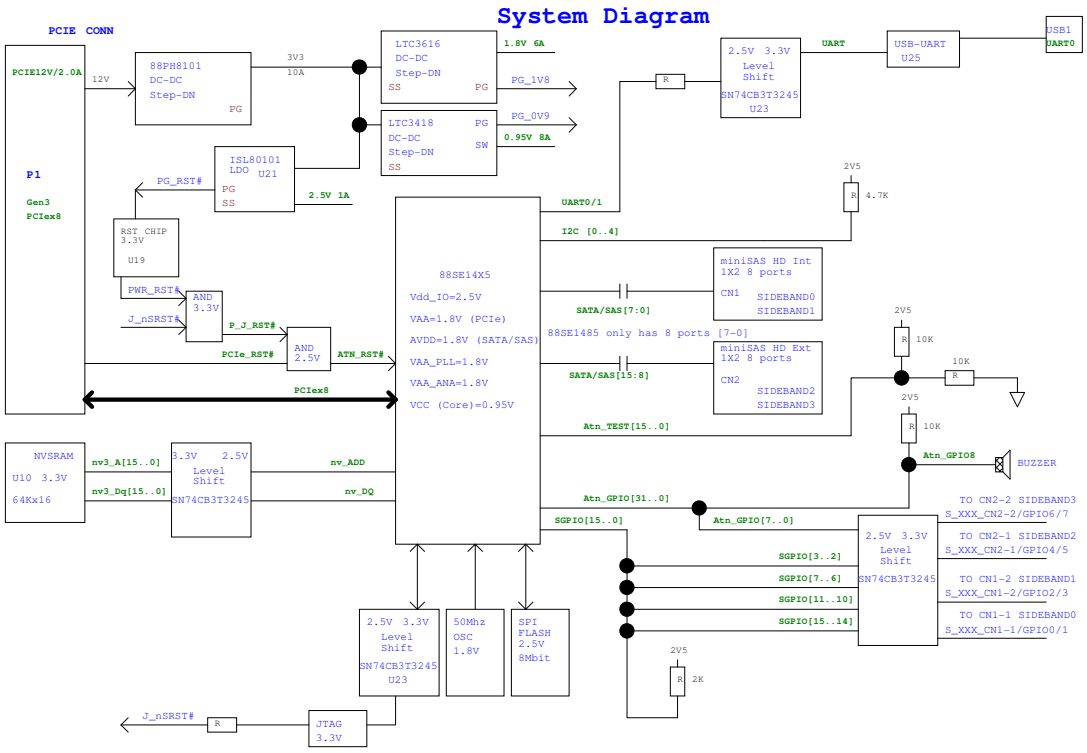
This chapter is for customers designing schematics and printed circuit boards with an 88SE1475-based system and is intended to aid in PCB design to ensure signal integrity. The guidelines in this chapter describe how to accommodate high-speed signals on the PCB.

4.2 Schematics

Customers can download the complete evaluation board schematic from the Marvell Extranet, or contact the Marvell Field Applications Engineers for the latest version.

Figure 4-1 shows the 88SE1475 System Diagram.

Figure 4-1 88SE1475 System Diagram



4.3 Layer Stack-Up

This section contains the following subsections:

4.3.1 Layer Stack-Up Overview

This section describes requirements for an 8-layer PCB.

- Layer 1—Top Side
- Layer 2—Solid Ground Plane
- Layer 3—High Speed Signals and Power Plane
- Layer 4—Power Plane
- Layer 5—Solid Ground Plane
- Layer 6—High Speed Signals and Power Plane
- Layer 7—Ground
- Layer 8—Bottom Side

Note: A minimum of 5 mil–wide traces and trace spacings for a 1.5 oz. copper layer are recommended.

4.3.2 Layer 1—Top Side

Place all active parts on the top side. Reserve Layer 1 for power traces and high-speed signals, such as those for the SATA bus, SDRAM, and PCI Express.

4.3.3 Layer 2—Solid Ground Plane

Place a solid ground plane directly below Layer 1, using 1 oz. copper. To reduce the amount of cross talk and EMI, place Layer 2 a minimum of 4 mils below Layer 1.

4.3.4 Layer 3—High Speed Signals and Power Plane

Use Layer 3 for a very few slow signals and high-speed signals that cannot be placed on Layer 1. To reduce the amount of cross talk and EMI, place Layer 3 a minimum of 4 mils below the ground plane. Create a power plane using any unused space. The copper planes help create internal capacitance, which helps reduce noise levels on the power supply of the chip. Avoid narrow traces and necks on this plane.

4.3.5 Layer 4—Power Plane

Limit the number of components on this layer. Placing one capacitor per power pin with different capacitor values, such as 1 µF, 0.1 µF and 0.01 µF, is recommended. Place slow or static signals, such as reset, on this layer. Create additional power or ground planes as needed.

4.3.6 Layer 5—Solid Ground Plane

A solid ground plane adds balance to the board layout stack-up. It provides coupling for the power plane on layer 4.

4.3.7 Layer 6—High Speed Signals and Power Plane

Some of the high-speed signals are routed on this layer. A differential 85Ω impedance for PCIe and 90Ω impedance for SAS must be maintained for the high-speed signals.

4.3.8 Layer 7—Ground

A solid ground plane must be located directly below the top layer of the PCB. This layer must be a minimum distance below the top layer in order to reduce the amount of crosstalk and EMI. There should be no cutouts in the ground plane. Use of 1 ounce copper is recommended.

4.3.9 Layer 8—Bottom Side

Some of the differential pairs for SATA and PCIe are routed on the top layer. A differential 85Ω impedance for PCIe and 90Ω impedance for SATA must be maintained for the high-speed signals.

4.3.10 Board Stack-Up/Routing Example

The board stack-up/routing example assumes the following:

- Board has 62 mils ± 5 mils thickness (1.57 mm ± 8%)
- The differential pairs have an impedance of 85Ω for PCIe and 90Ω for SATA.See Figure 4-2 for edge-coupled coated surface microstrips.

- The dielectric constant (E_R) is 4.2. (FR4 370HR 2116 E_R = 4.2 at 1GHz)

Figure 4-2 Edge-Coupled Coated Surface Microstrip

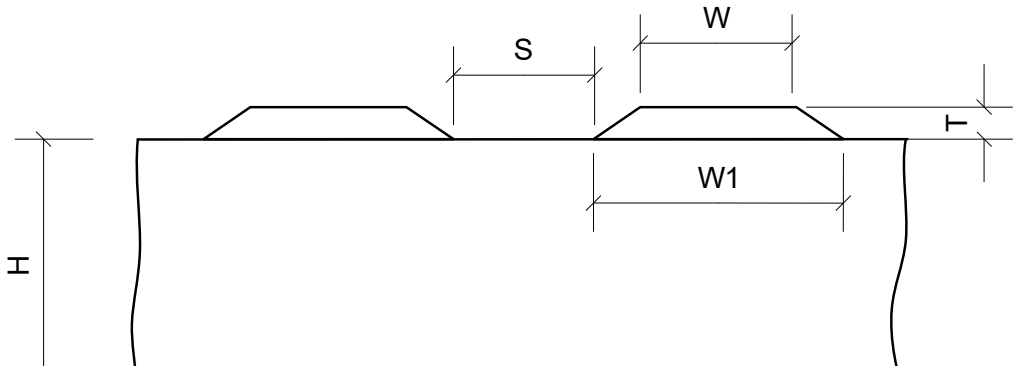


Table 4-1 details the dimensions for the edge-coupled coated surface microstrip shown in Figure 4-2.

Table 4-1 Microstrip Dimensions

Dimension	Length (Inches)
Height (H)	0.0045
Track Width (W)	0.004
Track Width (W1)	0.005
Separation (S)	0.006
Thickness (T)	0.0021

Note: The resulting differential impedance is 85Ω for PCIe and 90Ω for SAS, and the propagation delay is 150.185 ps/in.

Figure 4-3 provides an example of the PCB stack-up. This arrangement can vary as long as the 85Ω differential impedance for PCIe and 90Ω for SATA is maintained.

Figure 4-3 PCB Layer Stack-Up

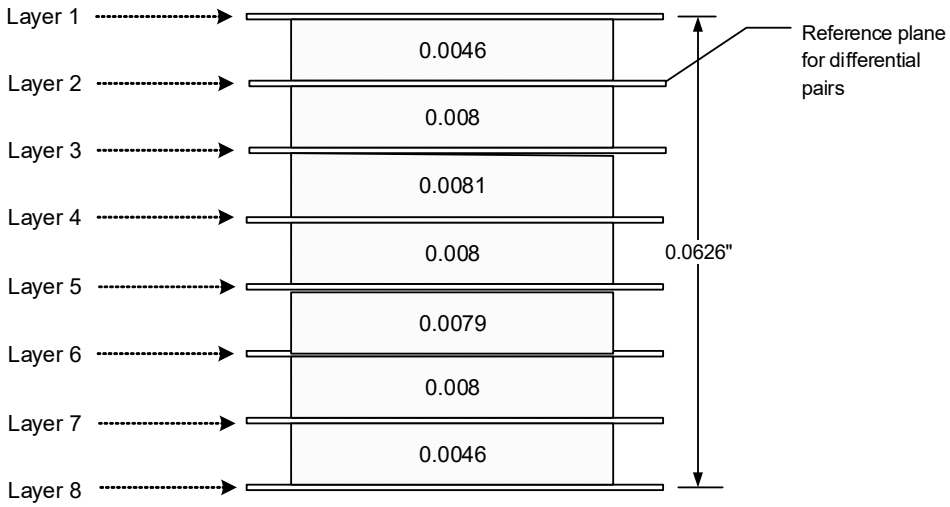


Table 4-2 details the stack-up parameters for the board shown in Figure 4-3.

Table 4-2 PCB Stack-Up Parameters

Layer	Description	Copper Weight (Ounces)	Trace Reference (Inches)	Target Impedance (Ω ± 10%)
1	Top Side	1	0.0085 trace	PCIe 85Ω differential
			0.0095 space	
			0.008 trace	SAS 90Ω differential
			0.011 space	
2	Solid Ground Plane	1	N/A	PCIe 85Ω differential
				SAS 90Ω differential
3	Low and High-Speed Signals	1	0.00825 trace	PCIe 85Ω differential
			0.01075 space	
			0.00725 trace	SAS 90Ω differential
			0.01075 space	
4	Power Plane	1	N/A	PCIe 85Ω differential
				SAS 90Ω differential
5	Solid Ground Plane	1	N/A	PCIe 85Ω differential
				SAS 90Ω differential
6	Low and High-Speed Signals	1	0.00825 trace	PCIe 85Ω differential
			0.01075 space	
			0.00725 trace	SAS 90Ω differential
			0.01075 space	
7	Ground	1	N/A	PCIe 85Ω differential
				SAS 90Ω differential
8	Bottom Side	1	0.0085 trace	PCIe 85Ω differential
			0.0095 space	
			0.008 trace	SAS 90Ω differential
			0.011 space	

4.4 Recommended PCB Layout and Design Guidelines

This section contains the following subsections:

4.4.1 Recommended PCB Layout and Design Guidelines Overview

This section describes the recommended PCB layout and design guidelines for PCB designers.

4.4.2 High-Speed Design Guidelines

This section contains the following subsections:

4.4.2.1 High-Speed Design Guidelines Overview

Any high-speed design must begin with a good board stack-up and careful consideration of the power planes. For the 88SE1475, the following power planes are required:

- VDDIO (2.5V power source for the digital I/O pins)
- VDD (0.95V power source for the core and digital circuitry)
- VAA_ANA, VAA_PLL, and VAA (1.8V power source for the analog circuitry and PCIe PHY)
- AVDD18 (1.8V absolute analog power supply for SAS PHY)

A single, solid ground plane is necessary to provide a good return path for routing layers. Take special care when routing the VAA and VSS.

4.4.2.2 General Tips for Stack-Up and Board Routing

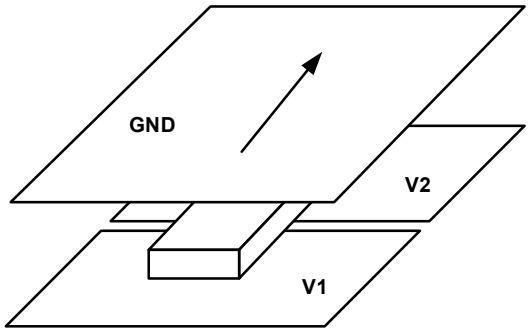
This section provides general tips for determining the stack-up and board routing. These tips are not intended as a substitute for consulting with a signal-integrity expert or performing simulations. Specific numbers or rules-of-thumb are not used, because they might change considerably depending on the situation.

General tips for determining the stack-up and board routing are as follows:

- Do not split the ground planes. Keep good spacing between possible sensitive analog circuitry on the board and the digital signals to sufficiently isolate noise. Try to provide at least one ground plane adjacent to all routing layers (See Figure 4-4).

- Keep trace layers as close as possible to the adjacent ground or power planes. This helps to limit cross talk and improve noise control on the planes.

Figure 4-4 Trace with at least One Solid Plane for Return Path



- When routing adjacent to a power plane, do not cross splits. If traces route over the power-plane splits, then provide a decoupling capacitor near the trace at the end that is not supplied by the adjacent power plane.
- Avoid running the critical signals in parallel and close to or directly over a gap, as this would change the impedance of the trace.
- Separate analog powers onto opposing planes to minimize the coupling area that an analog plane shares with an adjacent digital plane.
- Avoid more than two routing layers in a row for dual strip-line routing. The traces should cross at 90 degrees. This limits the tandem cross talk and offers better control impedance.
- Distribute the planes evenly to minimize warping.
- Prepare the impedance calculations or modeling prior to routing. This ensures that a reasonable trace thickness is used and that a desired board thickness is obtainable. Consult with a board fabricator for accurate impedance calculations.
- Allow adequate separation between fast signals to avoid cross talk. Cross talk also increases as the parallel traces get longer.

4.4.2.3 General Tips for Routing Traces Over a Split Power Plane

When packages become smaller (forcing vias to become smaller, thereby reducing the board thickness and layer counts) the PCB design may need to route traces over a split power plane.

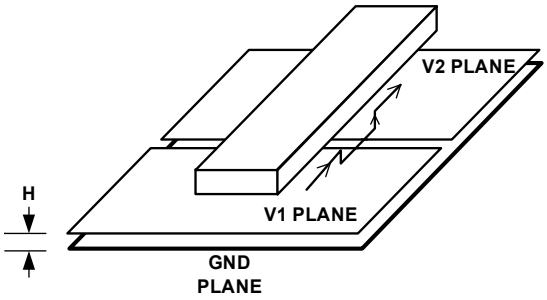
Some alternatives for providing return paths for these signals are as follows:

- Place a ground layer close enough to the split power plane to couple to a degree that provides buried capacitance, as shown in Figure 4-5. Having a thermal ground underneath the chip is recommended. Return signals that encounter splits in this situation simply jump to the ground plane, over the split, and back to the other power plane. Buried capacitance also provides the benefit of adding low-inductance decoupling to the board. To determine the amount of capacitance the planes provide, use the following equation:

$$C = 1.249 \bullet 10^{-13} \bullet E_r \bullet L \bullet W / H$$

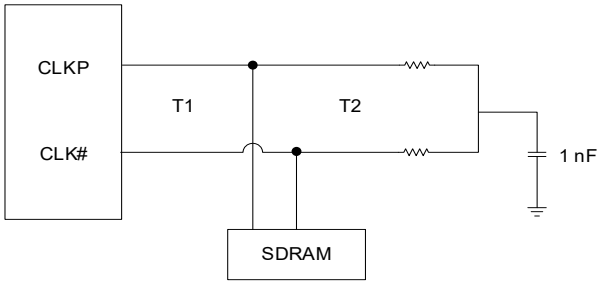
Where E_R is the dielectric coefficient, L • W represents the area of copper, and H is the separation between planes.

Figure 4-5 Close Power and Ground Planes Provide Coupling for Good Return Path



- Provide return-path capacitors that connect to both power planes and jump the split, as shown in Figure 4-6. Place them close to the traces so that there is one capacitor for every four or five traces. The capacitors then provide the return path.

Figure 4-6 Return Path Capacitor for Split Planes



- Allow only static or slow signals on layers where they are adjacent to split planes.

Use caution when applying these techniques. Digital traces should not cross over analog planes and vice-versa. All of these rules should be followed closely to prevent noise-contamination problems caused by routing over the wrong plane. By controlling the return path tightly, noise on the power and ground planes can be controlled.

4.4.3 Differential Impedance Signal Design Guidelines

This section contains the following subsections:

- Differential Impedance Signal Design Guidelines Overview
- Differential Impedance Design
- Differential Impedance Structures

4.4.3.1 Differential Impedance Signal Design Guidelines Overview

The differential signals have very fast rise or fall times—on the order of picoseconds. Treat these interconnects as transmission lines rather than simple wire connections. One of the fundamental properties of a transmission line is the characteristic impedance, or Z0. The characteristic impedance is determined by the relative dielectric constant of the PCB material (E_R), the thickness of the dielectric, and the width of the transmission line.

Keeping the trace length identical between the two traces is recommended when routing the differential pairs. Differences in trace length translate directly into signal skew. In the case of differential signals, the signals travel in opposite directions and noise cancellation occurs due to coupled complementary fields. The field cancellation of differential signals reduces far-field emissions. In this configuration, emissions from differential signals can come only from differential skew, so controlling skew through routing is a key to reduced EMI levels.

4.4.3.2 Differential Impedance Design

The major steps in differential impedance design are as follows:

1. Select the transmission line geometry. An over-under geometry that provides very strong coupling between traces is not recommended, because it requires extra layers. A stack-up thickness geometry is difficult to control, which results in variation of the differential impedance. A side-side geometry or an edge-side coupled geometry controls impedance and avoids adjacent-layer coupling when using solid ground planes.
2. Determine the target impedance for signals without coupling using the nominal width and stack-up. The nominal uncoupled trace impedance should be approximately 5Ω to 10Ω higher than one half of the desired differential impedance.
3. Compute the differential impedance.
4. Adjust the spacing and re-route until the proper differential impedance is achieved, or adjust the trace width and reroute.

4.4.3.3 Differential Impedance Structures

The following are typical structures used in differential impedance design:

- Strip-Line Structure
- Micro-Strip Structure

Strip-Line Structure

Advantages of the strip-line structure are as follows:

- Strong coupling between the traces
- Constant impedance and propagation velocity
- Less radiated emission and EMI issues
- Less cross talk

Micro-Strip Structure

Advantages of the micro-strip structure are as follows:

- Top layer can be used for signal trace
- Fewer layers
- Vias are not required

The SATA lines are 90Ω differential lines. The 90Ω termination resistors are built into the chip, so no additional external 90Ω resistors are required on the Tx and Rx pairs.

4.4.4 General Design Guidelines

This section contains the following subsections:

4.4.4.1 General Design Guidelines Overview

The following guidelines help to improve signal quality and transmission distances:

- Use surface-mount package resistors and capacitors with a smaller package parasitic value (for example, 0402 is better than 0603).
- Use rounded corners rather than 90º or 45º corners.
- Do not route the digital signals from other circuits across the area of the transmitter and receiver.
- Route PCIe Rx ± on the top layer and PCIe Tx ± on another signal layer.
- For each SAS port, route the SAS Tx ± on the top layer and the SAS Rx ± on another signal layer.
- Use Mini-SAS HD through-holeconnectors. Based on 88SE1475 ball map, Tx are the outer rows, which can be routed on the top layer. Rx are the inner rows, which can be routed as the bottom layer by one via. Route RXP/N[7] as the bottom layer although it is the outer row.
- Each pair of PCIe and SAS differential vias must have a pair GND vias next to them.
- The spacing between the trace pair and any other differential pair should be a least three times the spacing within the trace pair.
- The spacing between the trace pair and any non-differential signal should be a least four times the spacing within the trace pair

4.4.4.2 Analog Input Signal Interconnect

The pin placements minimize the coupling between digital signals and the analog counterparts. Try to keep the analog input traces away from possible sources of noise.

To avoid picking up noise on the analog inputs, shield the input traces with ground traces extending to the outputs.

To achieve the best noise reduction, try to reduce and equalize the parasitic capacitances and inductances seen by the differential analog input signals. These traces should have matched lengths, a minimal gap between them, and an 85Ω differential impedance for PCIe and 90Ω for SATA.

4.4.4.3 Bias Current Resistor (ISET)

Connect a bias current resistor between the ISET pin and the adjacent top ground plane, mounting it as close as possible to the ISET pin. Refer to the ISET pin description in Table 3-9, PCIe Interface Signals for the recommended resistance value.

4.4.4.4 Digital Signal Interconnect

Isolate the analog signals from the digital signals. The digital signals should not overlay the analog signals or power traces.

To reduce digital noise injected into the internal protection diodes, avoid excessively high slew-rate signals, which can contribute to ringing that nearby analog lines can detect. To reduce the slew rates of certain critical digital signal lines, such as the SDRAM clock signal line, use series resistors at the signal source.

4.4.4.5 Traces

Keep the traces as short as possible. The initial component placement should be carefully considered. Eliminate or reduce stub lengths. Keep the high-speed traces at least ten times the trace width away from any other signal, which might cause capacitively coupled noise in the signals.

Critical signals should avoid running parallel and close to or directly over a gap, as this would change the impedance of the trace. To avoid cross talk, allow separation between the fast signals. Cross-talk also increases as the parallel traces get longer.

When routing the traces for the decoupling capacitors, make the traces short and thick.

4.4.4.6 Vias

Each signal in a pair must have the same number of vias. Vias and their clearance holes in power or ground planes can cause the impedance discontinuities in nearby signals. To minimize impedance discontinuities, eliminate the use of vias and keep the differential pair traces on the same side and layer of the PCB.

If vias cannot be eliminated, keep them away from the traces by at least 2.5 times the trace width. Minimize the number of vias as much as possible, as vias increase the capacitive effect. Giving vias more clearance reduces the capacitive effect.

4.4.4.7 Power Pins

The VAA (analog power) pins are separated from the digital power pins using a low-impedance ferrite bead. The bead acts as a wide-band choke where the frequency is attenuated by 30 dB or more between 1 MHz and 650 MHz. The noise levels on these analog power pins should be less than 100 mV.

4.4.4.8 SATA Lines

The SATA lines (TX_P, TX_M, RX_P, RX_M) are 90Ω differential lines. The 90Ω termination resistors are built into the chip, so no additional external 90Ω resistors are required on the Tx and Rx pairs. See section 4.5, SATA Routing for more information on SATA routing.

4.4.4.9 Reference Clock

For reliable operation, the reference clock to the 88SE1475 should be accurate and stable. Use an oscillator with jitter bandwidth from 50 MHz to half of the reference clock frequency and the peak-to-peak jitter to less than 150 ps.

4.5 SATA Routing

The Serial AT Attachment standard calls for AC coupling of the signals. Using 0.01 µF, 0402 10% X7R or NPO-type capacitors enables DC blocking. Using 0402 capacitors is critical to reducing inductance and for improving signal quality.

The guidelines for SATA lines are as follows:

The Tx and Rx trace pairs should have a 90Ω differential impedance.

The Tx and Rx trace pairs should have single-ended impedance of 50Ω ± 5Ω or common-mode impedance of 25Ω ± 2.5Ω.

The Tx and Rx trace pairs of the high speed 1.5/3.0/6.0 GHz SATA lines should have matching lengths. For example, TX_P should be matched to TX_M, and RX_P should be matched to RX_M.

No other signals should be routed to these traces on any layer. No via or stubs should be on these traces. Keep these traces as short as possible to the connector. A solid ground plane should lie directly under these traces.

The length of differential pair (TX_P, TX_M and RX_P, RX_M) should be as short as possible, preferably less than two inches.

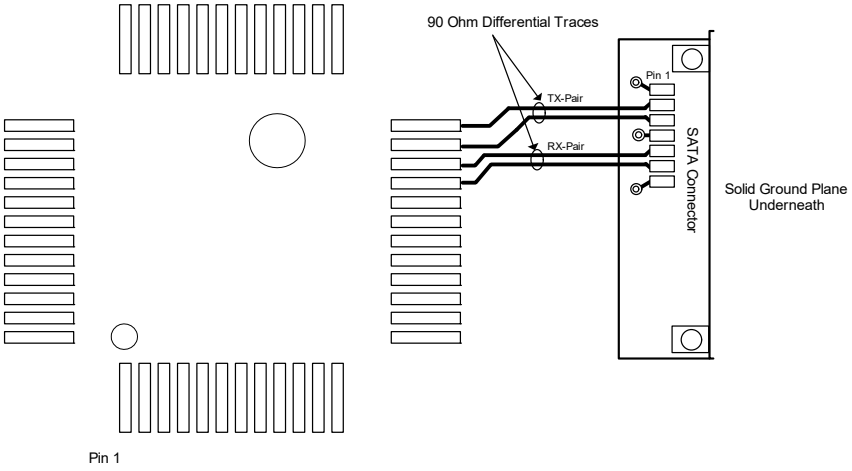
The pairs should have the same length and number of vias (0, if possible).

Limit the skew requirement between the TX_P and TX_M, or RX_P and RX_M to less than 1% of the cycle time (333.3 ps). This means the skew should be less than 3.33 ps.

Typically, if FR-4 is used as the dielectric material and the reflective index is equal to 2.0, then by calculation, an electromagnetic wave takes 1 ps to travel 200 µm with FR-4 as the dielectric. Using this calculation, the skew requirement translates into a maximum of 750 µm difference between the TX_P and TX_M, and RX_P and RX_M lines. However, 666 µm is the maximum acceptable difference. Keeping the difference in length to less than 500 µm is preferable.

Figure 4-7 illustrates an example of SATA trace routing. The decoupling capacitors (not shown in the figure) are located on the backside of the PCB. Vias are used to connect the capacitors to their associated pin locations on the PCB.

Figure 4-7 Example of SATA Trace Routing



4.6 Power and Ground

This section contains the following subsections:

4.6.1 Power and Ground Overview

The 88SE1475 operates using the following power supplies:

- VDD Power (0.95V)
- VAA and AVDD18 Power (1.8V)
- VDDIO Power (2.5V)

Note: Verify that the regulators can support the required wattage.

4.6.2 VDD Power (0.95V)

Use short and wide copper traces to connect all digital power (VDD) pins directly to a VDD plane to minimize digital power-trace inductances.

Note: VDD always requires 1.0V and must be isolated from the rest of the power plane.

To connect to the VDD plane, place vias close to the VDD pins and avoid using the traces on the top layer. Place capacitors around the three sides of the PCB near the VDD pins, with the following ratings:

- 0.001 µF (1 capacitor)
- 0.1 µF (2 capacitors)
- 2.2 µF (1 ceramic capacitor)

The 2.2 µF ceramic decoupling capacitor filters the lower frequency power supply noise.

These PCB layout recommendations assume that the components are placed on a single side. If placing components on both sides, install the power-pin capacitors on the second side directly under the 88SE1475.

To reduce system noise, place the high-frequency surface-mount monolithic ceramic bypass capacitors as close as possible to the VDD pins. Place at least one decoupling capacitor on each side of the IC package.

Alternatively, if using a two-sided PCB, place the decoupling capacitors behind the PCB near the pins—those with low ratings (1000–10,000 pF) are more effective at higher frequencies. Use short and wide copper traces to minimize parasitic inductances.

4.6.3 VAA and AVDD18 Power (1.8V)

When routing the 88SE1475 device, ensure that the VAA signals are highly filtered with decoupling capacitors placed as close to the pins as possible.

Analog power (VAA) and analog power supply for SAS PHY (AVDD18) operate at 1.8V. Do not connect the VAA pins directly to the localized digital power (VDD) plane. Instead, create a small power plane on the internal power layer below the VAA pins. Place a ferrite bead and decoupling capacitors close to the pins. Route each pin directly to the isolated plane.

4.6.4 VDDIO Power (2.5V)

VDDIO is the digital I/O supply and operates either at 2.5V.

To connect to the 2.5V power plane, place a via close to the VDDIO pins and avoid using a long trace on the top layer. Connect a 0.001 µF and a 0.01 µF capacitor between VDDPIO and the via connecting to the PCB 2.5V internal power plane.

5 ELECTRICAL SPECIFICATIONS

This chapter contains the following sections:

5.1 Power Supply

Table 5-1 defines the Power Supply for the 88SE1475.

Table 5-1 Power Supply

Parameter	Symbol	Minimum	Typical	Maximum	Units
Absolute Digital I/O Pad Power Supply	VDDOX	N/A	N/A	200	mA
Absolute Digital Power Supply	VDD	N/A	N/A	9500	mA
Absolute Analog Power	VAA_ANA	N/A	N/A	15	mA
Absolute Analog Power	VAA_PLL	N/A	N/A	15	mA
Absolute Analog Power Supply for SATA PHY	VAA	N/A	N/A	2000	mA
Absolute Analog Power Supply for PCIe PHY	AVDD18	N/A	N/A	1000	mA

5.2 Absolute Maximum Ratings

Table 5-2 defines the Absolute Maximum Ratings for the 88SE1475.

Table 5-2 Absolute Maximum Ratings

Parameter	Symbol	Minimum	Typical	Maximum	Units
Absolute Digital Power Supply Voltage	VDD_ABS	-0.40		1.08	V
Absolute Digital I/O Power Supply Voltage	VDDIOX_ABS	-0.40		3.00	V
Absolute Analog Power Supply Voltage for TBG	VAA_ABS	-0.50		2.16	V
Absolute Input Voltage	VIN_ABS	-0.40		3.96	V
Absolute Storage Temperature	T_STORE_ABS	-55		85	C
Absolute Junction Temperature	T_JUNC_ABS	0		125	C

CAUTION: Exposure to conditions at or beyond the maximum rating may damage the device. Operation beyond the recommended operating conditions (Table 5-3) is neither recommended nor guaranteed.

Note: Before designing a system, it is recommended that you read application note AN-63: *Thermal Management for Marvell Technology Products*. This application note presents basic concepts of thermal management for integrated circuits (ICs) and includes guidelines to ensure optimal operating conditions for Marvell Technology's products.

5.3 Recommended Operating Conditions

Table 5-3 defines the Recommended Operating Conditions for the 88SE1475.

Table 5-3 Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units
Ambient Operating Temperature	N/A	0	N/A	70	C
Operating Digital Power Supply Voltage	VDD_OP	0.90	0.95	1.00	V
Operating Digital I/O Pad Supply Voltage	VDDIOX_OP	2.38	2.50	2.63	V
Operating Analog Power Supply Voltage	VAA_OP	1.71	1.80	1.89	V

CAUTION: Operation beyond the recommended operating conditions is neither recommended nor guaranteed.

Note: The heat sink and effective air flow are needed to ensure that the chip properly works.

5.4 DC Electrical Characteristics

Table 5-4 defines the DC Electrical Characteristics for the 88SE1475.

Table 5-4 DC Electrical Characteristics

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Input Low Voltage	V_IL	N/A	-0.4	N/A	0.3 × VDDIO	V
Input High Voltage	V_IH	N/A	0.7 × VDDIO	N/A	1.1 × VDDIO	V
Output Low Current, Digital I/O	I_OL	VDDIO = 0.4V	8	N/A	N/A	mA
Output High Current, Digital I/O	V_OH	VDDIO = 0.4V	8	N/A	N/A	mA

CAUTION: Operation beyond the recommended operating conditions is neither recommended nor guaranteed.

5.5 Thermal Data

It is recommended to read application note *AN-63 Thermal Management for Selected Marvell® Products* (Document Number MV-S300281-00) and the *ThetaJC, ThetaJA, and Temperature Calculations White Paper*, available from Marvell, before designing a system. These documents describe the basic understanding of thermal management of integrated circuits (ICs) and guidelines to ensure optimal operating conditions for Marvell products.

Note: In addition to the heat sink requirement, airflow is required to assist the thermal dissipation.

Table 5-5 provides the thermal data for the 88SE1475. The simulation was performed according to JEDEC standards.

All data is based on parts mounted on 4 inches × 4.5 inches JEDEC 6L PCB.

Table 5-5 Package Thermal Data

Parameter	Definition	Airflow Value			
		0 m/s	1 m/s	2 m/s	3 m/s
θ_{JA}	Thermal Resistance: Junction To Ambient	12.5 C/W	10.6 C/W	9.7 C/W	9.1 C/W
Ψ_{JB}	Thermal Characterization Parameter: Junction to Bottom Surface Center of the Package.	6.8 C/W	N/A	N/A	N/A
ψ_{JT}	Thermal Characterization Parameter: Junction to top Center	0.9 C/W	N/A	N/A	N/A

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