88SE9345 R3.3

Four-Lane PCIe 2.0 to Four-Port SATA 6 Gbps RAID I/O Controller

Preliminary Datasheet

Doc No. MV-S109418-00 Rev. A

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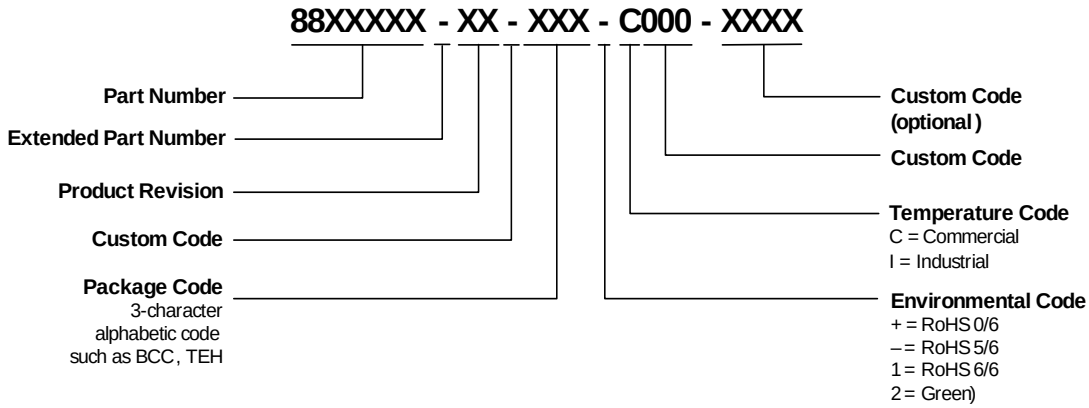
ORDERING INFORMATION

Ordering Part Numbers and Package Markings

The following figure shows the ordering part numbering scheme for the 88SE9345 part. For complete ordering information, contact your Marvell FAE or sales representative.

Sample Ordering Part Number



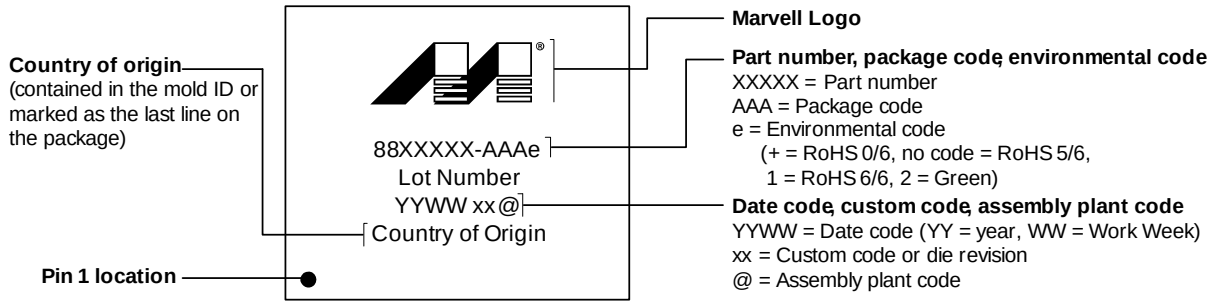
The standard ordering part numbers for the respective solutions are indicated in the following table.

Ordering Part Numbers

Part Number	Description
88SE9345C3-BMJ2C000	481-Ball TFBGA 19 × 19 mm This product does not support Marvell RAID stack.

The next figure shows a typical Marvell package marking.

88SE9345 Package Marking and Pin 1 Location



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CHANGE HISTORY

The following table identifies the document change history for Rev. A.

Document Changes *

Location	Type	Description	Date
Page 1-1	Update	Updated the description for chapter 1, Overview: from The 88SE9345 is a four-port, 6.0 Gbps SATA controller that provides a one- or four-lane PCIe 2.0 host interface, and supports advanced RAID topologies. The 88SE9xx5 is similar to the 88SE9xx0, but does not support the Marvell RAID stack. to The 88SE9345 is a four-port, 6.0 Gbps SATA controller that provides a one-, two-, or four-lane PCIe 2.0 host interface, and supports advanced RAID topologies. The 88SE9xx5 is similar to the 88SE9xx0, but does not support the Marvell RAID stack.	December 8, 2014
Page 2-2	Update	Updated the description for section 2.1, General.	December 5, 2014
Page 3-5	Update	Updated Table 3-1, Signal Type Definitions.	December 8, 2014
Page 3-8	Update	Updated the description for PIN_TEST[9:8] in Table 3-2, General Purpose I/O Signals: from PIN_TEST[9:8]–PCIe maximum lane width **0h:** x8 **1h:** x1 **2h:** x4 **3h:** x8 to PIN_TEST[9:8]–PCIe maximum lane width **0h:** x8 ***Note:*** *Always use 0h.*	January 14, 2015
Page 4-2	Update	Added notes for the following schematics in section 4.1, 88SE9345 Board Schematics: • 88SE9345 Example Board Schematic (1 of 4) • 88SE9345 Example Board Schematic (2 of 4) • 88SE9345 Example Board Schematic (3 of 4) • 88SE9345 Example Board Schematic (4 of 4)	June 27, 2014

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Document Changes * (continued)

Location	Type	Description	Date
Page 5-4	Parameter	Updated Table 5-3, DC Electrical Characteristics: • Updated Analog Power for PCIe PHY 1.8V. • Updated Analog Power for SATA PHY 2.5V, Chip PLL. • Updated Digital Core Power. • Updated Digital I/O Power. • Corrected the Maximum value of Input Low Voltage of Digital I/O from 0.8 to 0.3 × VDDOx. • Corrected the Minimum value of Input High Voltage of Digital I/O from 2.0 to 0.7 × VDDOx. • Corrected the Maximum value of Input High Voltage of Digital I/O from 3.6 to VDDOx + 0.4. • Corrected the Typical value of Output High Voltage of Digital I/O from VDDO1/VDDO2 to VDDOx.	December 18, 2014
Page 5-5	Update	Updated the description for section 5.4, Thermal Data: from Table 5-5 shows the values for the package thermal parameters for the 484-pin TFBGA mounted on a 4-layer PCB. to Table 5-5 shows the values for the package thermal parameters for the 481-ball TFBGA mounted on a 4-layer PCB.	December 4, 2014

* The type of change is categorized as: Parameter, Revision, or Update. A Parameter change is a change to a spec value, a Revision change is one that originates from the chip Revision Notice, and an Update change includes all other document updates.

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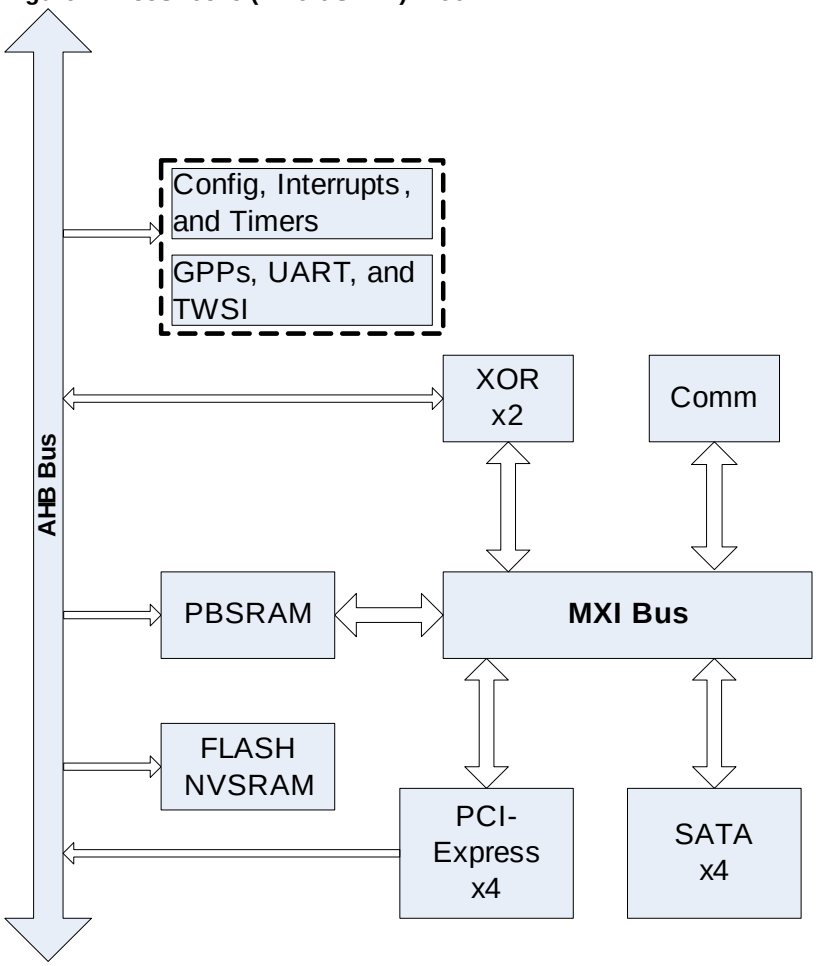
1 OVERVIEW

The 88SE9345 is a four-port, 6.0 Gbps SATA controller that provides a one-, two-, or four-lane PCIe 2.0 host interface, and supports advanced RAID topologies. The 88SE9xx5 is similar to the 88SE9xx0, but does not support the Marvell RAID stack.

The 88SE9345 controller brings a high-performance, low-cost 6.0 Gbps per port SATA solution to HBA, workstation, and server designs utilizing a one- or four-lane PCIe 2.0 interface. The 88SE9345 integrates four high-performance SATA PHYs and a self-configuring four-lane PCIe core. Each of the four PHYs is capable of 1.5 Gbps, 3.0 Gbps, and 6.0 Gbps SATA link rates. The controller supports the SATA protocol defined in the Serial ATA, Revision 3.0 Specification.

Figure 1-1 shows the system block diagram.

Figure 1-1 88SE9345 (4-Port SATA) Block



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2 FEATURES

The chapter contains the following sections:

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2.1 General

- Four SATA ports.
- Choice of x1, x2, or x4 lane PCIe 2.0 host interface.
- Supports three Serial Device Bus (I2C) controllers for communicating with hardware monitoring ICs.
- Supports two industry standard 57600 UARTs.
- Supports two SFF-8485 compliant SGPIO ports.
- Up to 2048 concurrent I/O operations.
- Up to 64 concurrent SATA Devices.
- No hardware limit on the number of SAS devices supported.
- 55 nm CMOS process, 1.0V digital core, 2.5V analog power supply, and 3.3V I/O supply.
- Estimated power (4-port):
  - Minimum = 3.0W
  - Typical = 3.93W
  - Maximum = 5.7W
- Up to 34 LED/GPIO ports.
- Supports hardware RAID 5 and RAID 6 acceleration.
- Supports Data Path Parity Protection (DPP).

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2.2 PCIe

- Supports x1, x2, or x4 lane PCIe 2.0 Interface (5.0 Gbps).
- Supports four fully independent PCIe functions.
- Supports independent interrupt mechanisms for each PCIe function.
- Supports Message Signal Interrupts (MSI).
- All registers memory mapped.
- Supports PCIe Power Management: D0, D1, $D3_{COLD}$, $D3_{HOT}$.

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2.3 SATA

- Serial ATA Revision 3.0 (6 Gbps) compliant, with speed negotiation to 3.0 Gbps and 1.5 Gbps.
- Supports programmable SATA signaling levels, including Gen1x, Gen2i, and Gen2x.
- Supports ATA and ATAPI commands.
- Supports Native Command Queuing (NCQ).
  - Non-zero offset and non-sequential data delivery.
  - 32 outstanding commands per device.
- Supports Port Multiplier.
  - FIS based Switching on NCQ and legacy commands.
- Supports Host mode and Device mode of operation.
- Supports hardware assisted Scatter-Gather.

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2.4 XOR Engine

- Supports Advanced RAID features including:
  - Dual XOR RAID 6.
  - P + Q + Copy, or Q + Q + Q RAID 6.
  - Memory Block Fill.
  - Zero Result Check.
- Generates up to 3 checksums concurrently, including any combination of P and Q.
- Independent GF Multiply coefficient for each of 3 concurrent Q checksum calculations.
- Supports rebuilding three failed drives simultaneously with a single read of remaining good drives.
- Supports chained XOR Descriptor Tables, with up to 32 operations in each table.
- Supports Scatter-Gather transfers using a common PRD format.
- Supports CRC32 checksum generation and checking.

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2.5 Peripherals

- Supports up to 4 MB of external NVSRAM memory (x8/x16).
- Supports up to 4 MB of external PBSRAM memory (x32).
- Supports up to 8 MB of external Parallel Flash memory (x8/x16).
- Supports up to 16 MB of external SPI Flash memory.

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3 PACKAGE

This chapter contains the following sections:

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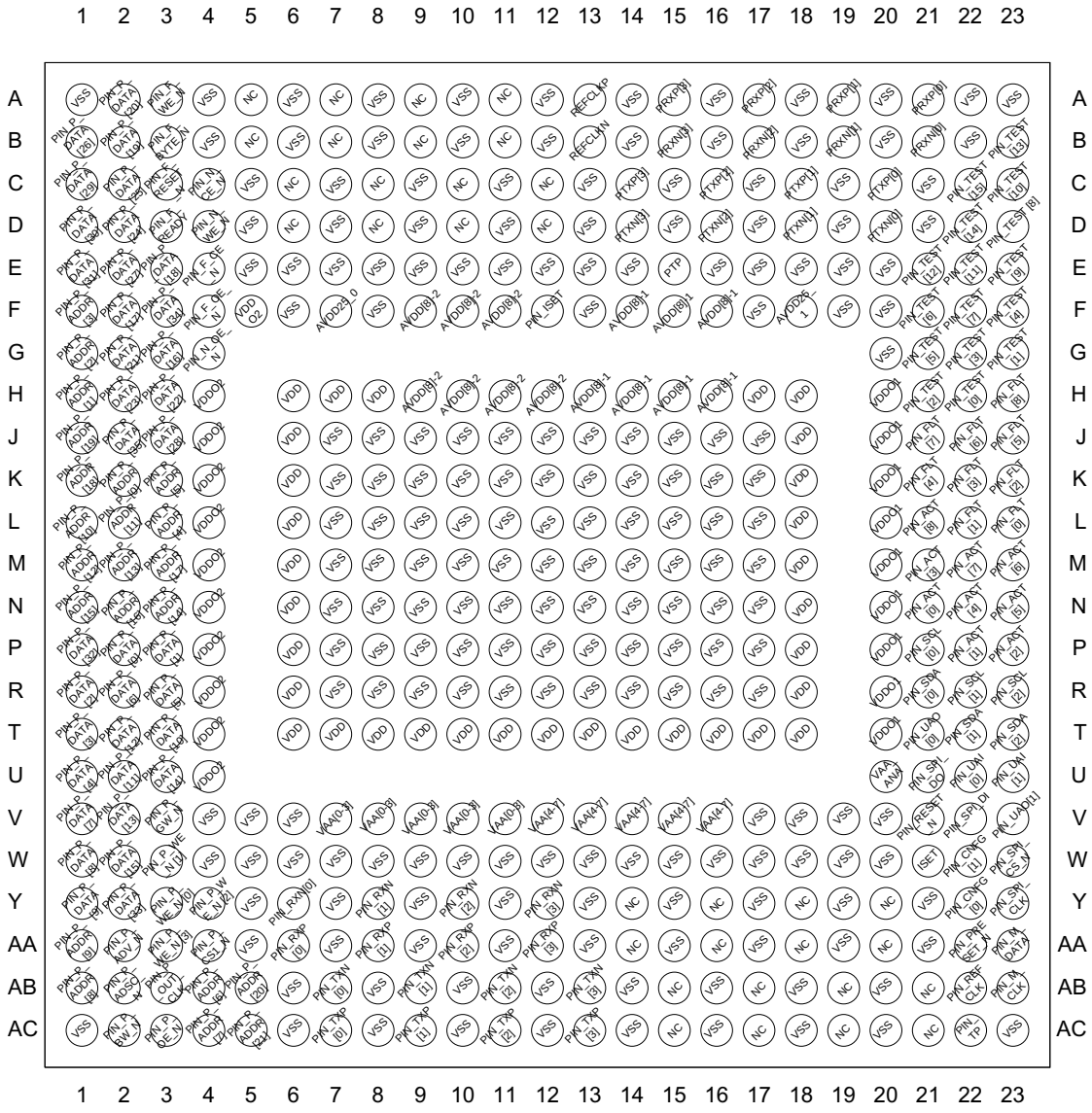
3.1 Ball Diagram

The 481-pin TFBGA ball diagram is illustrated in Figure 3-1.

Figure 3-1 Ball Diagram



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3.2 Mechanical Dimensions

The package mechanical drawing is shown in Figure 3-2 and the mechanical dimensions are shown in Figure 3-2.

Figure 3-2 Package Mechanical Drawing (BMJ)

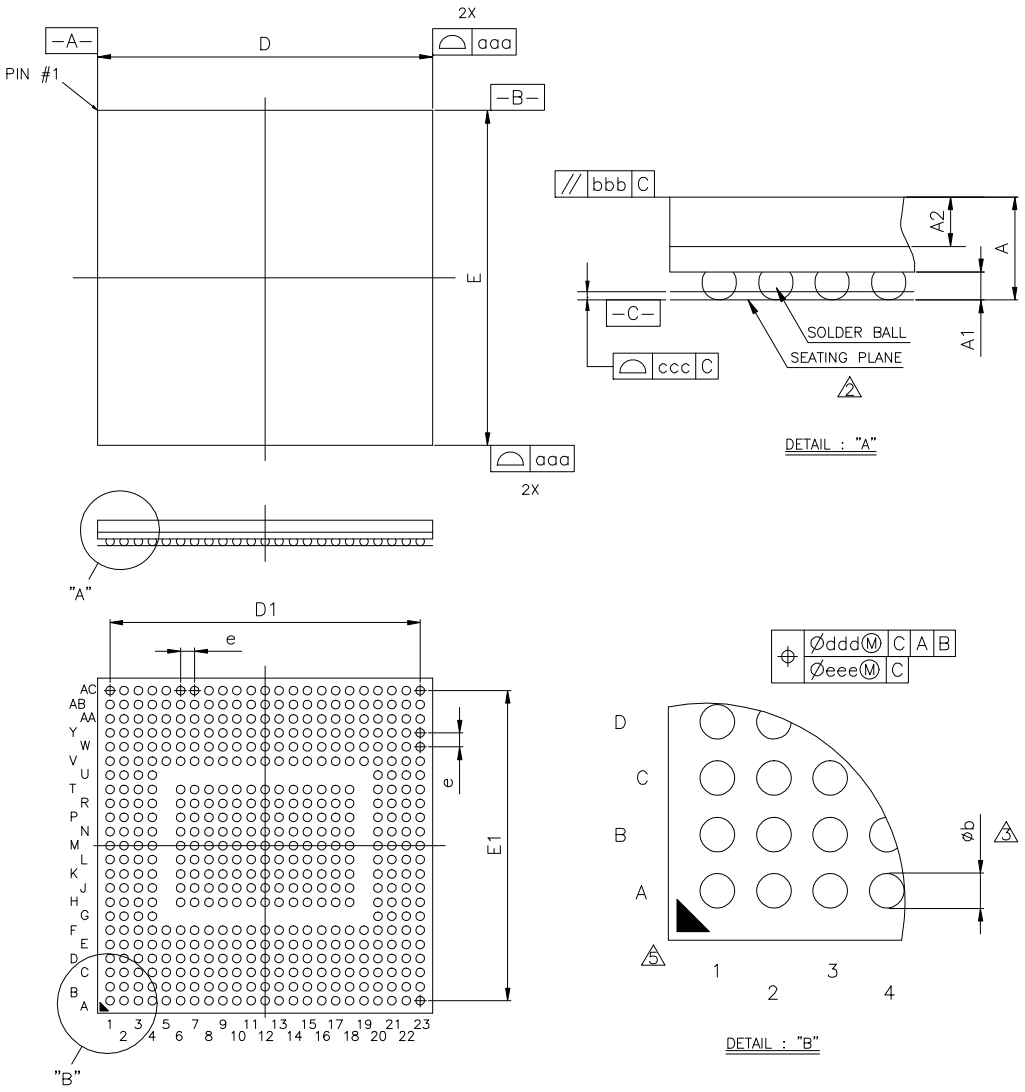

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Figure 3-3 Package Mechanical Dimensions (BMJ)

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.40	1.50	1.60	0.055	0.059	0.063
A1	0.35	0.40	0.45	0.014	0.016	0.018
A2	0.69	0.70	0.71	0.027	0.028	0.028
D/E	18.90	19.00	19.10	0.744	0.748	0.752
D1/E1	---	17.60	---	---	0.693	---
e	---	0.80	---	---	0.031	---
b	0.45	0.50	0.55	0.018	0.020	0.022
aaa	0.12			0.005		
bbb	0.15			0.006		
ccc	0.15			0.006		
ddd	0.15			0.006		
eee	0.10			0.004		

NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM OPENING DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
5. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.

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3.3 Signal Descriptions

This section includes information on signal definitions and descriptions:

- Signal Definitions
- Signal Descriptions

3.3.1 Signal Definitions

Signal type definitions are shown in Table 3-1.

Table 3-1 Signal Type Definitions

Signal Type	Definition
I/O	Input and output
I	Input only
O	Output only
OC	Open Collector
OD	Open-Drain pad
Ground	Ground
Power	Power
NC	No Connect*
DNC	Do Not Connect†
N/A	Not Applicable

* Pin is floating and is not connected internally to any active circuitry nor has any electrical continuity to any other pin

† Device pin to which there may or may not be an internal connection, but to which no external connections are allowed.

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3.3.2 Signal Descriptions

This section outlines the 88SE9345 signal descriptions. Signals ending with the letter “N” are active-low signals.

Table 3-2 General Purpose I/O Signals

Signal Name	Signal Number	Type	Description
PIN_ACT[8]	L21	I/O, OC	Activity LED.
PIN_ACT[7]	M22		Active low.
PIN_ACT[6]	M23		PIN_ACT is active when SATA PHY is transmitting or receiving.
PIN_ACT[5]	N23		
PIN_ACT[4]	N22		These pins can be used as GPIO.
PIN_ACT[3]	M21		PIN_ACT[3:0]–SATA PHY[3:0] activity.
PIN_ACT[2]	P23		PIN_ACT[7:4]—Not used.
PIN_ACT[1]	P22		PIN_ACT[8]–Global Activity. Enabled when any SATA PHY is active.
PIN_ACT[0]	N21		

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Table 3-2 General Purpose I/O Signals (continued)

Signal Name	Signal Number	Type	Description
PIN_FLT[8]	H23	I/O, OC	Fault LED.
PIN_FLT[7]	J21		Active low signals.
PIN_FLT[6]	J22		PIN_FLT is active when PHY is not ready or when PHY is ready and there is any PHY related error or connection error.
PIN_FLT[5]	J23		
PIN_FLT[4]	K21		These pins can be used as GPIO, SGPIO, I2C, or FLT_LED. See GPIO_FLT_CFG (R10080h [7:0]) and I2C_SGPIO_FLT_PAD_SEL (R10104h [9:8]).
PIN_FLT[3]	K22		
PIN_FLT[2]	K23		
PIN_FLT[1]	L22		Pins used as Fault LED:
PIN_FLT[0]	L23		• PIN_FLT[8]: Global Fault indication. The indicator is on when any SATA_PHY has a fault. • PIN_FLT[3:0] corresponds to SATA_PHY3 through PHY0.
			Note: *When PHY is not ready, PIN_FLT[7:0] is always on. After the PHY is ready, a fault occurs.*
			Pins used as SGPIO:
			• PIN_FLT[8]: Same as FLT mode. • PIN_FLT[7:4]: SGPIO1 SCLK, SLOAD, SDOUT, SDIN • PIN_FLT[3:0]: SGPIO0 SCLK,SLOAD,SDOUT,SDIN
			Used as I2C:
			• PIN_FLT[8]: Same as FLT Mode • PIN_FLT[7:6]: I2C2 CLK, DATA • PIN_FLT[5:4]: Not used • PIN_FLT[3:2]: I2C1 CLK, DATA • PIN_FLT[1:0]: Not used

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Table 3-2 General Purpose I/O Signals (continued)

Signal Name	Signal Number	Type	Description
PIN_TEST[15]	C22	I/O	Configuration and test pins.
PIN_TEST[14]	D22		These pins can be used as GPIO.
PIN_TEST[13]	B23		PIN_TEST[15]-PCIe power-up disable
PIN_TEST[12]	E21		**0h**: Enable PCIe after power-up **1h:** Disable PCIe after power-up
PIN_TEST[11]	E22		
PIN_TEST[10]	C23		Not applicable to this chip. This signal needs pull-down.
PIN_TEST[9]	E23		PIN_TEST[14:13]–Chip reference clock selection
PIN_TEST[8]	D23		**0h:** 20 MHz **1h:** 50 MHz **2h:** 100 MHz **3h:** 75 MHz
PIN_TEST[7]	F22		
PIN_TEST[6]	F21		
PIN_TEST[5]	G21		
PIN_TEST[4]	F23		PIN_TEST[12:11]–Reserved
PIN_TEST[3]	G22		PIN_TEST[10]–PCIe ROM location
PIN_TEST[2]	H21		**0h:** Parallel Flash **1h:** Serial Flash
PIN_TEST[1]	G23		
PIN_TEST[0]	H22		PIN_TEST[9:8]–PCIe maximum lane width **0h:** x8 *Always use 0h.*PIN_TEST[7:6]–Reserved PIN_TEST[5]—PCIe configuration access enable. **0h:** PCIe responds to configuration access. **1h:** PCIe returns a retry configuration access. Not applicable to this chip. This signal needs pull-down. PIN_TEST[4]–Parallel Flash x8/x16 **0h:** Byte mode **1h:** Word mode PIN_TEST[3:2]–Reserved PIN_TEST[1]–UART baudrate **0h:** 57600 **1h:** Reserved PIN_TEST[0]–UART mode **0h:** Reserved **1h:** Terminal mode

Table 3-3 Clock and Reset Signals

Signal Name	Signal Number	Type	Description
PIN_REFCLK	AB22	I	Reference clock input. 2.5V, ± 350 ppm.
PIN_RESET_N	V21	I	Power-on reset.

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Table 3-3 Clock and Reset Signals (continued)

Signal Name	Signal Number	Type	Description
PIN_PRESET_N	AA22	I	PCIe Reset
PIN_TP	AC22	O	SATA analog test port.

Table 3-4 I2C Signals

Signal Name	Signal Number	Type	Description
PIN_SCL[2]	R23	I/O, OC	I2C clock.
PIN_SCL[1]	R22		
PIN_SCL[0]	P21		
PIN_SDA[2]	T23	I/O, OC	I2C data.
PIN_SDA[1]	T22		
PIN_SDA[0]	R21		

Table 3-5 UART Signals

Signal Name	Signal Number	Type	Description
PIN_UAI[1]	U23	I	UART input.
PIN_UAI[0]	U22		
PIN_UAO[1]	V23	O	UART output.
PIN_UAO[0]	T21		

.

Table 3-6 Parallel Flash Signals

Signal Name	Signal Number	Type	Description
PIN_F_BYTE_N	B3	O	Parallel flash Byte mode.
PIN_F_CE_N	E4	O	Parallel flash chip select.
PIN_F_OE_N	F4	O	Parallel flash output enable.
PIN_F_READY	D3	I	Parallel flash ready signal. Requires external pull-up resistor.
PIN_F_RESET_N	C3	O	Parallel flash reset.
PIN_F_WE_N	A3	O	Parallel flash write enable.

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Table 3-6 Parallel Flash Signals (continued)

Signal Name	Signal Number	Type	Description
PIN_P_ADDR[21]	AC5	O	Shared address bus for parallel flash, NVSRAM and PBSRAM. For Parallel Flash, signals are word addresses. For NVSRAM, signals are WORD addresses. For PBSRAM, signals are Dword addresses.
PIN_P_ADDR[20]	AB5		
PIN_P_ADDR[19]	J1		
PIN_P_ADDR[18]	K1		
PIN_P_ADDR[17]	M3		
PIN_P_ADDR[16]	N2		
PIN_P_ADDR[15]	N1		
PIN_P_ADDR[14]	N3		
PIN_P_ADDR[13]	M2		
PIN_P_ADDR[12]	M1		
PIN_P_ADDR[11]	L2		
PIN_P_ADDR[10]	L1		
PIN_P_ADDR[9]	AA1		
PIN_P_ADDR[8]	AB1		
PIN_P_ADDR[7]	AC4		
PIN_P_ADDR[6]	AB4		
PIN_P_ADDR[5]	K3		
PIN_P_ADDR[4]	L3		
PIN_P_ADDR[3]	F1		
PIN_P_ADDR[2]	G1		
PIN_P_ADDR[1]]	H1		
PIN_P_ADDR[0]	K2		

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Table 3-6 Parallel Flash Signals (continued)

Signal Name	Signal Number	Type	Description
PIN_P_DATA[35]	J2	I/O	Shared Data Bus for Parallel Flash/NVSRAM/PBSRAM.
PIN_P_DATA[34]	F3		For Parallel Flash, DATA[15:0] are used.
PIN_P_DATA[33]	Y2		In Byte mode, DATA[15] is address bit 0. DATA[7:0] are data.
PIN_P_DATA[32]	P1		
PIN_P_DATA[31]	E1		In Word mode, DATA[15:0] are data.
PIN_P_DATA[30]	D1		For NVSRAM, DATA[15:0] are used.
PIN_P_DATA[29]	C1		For PBSRAM, DATA[35:0] are used.
PIN_P_DATA[28]	J3		DATA[35] is parity for Byte 3.
PIN_P_DATA[27]	E2		DATA[34] is parity for Byte 2.
PIN_P_DATA[26]	B1		DATA[33] is parity for Byte 1.
PIN_P_DATA[25]	C2		DATA[32] is parity for Byte 0.
PIN_P_DATA[24]	D2		
PIN_P_DATA[23]	H2		
PIN_P_DATA[22]	H3		
PIN_P_DATA[21]	G2		
PIN_P_DATA[20]	A2		
PIN_P_DATA[19]	B2		
PIN_P_DATA[18]	E3		
PIN_P_DATA[17]	F2		
PIN_P_DATA[16]	G3		
PIN_P_DATA[15]	W2		
PIN_P_DATA[14]	U3		
PIN_P_DATA[13]	V2		
PIN_P_DATA[12]	T2		
PIN_P_DATA[11]	U2		
PIN_P_DATA[10]	T3		
PIN_P_DATA[9]	Y1		
PIN_P_DATA[8]	W1		
PIN_P_DATA[7]	V1		
PIN_P_DATA[6]	R2		
PIN_P_DATA[5]	R3		
PIN_P_DATA[4]	U1		
PIN_P_DATA[3]	T1		
PIN_P_DATA[2]	R1		
PIN_P_DATA[1]]	P3		
PIN_P_DATA[0]	P2		

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Table 3-7 NVSRAM Signals

Signal Name	Signal Number	Type	Description
PIN_N_CE_N	C4	O	nvSRAM chip select.
PIN_N_OE_N	G4	O	nvSRAM output enable.
PIN_N_WE_N	D4	O	nvSRAM write enable.

Table 3-8 PBSRAM Signals

Signal Name	Signal Number	Type	Description
PIN_P_ADSC_N	AB2	O	PBSRAM ASDC mode.
PIN_P_ADV_N	AA2	O	PBSRAM address advance.
PIN_P_BW_N	AC2	O	PBSRAM BW.
PIN_P_CS1_N	AA4	O	PBSRAM chip select.
PIN_P_GW_N	V3	O	PBSRAM global write enable.
PIN_P_OE_N	AC3	O	PBSRAM output enable.
PIN_P_OUT_CLK	AB3	O	PBSRAM clock.
PIN_P_WE_N[3]	AA3	O	PBSRAM write enable.
PIN_P_WE_N[2]	Y4		
PIN_P_WE_N[1]	W3		
PIN_P_WE_N[0]	Y3		

Table 3-9 System Interface Signals

Signal Name	Signal Number	Type	Description
PIN_CNFG[1] PIN_CNFG[0]	W22 Y22	I	Configuration. **00:** Normal Functional mode. **Others:**Test Mode.
REFCLKP	A13	I	PCIe reference clock input. 100MHz ± 300ppm.No internal clock termination.
REFCLKN	B13	I	PCIe reference clock input. 100MHz ± 300ppm.No internal clock termination.

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Table 3-10 SPI Interface Signals

Signal Name	Signal Number	Type	Description
PIN_SPI_DI	V22	I	SPI data input.
PIN_SPI_CLK	Y23	O	SPI clock.
PIN_SPI_CS_N	W23	O	SPI chip select.
PIN_SPI_DO	U21	O	SPI data output.

Table 3-11 PCIe Interface Signals

Signal Name	Signal Number	Type	Description
ISET	W21	I/O	Reference Current for PCI-Express PHY. This pin must be connected to an external 6.04 kΩ, 1% resistor to ground.
PIN_ISET	F12	I	Chip reference resistor 5 kΩ.
PTP	E15	O	Analog test port for PCIe.
PIN_M_CLK	AB23	I	PCIe debugging MDIO interface, clock.
PIN_M_DATA	AA23	I/O	PCIe debugging MDIO interface, data.

Table 3-12 SATA Transmitter and Receiver Interface Signals

Signal Name	Signal Number	Type	Description
PIN_RXP[3]	AA12	I	PIN_RXP[3:0]–SATA PHY 3–0 Receiver Differential Signal.
PIN_RXP[2]	AA10		
PIN_RXP[1]	AA8		
PIN_RXP[0]	AA6		
PIN_RXN[3]	Y12	I	PIN_RXN[3:0]–SATA PHY 3–0 Receiver Differential Signals.
PIN_RXN[2]	Y10		
PIN_RXN[1]	Y8		
PIN_RXN[0]	Y6		

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Table 3-12 SATA Transmitter and Receiver Interface Signals (continued)

Signal Name	Signal Number	Type	Description
PIN_TXP[3]	AC13	O	PIN_TXP[3:0]–SATA PHY 3–0 Transmitter Differential Signals.
PIN_TXP[2]	AC11		
PIN_TXP[1]	AC9		
PIN_TXP[0]	AC7		
PIN_TXN[7]	–	O	PIN_TXN[3:0]–SATA PHY 3–0 Transmitter Differential Signals.
PIN_TXN[6]	–		
PIN_TXN[5]	–		
PIN_TXN[4]	–		
PIN_TXN[3]	AB13		
PIN_TXN[2]	AB11		
PIN_TXN[1]	AB9		
PIN_TXN[0]	AB7		

Table 3-13 PCIe Transmitter and Receiver Interface Signals

Signal Name	Signal Number	Type	Description
PRXP[3]	A15	I	PRXP[3:0]–PCI-Express Lane 3–0 Receiver Differential Signal (PCI-Express RX +/-).
PRXP[2]	A17		
PRXP[1]	A19		
PRXP[0]	A21		
PRXN[3]	B15	I	PRXN[3:0]–PCI-Express Lane 3–0 Receiver Differential Signals (PCI-Express RX +/-).
PRXN[2]	B17		
PRXN[1]	B19		
PRXN[0]	B21		
PTXP[3]	C14	O	PTXP[3:0]–PCI-Express Lane 3–0 Transmitter Differential Signals (PCI-Express TX -/+).
PTXP[2]	C16		
PTXP[1]	C18		
PTXP[0]	C20		
PTXN[3]	D14	O	PTXN[3:0]–PCI-Express Lane 3–0 Transmitter Differential Signals (PCI-Express TX -/+).
PTXN[2]	D16		
PTXN[1]	D18		
PTXN[0]	D20		

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Table 3-14 Power Interface Signals

Signal Name	Signal Number	Type	Description
AVDD25_0	F7	Power, I	I/O Pad Power 2.5V.
AVDD25_1	F18	Power, I	I/O Pad Power 2.5V.
AVDD[8]-1	F14, F15, F16. H13, H14, H15, H16	Power, I	1.8V analog power for PCI-Express PHY. AVDD[8] is for PLL and the current source.
AVDD[8]-2	F9, F10, F11, H9, H10, H11, H12	Power, I	1.8V analog power for PCI-Express PHY. AVDD[8] is for PLL and the current source.
VAA[0-3]	V7, V8, V9, V10, V11	Power, I	2.5V analog power for SATA PHY.
VAA[4-7]	V12, V13, V14, V15, V16	Power, I	2.5V analog power for SATA PHY.
VAA_ANA	U20	Power, I	2.5V analog power for PLL.
VDD	H6, H7, H8, H17, H18, J6, J18, K6, K18, L6, L18, M6, M18, N6, N18, P6, P18, R6, R18, T6, T7, T8, T9, T10, T11, T12, T13, T14, T15, T16, T17, T18	Power, I	1.0V digital core power.
VDDO1	H20, J20, K20, L20, M20, N20, P20, R20, T20	Power, I	Digital Power. 3.3V I/O Power to supply digital and I/Os.
VDDO2	F5, H4, J4, K4, L4, M4, N4, P4, R4, T4, U4		

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Table 3-14 Power Interface Signals (continued)

Signal Name	Signal Number	Type	Description
VSS	A1, A4, A6, A8, A10, A12, A14, A16, A18, A20, A22, A23, B4, B6, B8, B10, B12, B14, B16, B18, B20, B22, C5, C7, C9, C11, C13, C15, C17, C19, C21, D5, D7, D9, D11, D13, D15, D17, D19, D21, E5–E14, E16–E20, F6, F8, F13, F17, F19, F20, G20, J7–J17, K7–K17, L7–L17, M7– M17, N7–N17, P7–P17, R7–R17, V4–V6, V17–V20, W4–W20, Y5, Y7, Y9, Y11, Y13, Y15, Y17, Y19, Y21, AA5, AA7, AA9, AA11, AA13, AA15, AA17, AA19, AA21,	Ground	Ground.

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Table 3-14 Power Interface Signals (continued)

Signal Name	Signal Number	Type	Description
VSS	AB6, AB8, AB10, AB12, AB14, AB16, AB18, AB20, AC1, AC6, AC8, AC10, AC12, AC14, AC16, AC18, AC20, AC23	Ground	Ground.

Table 3-15 No Connect Signals

Signal Name		Signal Number	Type	Description
NC	–	A5, A7, A9, A11, B5, B7, B9, B11, C6, C8, C10, C12, D6, D8, D10, D12, Y14, Y16, Y18, Y20, AA14, AA16, AA18, AA20, AB15, AB17, AB19, AB21, AC15, AC17, AC19, AC21	N/A	No Connect

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4 LAYOUT GUIDELINES

This chapter describes the system recommendations from the Marvell Semiconductor design and application engineers who work with the 88SE9345. It is written for those who are designing schematics and printed circuit boards for an 88SE9345-based system. Whenever possible, the PCB designer should try to follow the suggestions provided in this chapter.

The information in this chapter is preliminary. Please consult with Marvell Semiconductor design and application engineers before starting your PCB design.

The chapter contains the following sections:

- 88SE9345 Board Schematics
- Layer Stack-Up
- Power Supply
- PCB Trace Routing
- Recommended Layout

Refer to Chapter 3, Package, for package information.

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4.1 88SE9345 Board Schematics

This section contains the following example board schematics:

- Figure 4-1, 88SE9345 Example Board Schematic (1 of 4)
- Figure 4-2, 88SE9345 Example Board Schematic (2 of 4)
- Figure 4-3, 88SE9345 Example Board Schematic (3 of 4)
- Figure 4-4, 88SE9345 Example Board Schematic (4 of 4)

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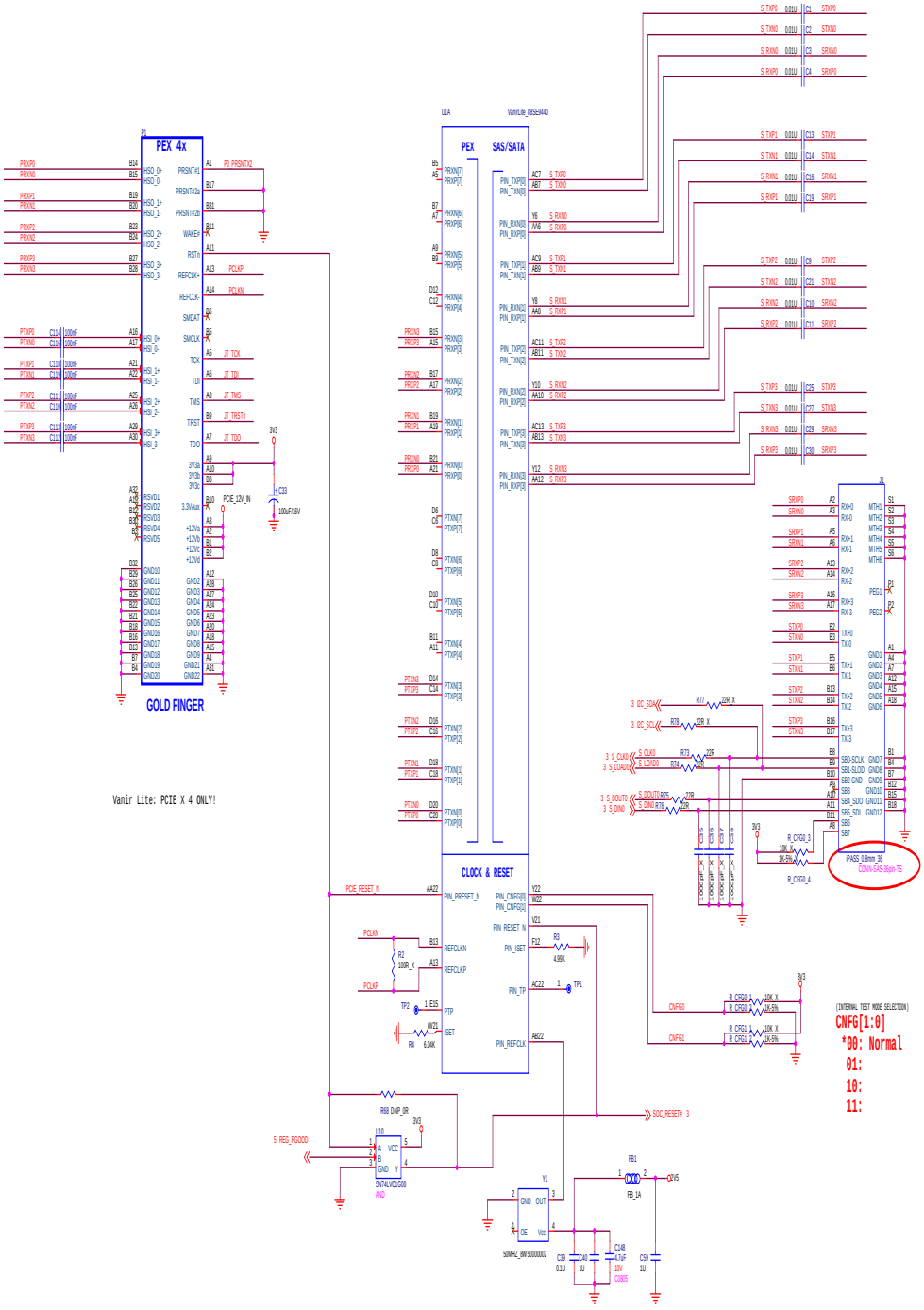
- Figure 4-4, 88SE9345 Example Board Schematic (4 of 4)

Figure 4-1 88SE9345 Example Board Schematic (1 of 4)



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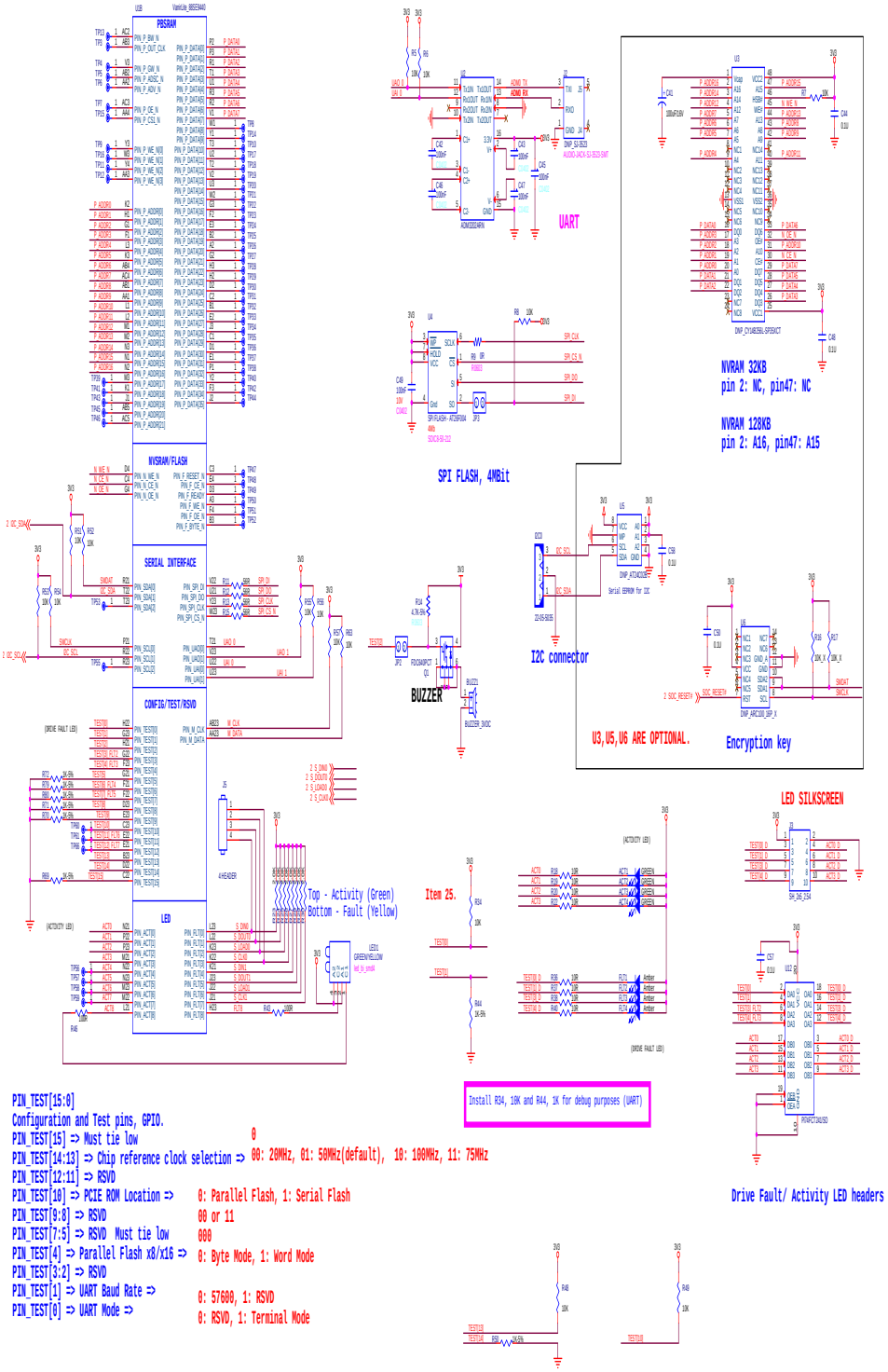
Note: This diagram is for reference only. Contact your Marvell field applications engineer for the latest schematics.

Figure 4-2 88SE9345 Example Board Schematic (2 of 4)



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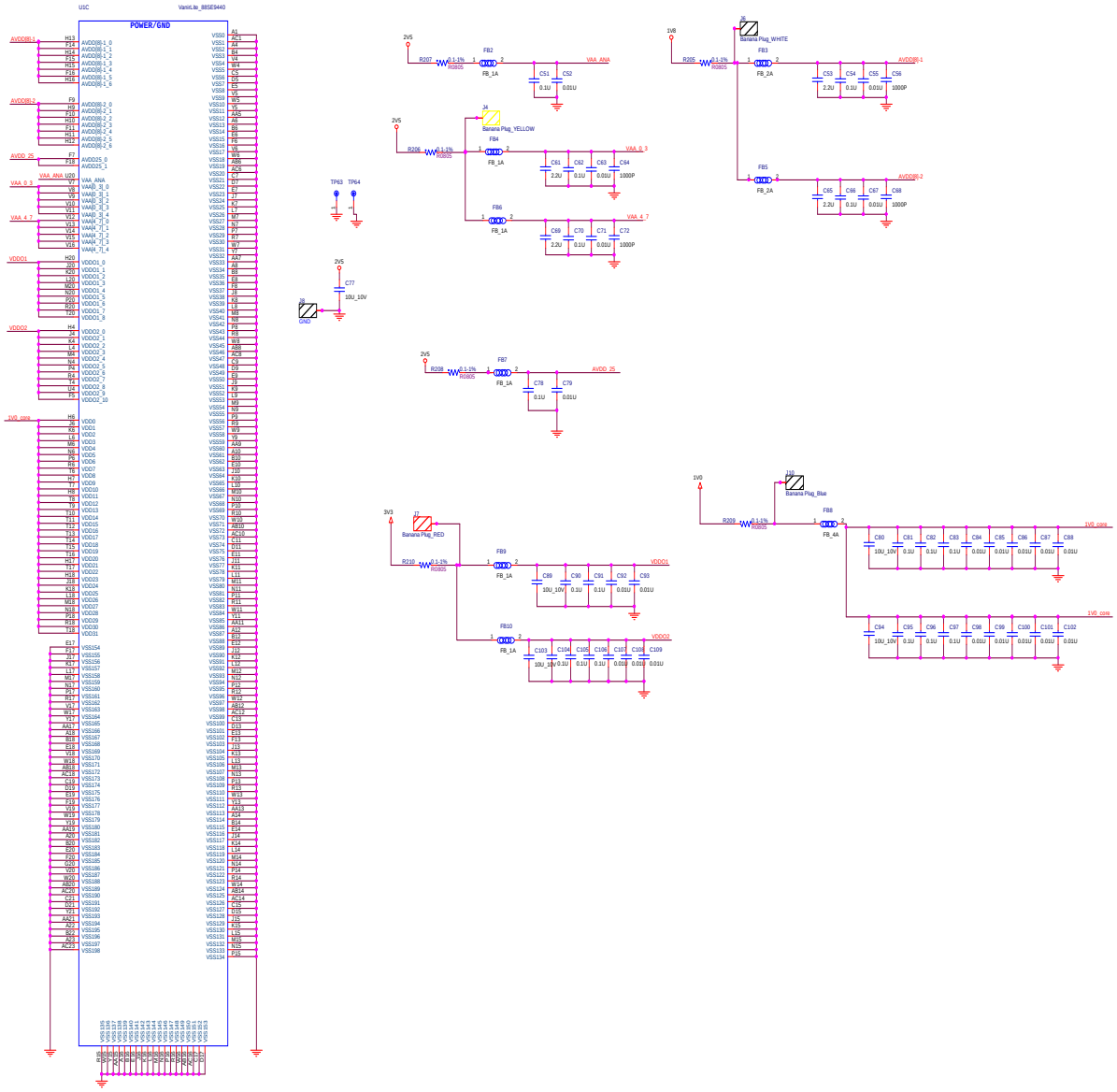
Note: This diagram is for reference only. Contact your Marvell field applications engineer for the latest schematics.

Figure 4-3 88SE9345 Example Board Schematic (3 of 4)



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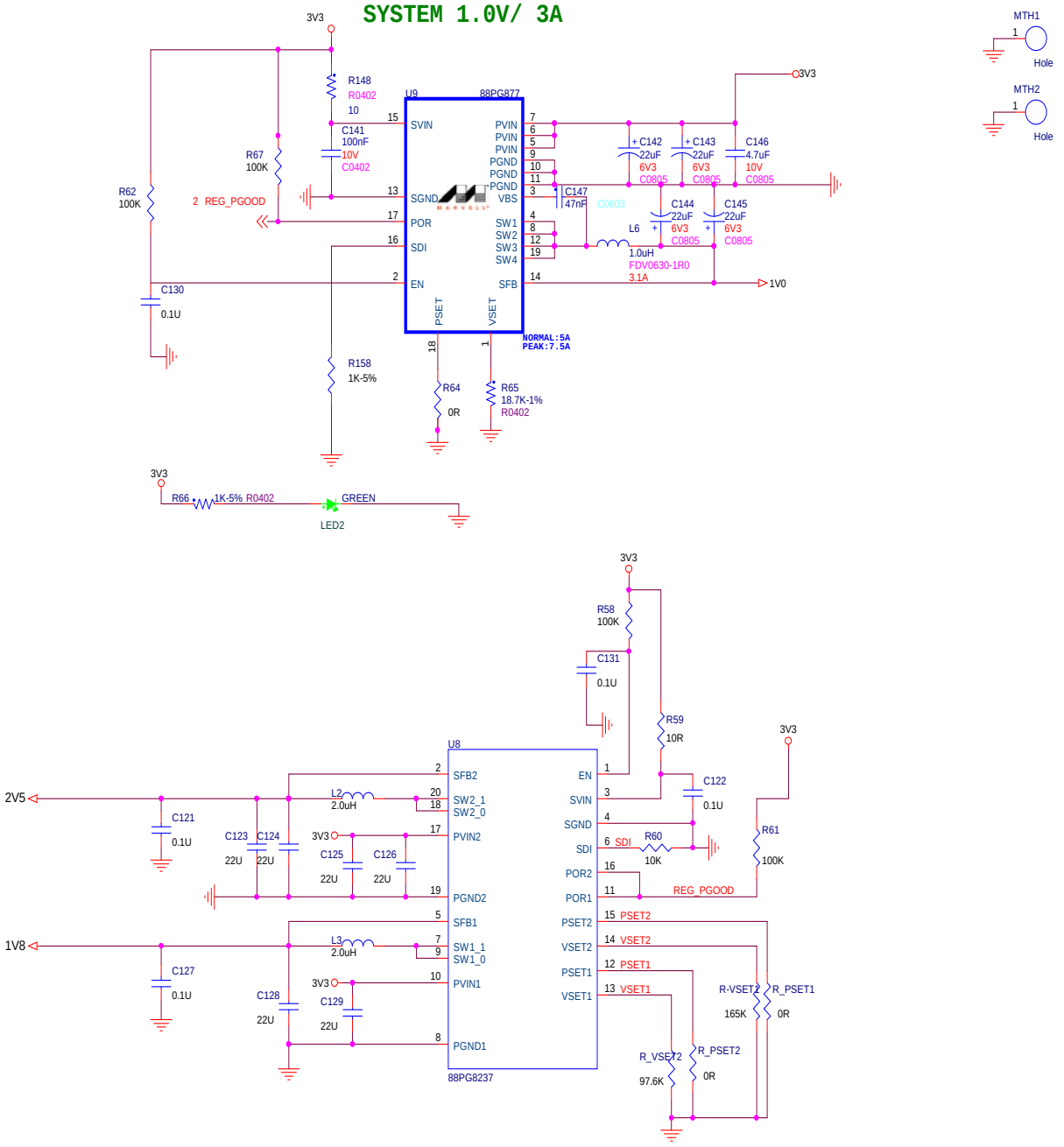
Note: This diagram is for reference only. Contact your Marvell field applications engineer for the latest schematics.

Figure 4-4 88SE9345 Example Board Schematic (4 of 4)



Note: This diagram is for reference only. Contact your Marvell field applications engineer for the latest schematics.

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4.2 Layer Stack-Up

The following layer stack up is recommended

- Layer 1–Topside, Parts, Low and High-Speed Signal Routes, and Power Routes
- Layer 2–Solid Ground Plane
- Layer 3–Power Plane and Low Speed Signals
- Layer 4–Power Plane
- Layer 5–Solid Ground Plane
- Layer 6–Bottom Layer, Low and High-Speed Signal Routes, and Power Routes

5 mil traces and 5 mil spacing are the recommended minimum requirements.

4.2.1 Layer 1–Topside, Parts, Low and High-Speed Signal Routes, and Power Routes

All active parts are to be placed on the topside. Some of the differential pairs for SATA and PCIe are routed on the top layer, differential 100 ohm impedance needs to be maintained for those high-speed signals.

4.2.2 Layer 2–Solid Ground Plane

A solid ground plane should be located directly below the top layer of the PCB. This layer should be a minimum distance below the top layer in order to reduce the amount of crosstalk and EMI. There should be no cutouts in the ground plane. Use of 1 ounce copper is recommended.

4.2.3 Layer 3–Power Plane and Low Speed Signals

Use solid planes on layer 3 to supply power to the ICs on the PCB. Avoid narrow traces and necks on this plane.

4.2.4 Layer 4–Power Plane

Use solid planes on layer 4 to supply power to the ICs on the PCB. Avoid narrow traces and necks on this plane.

4.2.5 Layer 5–Solid Ground Plane

A solid ground plane should be located directly below the top layer of the PCB. This layer should be a minimum distance below the top layer in order to reduce the amount of crosstalk and EMI. There should be no cutouts in the ground plane. Use of 1 ounce copper is recommended.

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4.2.6 Layer 6–Bottom Layer, Low and High-Speed Signal Routes, and Power Routes

Some of the differential pairs for SATA and PCIe are routed on the top layer, differential 100Ω impedance needs to be maintained for those high speed signals.

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4.3 Power Supply

The 88SE9345 operates using the following power supplies:

- VDD Power (1.0V) for the digital core
- PCIe Analog Power Supply (1.8V)
- SATA Analog Power Supply (2.5V)
- General I/O Power (3.3V)

4.3.1 VDD Power (1.0V)

All digital power pins (VDD pins) must be connected directly to a VDD plane in the power layer with short and wide traces to minimize digital power-trace inductances.

Use vias close to the VDD pins to connect to this plane and avoid using the traces on the top layer. Marvell recommends placing capacitors around the three sides of the PCB near VDD pins with the following dimensions:

- 0.001 µF (1 capacitor)
- 0.1 µF (2 capacitors)
- 2.2 µF (1 ceramic capacitor)

The combinations of small capacitors are used to suppress switching noise at various frequency ranges. The 2.2 µF ceramic decoupling capacitor is required to filter the lower frequency power-supply noise.

To reduce system noise, place high-frequency surface-mount monolithic ceramic bypass capacitors as close as possible to the channel VDD pins. Place at least one decoupling capacitor on each side of the IC package.

4.3.2 PCIe Analog Power Supply (1.8V)

The analog supply provides power for the PCIe link's high speed serial signals. To ensure high speed link operation, use a series of bypass capacitors for the supplies. A typical capacitor value combination is 1 nF, 0.1µF, and 2.2 µF.

4.3.3 SATA Analog Power Supply (2.5V)

The analog supply provides power for the SATA link's high speed serial signals. To ensure high speed link operation, use a series of bypass capacitors for the supplies. A typical capacitor value combination is 1 nF, 0.1µF, and 2.2 µF.

4.3.4 General I/O Power (3.3V)

A general I/O power supply provides power to the GPIO, flash and I2C blocks. A stable and clean power source is desired. Use proper bypass capacitors to provide a clean power source with good stability. A typical capacitor value combination is 0.1µF, and 2.2 µF.

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4.3.5 Bias Current Resistor (RSET)

Connect a 6.04KΩ (1%) resistor between the ISET pin and the adjacent top ground plane. This resistor should lie as close as possible to the ISET pin. Avoid routing noisy signals close to the ISET pin.

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4.4 PCB Trace Routing

The stack-up parameters for the reference board are shown in Table 4-1.

Table 4-1 PCB Board Stack-up Parameters

Layer	Layer Description	Copper Weight (oz)	Target Impedance (±10%)
1	Signal	0.5	50
2	GND	1	N/A
3	Power and Signal	1	50
4	Power	1	N/A
5	GND	1	N/A
6	Signal	0.5	50

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4.5 Recommended Layout

High-speed designs must consist of a good board stack-up and careful consideration of the power planes. For the 88SE9345, the following power planes are required:

- VDDIO_C, VDDIO_D, and VDDIO_P power plane (3.3V power source for the digital I/O pins)
- VDD (1.0V power source for the core and digital circuitry)
- VAA (2.5V power source for SATA analog)
- AVDD (1.8V power source for PCIe analog)

Solid ground planes are recommended. However, special care should be taken when routing VAA, AVDD, and VSS pins.

The following general tips describe what should be considered when determining your stack-up and board routing. These tips are not meant to substitute for consulting with a signal-integrity expert or doing your own simulations.

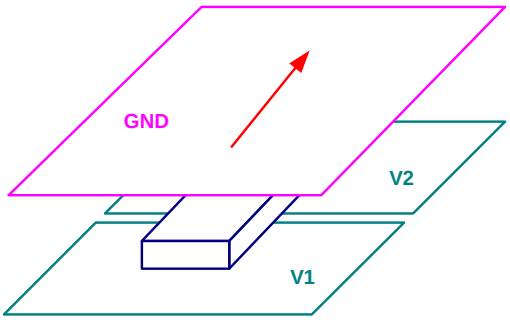
Note: Specific numbers or rules-of-thumb are not used here because they might not be applicable in every situation.

- Do not split ground planes.

  Keep good spacing between possible sensitive analog circuitry on your board and the digital signals to sufficiently isolate noise. A solid ground plane is necessary to provide a good return path for routing layers. Try to provide at least one ground plane adjacent to all routing layers (see Figure 4-5).
- Keep trace layers as close as possible to the adjacent ground or power planes.

  This helps minimize crosstalk and improve noise control on the planes.

Figure 4-5 Trace Has At Least One Solid Plane For Return Path



- When routing adjacent to only a power plane, do not cross splits.

  Route traces only over the power plane that supplies both the driver and the load. Otherwise, provide a decoupling capacitor near the trace at the end that is not supplied by the adjacent power plane.
- Critical signals should avoid running parallel and close to or directly over a gap.

  This would change the impedance of the trace.
- Separate analog powers onto opposing planes.

  This helps minimize the coupling area that an analog plane has with an adjacent digital plane.

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- For dual strip-line routing, traces should only cross at 90 degrees.

  Avoid more than two routing layers in a row to minimize tandem crosstalk and to better control impedance.
- Planes should be evenly distributed in order to minimize warping.
- Calculating or modeling impedance should be made prior to routing.

  This helps ensure that a reasonable trace thickness is used and that the desired board thickness is available. Consult with your board fabricator for accurate impedance.
- Allow good separation between fast signals to avoid crosstalk.

  Crosstalk increases as the parallel traces get longer.
- When packages become smaller, route traces over a split power plane

  Smaller packages force vias to become smaller, thereby reducing board thickness and layer counts, which might create the need to route traces over a split power plane. Some alternatives to provide return path for these signals are listed below.

  Caution must be used when applying these techniques. Digital traces should not cross over analog planes, and vice-versa. All of these rules must be followed closely to prevent noise contamination problems that might arise due to routing over the wrong plane.

  By tightly controlling the return path, control noise on the power and ground planes can be controlled.

  - Place a ground layer close enough to the split power plane in order to couple enough to provide buried capacitance, such as SIG-PWR-GND (see Figure 4-6). Return signals that encounter splits in this situation simply jumps to the ground plane, over the split, and back to the other power plane. Buried capacitance provides the benefit of adding low inductance decoupling to your board. Your fabricator may charge for a special license fee and special materials. To determine the amount of capacitance your planes provide, use the following equation:

    $$C = 1.249 \bullet 10^{-13} \bullet E_r \bullet L \bullet W / H$$

    Where E_R is the dielectric coefficient, L • W represents the area of copper, and H is the separation between planes.
  - Provide return-path capacitors that connect to both power planes and jumps the split. Place them close to the traces so that there is one capacitor for every four or five traces. The capacitors would then provide the return path (see Figure 4-7).
  - Allow only static or slow signals on layers where they are adjacent to split planes.

Figure 4-6 shows the ground layer close to the split power plane.

Figure 4-6 Close Power and Ground Planes Provide Coupling For Good Return Path

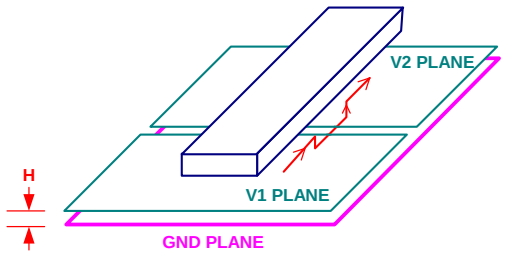

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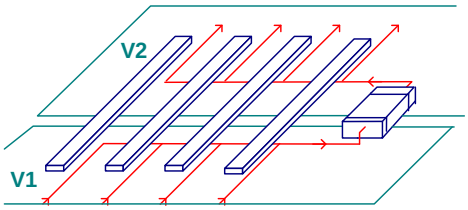
Figure 4-7 shows the thermal ground plane in relation to the return-path capacitor.

Figure 4-7 Suggested Thermal Ground Plane On Opposite Side of Chip



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5 ELECTRICAL SPECIFICATIONS

This chapter contains the following sections:

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5.1 Absolute Maximum Ratings

Table 5-1 Absolute Maximum Ratings

Parameter	Symbol	Minimum	Typical	Maximum	Units
Absolute Analog Power for PCIe PHY	AVDD[8:0]	1.62	1.8	1.98	V
Absolute Analog Power for SATA PHY, Chip PLL	VAA[7:0], VAA_ANA	2.25	2.5	2.75	V
Absolute Power for Digital Core	VDD	0.9	1.0	1.1	V
Absolute Digital I/O Power	VDDO1/VDDO2	3	3.3	3.6	V

CAUTION: Exposure to conditions at or beyond the maximum rating may damage the device. Operation beyond the recommended operating conditions (Table 5-2) is neither recommended nor guaranteed.

Note: Before designing a system, it is recommended that you read application note AN-63: *Thermal Management for Marvell Technology Products*. This application note presents basic concepts of thermal management for integrated circuits (ICs) and includes guidelines to ensure optimal operating conditions for Marvell Technology's products.

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5.2 Recommended Operating Conditions

Table 5-2 Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units
Analog Power for PCIe PHY	AVDD[8:0]	1.71	1.8	1.89	V
Analog Power for SATA PHY, Chip PLL	VAA[7:0], VAA_ANA	2.38	2.5	2.63	V
Digital Core Power	VDD	0.95	1.0	1.05	V
Digital I/O Power	VDDO1/VDDO2	3.14	3.3	3.47	V
Internal Bias Reference	ISET, PIN_ISET	5.74	6.04	6.34	KΩ
Ambient Operating Temperature	T_A	0	N/A	70	°C
Junction Operating Temperature	T_J	0	N/A	125	°C

CAUTION: Operation beyond the recommended operating conditions is neither recommended nor guaranteed.

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5.3 DC Electrical Characteristics

Table 5-3 DC Electrical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Units
Analog Power for PCIe PHY 1.8V	I_{AVDD}	0.19	0.215	0.24	A
Analog Power for SATA PHY 2.5V, Chip PLL	I_{VAA}	0.55	0.62	0.69	A
Digital Core Power	I_{VDD}	1.5	1.94	2.93	A
Digital I/O Power	I_{VDDO}	9.2	10.5	11.6	mA
Input Low Voltage of Digital I/O	V_{IL}	-0.4	N/A	0.3 × VDDOx	V
Input High Voltage of Digital I/O	V_{IH}	0.7 × VDDOx	N/A	VDDOx + 0.4	V
Output Low Voltage of Digital I/O	V_{OL}	N/A	0.13	N/A	V
Output High Voltage of Digital I/O	V_{OH}	2.0	VDDOx*	N/A	V

* VDDOx: VDDO1/VDDO2.

CAUTION: Operation beyond the recommended operating conditions is neither recommended nor guaranteed.

Table 5-4 shows the internal pull-up and pull-down strength.

Table 5-4 Internal Pull-Up and Pull-Down Strength

Specifications	Condition	Minimum	Nominal	Maximum	Unit
Pull-Up Strength	V(PAD) = 0.5 × VDDO	10	N/A	50	µA
	V(PAD) = 0	10	N/A	65	µA
Pull-Down Strength	V(PAD) = 0.5 × VDDO	10	N/A	50	µA

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5.4 Thermal Data

It is recommended to read application note *AN-63 Thermal Management for Selected Marvell® Products* (Document Number MV-S300281-00) and the *ThetaJC, ThetaJA, and Temperature Calculations White Paper*, available from Marvell, before designing a system. These documents describe the basic understanding of thermal management of integrated circuits (ICs) and guidelines to ensure optimal operating conditions for Marvell products.

Table 5-5 provides the thermal data for the 88SE9345. The simulation was performed according to JEDEC standards. The heat sink is 25.4 mm × 25.4 mm × 25 mm.

Table 5-5 shows the values for the package thermal parameters for the 481-ball TFBGA mounted on a 4-layer PCB.

Table 5-5 Package Thermal Data, 4-Layer PCB*

Parameter	Definition	Airflow Value			
		0 m/s	1 m/s	2 m/s	3 m/s
θ_{JA}	Thermal resistance: junction to ambient (no heat sink)	16.2 C/W	13.9 C/W	13.0 C/W	12.6 C/W
θ_{JA}	Thermal resistance: junction to ambient (with heat sink)	11.7 C/W	8.4 C/W	7.8 C/W	7.6 C/W
θ_{JC}	Thermal resistance: junction to case	5.30 C/W	N/A	N/A	N/A

* All data is based on parts mounted on a 4” x 4.5” JEDEC 4L PCB.

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5.5 AC Timing

This section discusses the following topics:

- SATA
- PCIe
- Parallel Flash and NVSRAM

5.5.1 SATA

This product conforms to AC timing requirements as specified in the *Serial ATA Revision 3.0 Specification* (www.sata-io.org).

5.5.2 PCIe

This product conforms to AC timing requirements as specified in the *PCIe® Base 2.0* specification (www.pcisig.com/).

5.5.3 Parallel Flash and NVSRAM

This section describes the timing for Parallel Flash and NVSRAM.

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Figure 5-1 illustrates the Parallel Flash and NVSRAM Read timing, and Table 5-6 provides parameter information for the timing diagram.

Figure 5-1 Parallel Flash / NVSRAM Read Timing

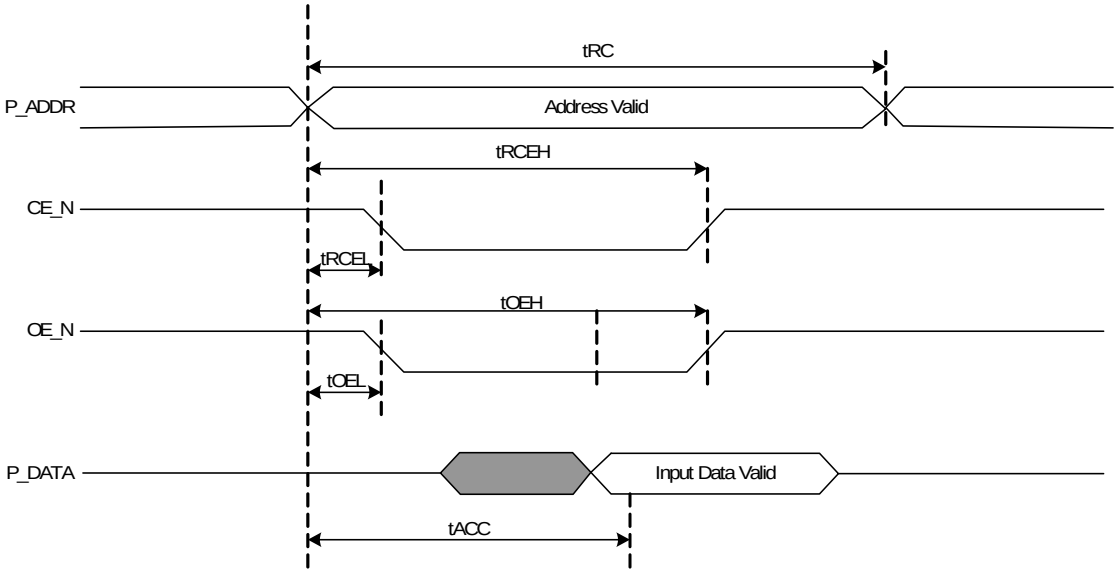

Table 5-6 Timing Parameters for Figure 5-1, Parallel Flash / NVSRAM Read Timing

Parameter	Description	NVSRAM	Parallel Flash	Unit
tRC	Read Cycle Time	(NV_RD_CYCLE_TM (R0C968h [7:0]) + 2) × Tclk	(FLSH_RD_CYCLE_TM (R0C978h [7:0]) + 2) × Tclk	ns
tRCEL	Read CE Assert Time	(NV_RD_CE_ASSRT_TM (R0C96Ch [23:16]) + 1) × Tclk	(FLSH_RD_CE_ASSRT_TM (R0C97Ch [23:16]) + 1) × Tclk	ns
tRCEH	Read CE Deassert Time	(NV_RD_CE_DEASSRT_TM (R0C96Ch [31:24]) + 2) × Tclk	(FLSH_RD_CE_DEASSRT_TM (R0C97Ch [31:24]) + 2) × Tclk	ns
tOEL	Read OE Assert Time	(NV_RD_OE_ASSRT_TM (R0C96Ch [7:0]) + 1) × Tclk	(FLSH_RD_OE_ASSRT_TM (R0C97Ch [7:0]) + 1) × Tclk	ns
tOEH	Read OE Deassert Time	(NV_RD_OE_DEASSRT_TM (R0C96Ch [15:8]) + 2) × Tclk	(FLSH_RD_OE_DEASSRT_TM (R0C97Ch [15:8]) + 2) × Tclk	ns
tACC	Read Data Latch Time	(NV_RD_DATA_LTCH_TM (R0C968h [15:8]) + 1) × Tclk - 20	(FLSH_RD_DATA_LTCH_TM (R0C978h [15:8]) + 1) × Tclk - 20	ns

Note: Tclk—Internal system clock cycle, default value is 3.33ns.

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Figure 5-2 illustrates the Parallel Flash and NVSRAM Write timing, and Table 5-7 provides parameter information for the timing diagram.

Figure 5-2 Parallel Flash / NVSRAM Write Timing

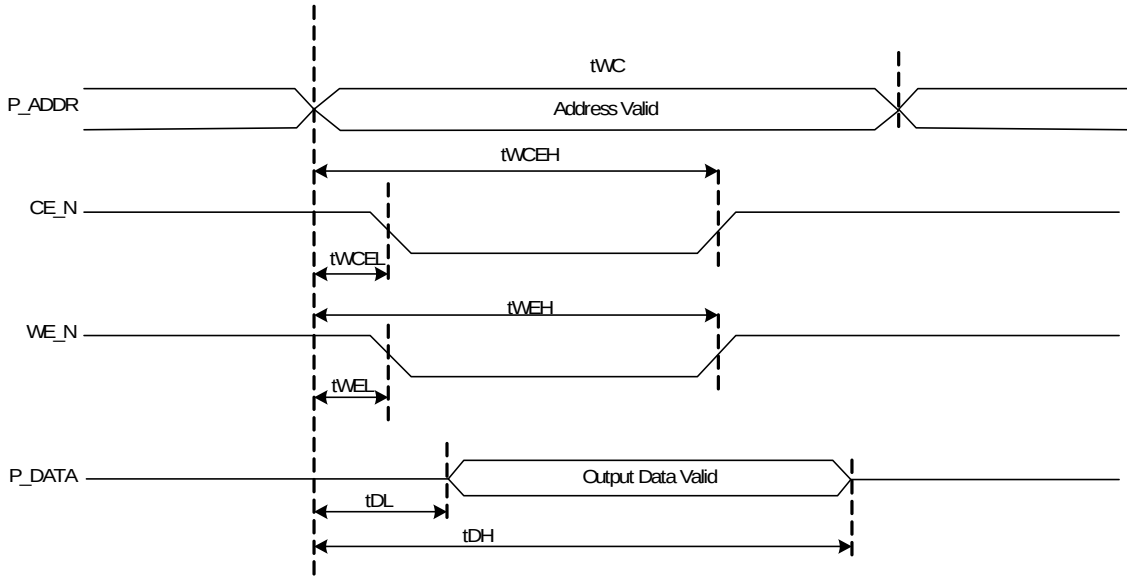

Table 5-7 Timing Parameters for Figure 5-1, Parallel Flash / NVSRAM Read Timing

Parameter	Description	NVSRAM	Parallel Flash	Unit
tWC	Write Cycle Time	(NV_WRT_CYCLE_TM (R0C960h [7:0]) + 2) × Tclk	(FLSH_WRT_CYCLE_TM (R0C970h [7:0]) + 2) × Tclk	ns
tWCEL	Write CE Assert Time	(NV_CE_ASSRT_TM (R0C960h [15:8]) + 1) × Tclk	(FLSH_CE_ASSRT_TM (R0C970h [15:8]) + 1) × Tclk	ns
tWCEH	Write CE Deassert Time	(NV_CE_DEASSRT_TM (R0C960h [23:16]) + 2) × Tclk	(FLSH_CE_DEASSRT_TM (R0C970h [23:16]) + 2) × Tclk	ns
tWEL	Write WE Assert Time	(NV_WRT_WE_ASSRT_TM (R0C964h [7:0]) + 1) × Tclk	(FLSH_WRT_WE_ASSRT_TM (R0C974h [7:0]) + 1) × Tclk	ns
tWEH	Read WE Deassert Time	(NV_WRT_WE_DEASSRT_TM (R0C964h [15:8]) + 2) × Tclk	(FLSH_WRT_WE_DEASSRT_TM (R0C974h [15:8]) + 2) × Tclk	ns
tDL	Write Data IO Enable Time	(NV_WRT_DATA_IO_EN_TM (R0C964h [23:16]) + 1) × Tclk	(FLSH_WRT_DATA_IO_EN_TM (R0C974h [23:16]) + 1) × Tclk	ns
tDH	Write Data IO Disable Time	(NV_WRT_DATA_IO_DSBL_TM (R0C964h [31:24]) + 2) × Tclk	(FLSH_WRT_DATA_IO_DSBL_TM (R0C974h [31:24]) + 2) × Tclk	ns

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